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DC-biased Suzuki stack circuit for Josephson-CMOS memory applications

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Abstract

Josephson-CMOS hybrid memory leverages the high speed and low power operation of single-flux quantum logic and the high integration densities of CMOS technology. One of the commonly used type of interface circuits in Josephson-CMOS memory is a Suzuki stack, which is a latching high-voltage driver circuit. Suzuki stack circuits are typically powered by an AC bias voltage that has several limitations such as synchronization and coupling effects. To address these issues, a novel DC-biased Suzuki stack circuit is proposed in this paper. As compared to a conventional AC-biased Suzuki stack circuit, the proposed DC-biased design can provide similar output voltage levels and parameter margins, approximately two times higher operating frequency, and three orders of magnitude lower heat load of bias cables.

Keywords: Suzuki stack circuit, Josephson latching driver, superconductor-semiconductor interface circuit, DC power supply, Josephson-CMOS hybrid memory, cryogenic memory

1. Introduction

Josephson-CMOS hybrid memory combines the best features of superconductor and semiconductor technologies [1]. Particularly, the superconducting digital electronics such as single-flux quantum (SFQ) technology can operate at extremely high switching frequency (tens to hundreds of GHz) and consume significantly low energy per switching activity, in the order of 10^{-19} J [2–5], whereas CMOS technology is mature and can provide a memory with high capacity [1].

To interface SFQ and CMOS circuits, a special circuit is needed that can amplify the SFQ pulses, which are in the order of 1 mV, to a voltage level appropriate for CMOS operation. A Suzuki stack circuit (a.k.a. Josephson latching driver) is a latching high-voltage driver circuit, originally proposed in 1988 by Suzuki *et al* [6] and is commonly used in Josephson-CMOS hybrid memories [7–9]. As compared to other types of superconductor-semiconductor interface circuits such as superconducting quantum interference device (SQUID) stack [10–13] and SFQ-to-DC converter [2, 14], the Suzuki stack circuit can generate the highest output voltage in the order of tens to hundreds of mV. As a result, the CMOS amplifier stage, which is connected to the output of a Suzuki stack circuit and located at the same temperature of 4 K would require lower gain and, hence, lower power dissipation [15].

The Suzuki stack, SQUID stack, and SFQ-to-DC converter interface circuits consist of Josephson junctions (JJs), which are two-terminal devices. Several studies propose

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novel superconducting three-terminal devices such as nanocryotron (nTron) [16], nanowire-meander switch [17], and superconducting-ferromagnetic transistor [18, 19], which could be used in a superconductor-semiconductor interface. For example, an nTron has been used as an interface between SFQ and CMOS circuits in [20]. As compared to the JJ-based interface circuits, an nTron can offer smaller layout area, higher output impedance, and lower power dissipation. However, due to the immature fabrication technology, which is a common drawback of novel superconducting three-terminal devices, an nTron-based Josephson-CMOS hybrid memory has not been fully realized [21]. The state-of-the-art Josephson-CMOS hybrid memory architectures [9] still prefer Suzuki stack circuits due to their relatively robust operation and mature fabrication technology. This work focuses on Suzuki stack interface circuits.

A Suzuki stack circuit is typically powered by an AC-type bias voltage [22]. This type of power supply is used to reset the underdamped JJs in Suzuki stack circuit once they switch from superconducting to resistive states. An AC-bias scheme, however, introduces several drawbacks in the design of Suzuki stack circuits such as synchronization and coupling effects [7, 23]. This paper proposes a novel design of Suzuki stack circuit with a DC-bias scheme that can resolve drawbacks of the conventional (AC-biased) design.

The following are the key contributions of this work.

- A DC-biased Suzuki stack circuit is proposed. This interface circuit is specifically designed for Josephson-CMOS memory located at 4 K.
- The existing designs of DC-biased latching drivers are reviewed. A list of limitations, which prevent the use of these circuits in Josephson-CMOS memory, are identified.
- Unique advantages and potential drawbacks of the proposed DC-biased Suzuki stack circuit are discussed and compared with the conventional (AC-biased) design. Particularly, important design parameters such as average output voltage, power dissipation, maximum frequency, operating margins, layout area, synchronization, coupling effects, compatibility with existing optimization techniques, and heat load of bias cables are considered.

The rest of the paper is organized as follows. The working principle and limitations of a conventional AC-biased Suzuki stack circuit are discussed in section 2. The related works on DC-biased latching drivers are reviewed in section 3. The proposed DC-biased Suzuki stack circuit is presented in section 4 and compared with the conventional AC-biased design in section 5. Related conclusions are drawn in section 6.

2. Overview of conventional AC-biased Suzuki stack circuit

In this section, a conventional AC-biased Suzuki stack circuit is discussed. Particularly, the working principle and existing limitations are presented in sections 2.1 and 2.2, respectively.

2.1. Working principle

The schematic of a conventional interface circuit of Josephson-CMOS memory is depicted in figure 1. This interface circuit consists of an AC-biased Suzuki stack, an AC-biased four-junction logic (4JL) gate [24], and a CMOS amplifier. The 4JL gate is commonly used as a pre-amplifier for input and output stability of Suzuki stack circuits [7].

The simulation results of AC-biased interface circuit are shown in figure 2. The circuit parameters are partially selected from [7, 15, 22] and listed in table 1. Additionally, JJs are simulated with a Verilog-A RCSJ model in MIT Lincoln Lab SFQ5ee 10 kA cm^{-2} process [25]. The parasitic capacitance to ground of 0.15 fF (assuming that the ground plane underneath the Suzuki stack circuit is removed as suggested in [22, 26]) and parasitic series inductance of 0.2 pH are added for each JJ in the stack. Additionally, the thermal noise at 4.2 K is accounted for in the simulations.

When an SFQ pulse is received at the input terminal $V_{\rm in}$, the JJs with the critical current of $I_{c1,4JL}$, $I_{c2,4JL}$, and $I_{c,SS}$ (see figure 1 for notation) switch from superconducting to resistive states. A more detailed description of the internal switching is explained in section 2 in [15]. Since these JJs are underdamped (i.e. Stewart–McCumber parameter $\beta_c \gg 1$), the voltage across each JJ changes from zero to a gap voltage $V_{\rm g}$, which is equal to 2.8 mV. As a result, the steady-state output voltage of 4JL gate is

$$V_{\rm out,4JL} \approx 2V_{\rm g} = 5.6\,{\rm mV}, \tag{1}$$

and the output voltage of the Suzuki stack circuit becomes

$$V_{\rm out,SS} \approx mV_{\rm g} + R_{br}I_{b,SS}/2 = 46\,{\rm mV}, \tag{2}$$

where m is the number of JJs connected in series in one branch of Suzuki stack circuit. In figure 2, m is selected as 16, similar to [7, 22].

Once all JJs switch to the resistive state, the output voltage remains high as long as the bias voltage is high as shown in figure 2. By turning off the bias voltage sources $V_{b,4JL}$ and $V_{b,SS}$, the current flowing through each JJ becomes zero, which resets them back into the superconducting state.

One may notice that figure 2 also contains the simulation results of a CMOS amplifier (i.e. $V_{\rm in,CMOS}$ and $V_{\rm out,CMOS}$). The simulation setup and results of CMOS circuits will be discussed and compared with the proposed interface circuit in section 4.

2.2. Limitations

Other types of interface circuits such as SQUID stack [10–13] and SFQ-to-DC converter [2, 14] are DC-biased and asynchronous. As compared to these interface circuits, the AC-bias scheme of Suzuki stack circuit possesses several limitations that are listed below.

(1) The heat load of AC-bias (e.g. coaxial) cables is generally higher than the heat load of DC-bias (e.g. twisted pair) cables [28], which makes the cooling power constraint more stringent.

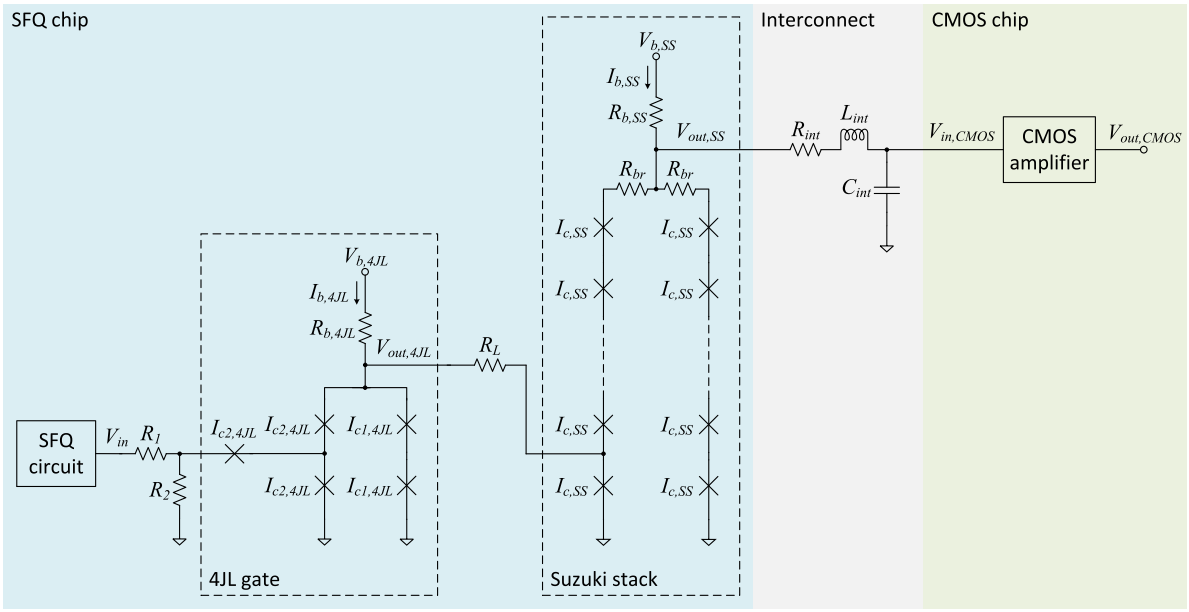

Figure 1. Schematic of the conventional interface circuit of Josephson-CMOS memory. The 4JL gate and Suzuki stack circuits (highlighted in dashed rectangles) are AC-biased (i.e. voltage sources $V_{b,4JL}$ and $V_{b,SS}$ are square-wave AC). Parasitic inductances of resistors, wires, and JJs are not shown.

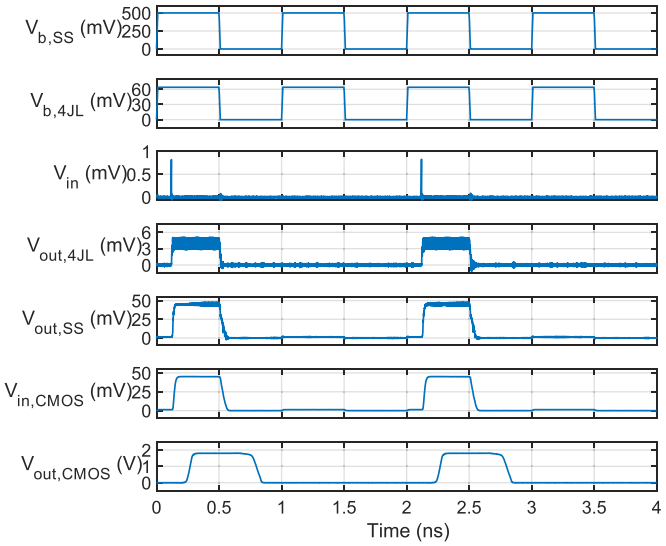

Figure 2. Simulation of the conventional AC-biased Suzuki stack circuit with 16 JJs in series. The notation is the same as in figure 1.

Table 1. Parameters of AC- and DC-biased Suzuki stack circuits.

Circuit	Parameter	Conventional AC-biased	Proposed DC-biased
Suzuki stack	$V_{b,SS}$	0–500 mV	500 mV
	$R_{b,SS}$	750 Ω	750 Ω
	R_{br}	4 Ω	4 Ω
	$I_{c,SS}$	400 μA	400 μA
	m	16	16
4JL gate	$V_{b,4JL}$	64 mV	64 mV
	$R_{b,4JL}$	200 Ω	200 Ω
	$I_{c1,4JL}$, $I_{c2,4JL}$	300, 100 μA	300, 100 μA
	R_L	10 Ω	10 Ω
	R_1, R_2	1, 2 Ω	1, 2 Ω
Interconnect	R_{int}	50 Ω	50 Ω
	L_{int}	100 pH	100 pH
	C_{int}	180 fF	180 fF
Passive reset	R_r	N/A	7 Ω
	L_r		150 pH
Active reset	W_{M_r}, L_{M_r}		10, 0.18 μm
	V_r		−50 mV

[a] All JJs are shunted with a resistance $R_{sh} = 6V_g/I_c$ (V_g is the gap voltage and I_c is the critical current) to achieve underdamped behavior [22].
[b] For each resistance R_i, a parasitic inductance $L_i = (R_i L_\square)/R_\square$ is added in series during simulations ($R_\square$ and $L_\square$ are sheet resistance and inductance of resistive, e.g. R5 layer in MIT Lincoln Lab process [27]).

(2) The large AC-bias voltage of Suzuki stack circuit that changes from, e.g. 0 to 500 mV, can influence SFQ circuits located on the same chip due to the coupling effects [7, 23]. To reduce the coupling effects, the SFQ circuit can be covered with a top Nb layer, which serves as a magnetic shield [7]. However, the additional shielding layer could make the design of SFQ circuits less flexible.
(3) The correct operation of Suzuki stack circuit relies on the synchronization of AC-bias voltage with the input SFQ pulses. Particularly, the SFQ pulse should be applied only when the bias voltage is high. This limitation can be partially solved by adding a storage inductor (to store flux Φ_0) at input terminal as has been proposed in [23]. Nevertheless, this inductor would require additional layout area.

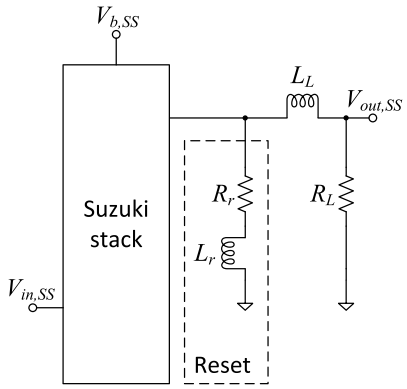

Figure 3. Schematic of a DC-biased Suzuki stack circuit with passive reset. The design has been proposed in [23]. Adapted from [23].

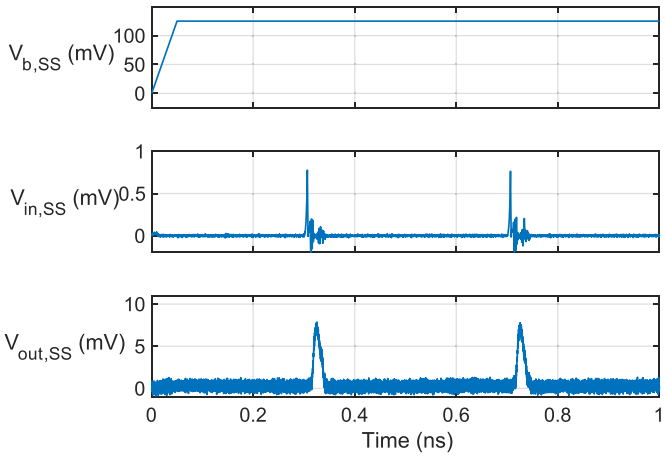

Figure 4. Simulation of the DC-biased Suzuki stack circuit with 4 JJs in series and passive reset. The bias voltage and resistance ($V_{b,SS}$ and $R_{b,SS}$) are set to 125 mV and 187.5 Ω, respectively (i.e. reduced by 4 times as compared to 16-JJ Suzuki stack).

By changing the AC-bias scheme of Suzuki stack circuit to the DC-bias scheme, the aforementioned limitations can be addressed, which is a primary objective of this paper.

3. Related work on DC-biased latching drivers

Several DC-biased latching drivers have been proposed by Suzuki and Tanabe in [23]. One of these drivers is a DC-biased high-voltage gate, which essentially has a similar schematic as the Suzuki stack circuit (see figure 5 in [23]). Instead of turning off the bias voltage $V_{b,SS}$ as in the conventional Suzuki stack circuit, the $V_{b,SS}$ is fixed to a constant (DC) value. The reset operation (i.e. switching all JJs from the resistive to superconducting states) is achieved by adding a resistor R_r and an inductor L_r in parallel to the output terminal, as shown in figure 3. Throughout this paper, this type of reset circuit is referred to as the 'passive reset' circuit.

The simulation results of the DC-biased Suzuki stack circuit with passive reset are shown in figure 4. In this figure, m is set to 4 similar to [23]. The circuit parameters are set to $R_r = 2.5\,\Omega$, $L_r = 250\,\text{pH}$, $R_L = 50\,\Omega$, $L_L = 100\,\text{pH}$ (see notation in figure 3), which satisfy the following four conditions that have been proposed in [23].

$$R_r < V_g/I_{c,SS}; \tag{3}$$

$$R_r \ll R_L; \tag{4}$$

$$L_r \gg L_L; \tag{5}$$

$$L_r/R_r \gg L_L/R_L. \tag{6}$$

As compared to a conventional AC-biased Suzuki stack circuit (with $m = 4$), the DC-biased design with the passive reset circuit has the following limitations.

(1) The time interval when the output voltage $V_{out,SS}$ is high (i.e. on-time), is limited by the time constant L_r/R_r. For example, in figure 4, the output pulse width is roughly equal to 26 ps. Such a small on-time could make the testing of fabricated circuits more difficult at low frequency mode. Particularly, the testing equipment may need a higher sampling rate to be able to capture the output signals. Alternatively, the on-time in the AC-biased design can be increased by simply changing the frequency of the bias voltage.

(2) The reset inductor L_r is relatively large (in the order of bias inductors in energy-efficient rapid SFQ (ERSFQ) circuits [29]), which adds to the area overhead.

(3) The peak output voltage $V_{out,SS}$ is smaller than in the AC-biased design (2). For instance, for $m = 4$, the maximum $V_{out,SS}$ is equal to 7.86 mV and 12.5 mV, respectively, in the DC- and AC-biased Suzuki stack circuits. This difference becomes even greater with larger value of m (e.g. for $m = 16$, $V_{out,SS}$ is 12.1 mV vs. 46.1 mV). Such behavior is caused by the passive reset circuit that activates according to the time constant L_r/R_r as soon as the first JJ is switched to the resistive state. Due to the parasitic inductance and capacitance in the Suzuki stack circuit, JJs do not switch simultaneously. As a result, the higher number of JJs in series would correspond to the longer rise time of the output voltage. When L_r/R_r is smaller than this rise time, a lower output voltage is produced.

(4) The output voltage $V_{out,SS}$ response (i.e. peak value and on-time) depends on the load condition. Due to the process parameter variations of R_r, L_r, R_L, and L_L, the $V_{out,SS}$ response can be different in a multi-channel interface circuit. As a result, the fabrication yield could be degraded.

The DC-biased Suzuki stack circuit with passive reset has been demonstrated in superconducting analog-to-digital converters [30–32]. However, due to the relatively low output voltage, short on-time, and other aforementioned limitations, this type of design cannot be used in a Josephson-CMOS memory, where the CMOS amplifier and memory are located at 4.2 K temperature. The state-of-the-art Josephson-CMOS memory designs still prefer using a conventional AC-biased Suzuki stack circuit as an interface circuit [7–9].

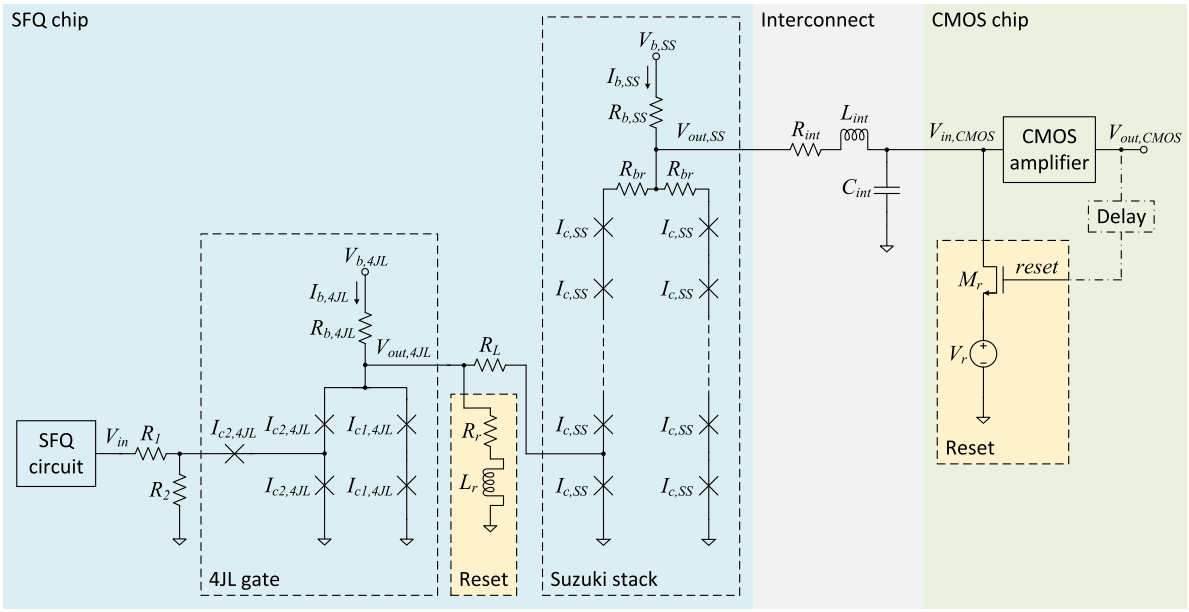

Figure 5. Schematic of the proposed interface circuit of Josephson-CMOS memory. The 4JL gate and Suzuki stack circuits (highlighted in dashed rectangles) are DC-biased (i.e. voltage sources $V_{b,4JL}$ and $V_{b,SS}$ are DC). The passive and active reset circuits are highlighted in yellow dashed rectangles. The elements in dash-dotted line show an optional configuration, where the interface circuit is automatically reset after certain delay time. Parasitic inductances of resistors, wires, and JJs are not shown. M_r is an NMOS transistor.

4. Proposed DC-biased Suzuki stack circuit

In this section, a novel DC-biased Suzuki stack circuit as an alternative interface circuit for Josephson-CMOS memory is proposed. The schematic of this proposed interface circuit is depicted in figure 5. It has a similar structure as in the conventional design (figure 1) except two circuit blocks highlighted in yellow dashed rectangles in figure 5. These circuit blocks are added to reset the 4JL gate and Suzuki stack circuits.

The first reset circuit, which is based on [23], consists of a resistor R_r and an inductor L_r similar to a passive reset circuit presented in section 3. This passive reset circuit is connected to the output of the 4JL gate, and its parameters are chosen according to the conditions (3)–(6).

The second reset circuit consists of a CMOS (particularly, NMOS) transistor M_r and a voltage source V_r. Since this reset circuit needs a *reset* signal to be applied to initiate the reset operation, it is referred to as the 'active reset' circuit. To reset the Suzuki stack circuit, the *reset* signal is applied to M_r, which acts as a switch. By setting V_r to a certain negative value, it is possible to redirect the bias current $I_{b,SS}$, which is initially flowing through JJs into the output terminal. As a result, all JJs in the Suzuki stack circuit switch from resistive to superconducting states. The DC-biased Suzuki stack circuit with passive and active reset leverages the co-design of both superconductor and semiconductor (SFQ and CMOS) chips and is proposed for the first time.

The circuit parameters of the proposed DC-biased interface circuit are similar to the conventional one and are listed in table 1. The simulation results of DC-biased interface circuit are shown in figure 6. As can be observed from this figure, the DC-biased Suzuki stack circuit operates correctly, producing the output voltage $V_{\mathrm{out,SS}}$ of approximately 45.0 mV. After the

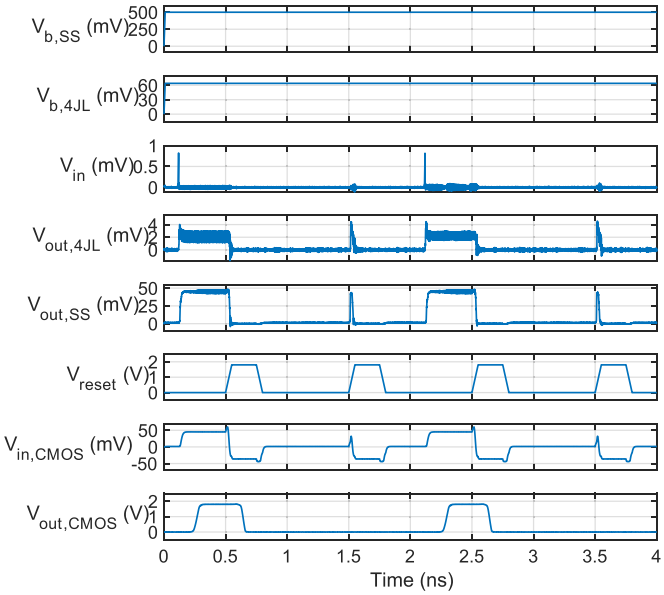

Figure 6. Simulation of the proposed DC-biased Suzuki stack circuit with 16 JJs in series. The notation is the same as in figure 5.

reset signal is applied, the $V_{\mathrm{out,SS}}$ becomes zero, signifying the successful reset operation. The proposed active reset circuit therefore resolves the existing limitations of passive reset circuit discussed in section 3.

One may notice that $V_{\mathrm{out,4JL}}$ in figure 6 is slightly smaller as compared to the AC-biased design in figure 2. Such voltage drop is mainly caused by the passive reset circuit. It should be noted that due to the underdamped behavior of JJs in the Suzuki stack, the 4JL gate does not have to provide a large input current for the entire clock cycle and is only needed at the

beginning to trigger the Suzuki stack circuit. In section 5.4, the margin analysis will show no significant difference between the AC- and DC-biased 4JL gate circuits (figure 7).

One may argue that when the active reset circuit is triggered, $V_{\text{in,CMOS}}$ can take some negative value due to the connected V_r and may disturb the correct operation of CMOS amplifier (see figure 5 for notation). To study this scenario, a CMOS amplifier (particularly, a self-biased differential source-follower amplifier) is considered. This type of amplifier is the most suitable for the interface circuit of Josephson-CMOS memory in terms of speed, robustness, and power consumption [33]. The transistor width parameters are partially taken from [7]. This amplifier is designed for 40 mV input voltage swing [33]. Although several cryogenic models of various CMOS technology nodes have been proposed in the literature [34–38], to the best of authors' knowledge, there is no open-access model available. In this work, the transistors are simulated by using a standard TSMC 0.18 μm predictive technology model (PTM) with the temperature set to 4.2 K. The simulation results are shown in figure 6. As can be seen from this figure, the negative voltage of $V_{\text{in,CMOS}}$ does not disturb the output voltage of CMOS amplifier ($V_{\text{out,CMOS}}$), making the proposed DC-bias scheme with active reset circuit a viable option. In fact, the output voltage swing of $V_{\text{out,CMOS}}$ is the same in AC- and DC-biased Suzuki stack circuits, as shown in figures 2 and 6 (i.e. from 0 V to 1.8 V). A similar behavior can be observed when the temperature is set to, e.g. 77 K and 300 K (i.e. when the CMOS amplifier is located at a higher temperature stage and the transistor model is more accurate). It should be noted that other types of CMOS amplifiers might operate incorrectly when $V_{\text{in,CMOS}}$ becomes negative due to the voltage source V_r. Further research is needed to understand the underlying physical behavior of CMOS amplifier with the active reset circuit.

Based on the simulation data, the minimum acceptable voltage swing and pulse duration of the input signal are approximately 12 mV and 100 ps, respectively. It should be noted that a higher input voltage swing (e.g. 40–45 mV) is desired to achieve a higher maximum operating frequency (i.e. data rate) of the CMOS amplifier.

In figure 6, the V_{reset} signal is simulated with a voltage source that switches from 0 to 1.8 V. In such a configuration, where the *reset* signal is decoupled from the main circuit, the proposed design requires the synchronization of SFQ input pulses and *reset* signals similar to the conventional (AC-biased) design. To make the proposed design asynchronous, the *reset* signal can be connected to $V_{\text{out,CMOS}}$ signal with a delay circuit (e.g. a chain of inverters) as shown in the dash-dotted line in figure 5. The duration of the delay circuit would determine the data pulse duration for the subsequent CMOS logic.

One may notice that $V_{\text{out,4JL}}$ and $V_{\text{out,SS}}$ in figure 6 have some spikes at around 1.5 and 3.5 ns. Such switching occurs when no input signal V_{in} is applied (i.e. logical '0'). These spikes are caused by the transient fluctuations of the output current of Suzuki stack circuit when the transistor M_r is turned on (i.e. V_r is connected to $V_{\text{in,CMOS}}$—see figure 5 for notation). Due to the inrush (a.k.a. input surge and switch-on surge) current effect, the output current (with the peak value of roughly 170 μA) starts flowing back into the stack for a short amount of time (around 10 ps). At this time instance, $(I_{b,\text{SS}} + 170\,\mu\text{A})/2 > I_{c,\text{SS}}$ resulting in switching of JJs from superconducting to resistive state. Once the transient period is passed, all JJs switch back to the superconducting state. Although these voltage spikes do not affect $V_{\text{out,CMOS}}$, they can be suppressed by adding a delay circuit and connecting the *reset* signal to $V_{\text{out,CMOS}}$, as shown in the dash-dotted line in figure 5. In this case, the *reset* signal is only applied when the input signal is logical '1'.

Table 2. Comparison of AC- and DC-biased Suzuki stack circuits.

Parameter	Conventional AC-biased	Proposed DC-biased
Average output voltage	45.1 mV	45.0 mV
Power dissipation[a]	170 μW	346 μW
Maximum frequency[b]	1.9 GHz	3.9 GHz

[a] Includes the power dissipation of Suzuki stack, 4JL gate, and passive reset circuits. The switching activity factor of $\alpha = 0.5$ is assumed.
[b] Simulated with CMOS amplifier circuit.

5. Comparison of AC- and DC-biased Suzuki stack circuits

In this section, a conventional AC-biased Suzuki stack circuit is compared with the proposed DC-biased design. For a fair comparison, the same circuit parameters of Suzuki stack, 4JL gate, and interconnect are considered (see table 1).

5.1. Output voltage

Since both designs (i.e. AC- and DC-biased Suzuki stack circuits) have the same number of JJs connected in series, the average output voltage $V_{\text{out,SS}}$ is approximately the same. Particularly, for AC- and DC-biased designs, the simulated $V_{\text{out,SS}} = 45.1$ and 45.0 mV, respectively (table 2).

5.2. Power dissipation

In Suzuki stack circuits, most of the power is dissipated across the bias resistor $R_{b,\text{SS}}$ [39]. A similar observation holds for the 4JL gate. By observing the bias voltage $V_{b,\text{SS}}$ and $V_{b,\text{4JL}}$ waveforms in figures 2 and 6, the DC-biased design seems to dissipate roughly two times more power because its bias voltage sources are always turned on, whereas these voltage sources are turned on only for a half of the clock cycle in the AC-biased design. As shown in table 2, the simulated power dissipation of DC-biased design is approximately 2.04 times higher as compared to the AC-biased design. The increased power dissipation of DC-biased Suzuki stack circuit can potentially be mitigated by using an optimization technique in [39], which can reduce the power dissipation by 30%–70%.

Besides the superconducting circuits, the DC-biased design also require an additional transistor M_r (figure 5). Since this

transistor operates as a switch, its on resistance R_{on} contributes the power dissipation. The power dissipation of M_r is simulated to be around 3.20 μW, which is less than 1% of the Suzuki stack power dissipation (table 2). This value could be further reduced by, e.g. increasing the transistor width (lower R_{on}) and/or reducing the on-time of the *reset* signal.

5.3. Maximum frequency

The simulated maximum frequency values of the AC- and DC-biased designs are listed table 2. It should be noted that the reported values are mainly limited by the CMOS amplifier. The Suzuki stack circuit can actually operate at much higher frequencies. In the DC-biased design, the on-time of *reset* signal may affect the maximum operating frequency. The circuit designer should make sure that the *reset* signal is turned OFF before the next SFQ input pulse is received. During simulations, the on-time is set to 1/5 of the total period. As listed in table 2, the maximum frequency of DC-biased design is about 2.05 times higher than that of the AC-biased design. Such a large difference is caused by the active reset circuit. Particularly, the negative voltage source V_r at the input terminal of CMOS amplifier causes the high-to-low transition of $V_{out,CMOS}$ to be faster, as shown in figures 2 and 6. Additionally, the propagation delay of interconnect no longer affects the high-to-low transition of $V_{out,CMOS}$ since the reset circuit is located on the CMOS chip (figure 5).

5.4. Margins

The simulated operating margins of the AC- and DC-biased designs are shown in figure 7. Overall, the margins of AC- and DC-biased designs are similar to each other, except for the lower margin of $V_{b,SS}$ and the upper margins of $R_{b,SS}$ and $I_{c,SS}$. The difference is mainly caused by the pre-amplifier circuit (particularly, passive reset circuit), which supplies a slightly different input current for the Suzuki stack circuit. Nevertheless, in both designs, the bias margins (i.e. $V_{b,SS}$ and $V_{b,4JL}$) are within $\pm$20% variation range, which is on par with the existing Suzuki stack circuits [7].

5.5. Area

Since the circuit parameters of Suzuki stack and 4JL gate are the same in both designs (table 1), the corresponding layout area on the SFQ chip should be identical. However, the DC-biased design contains an additional passive reset circuit, which consists of a resistor R_r and an inductor L_r (figure 5). Assuming that L_r and R_r are implemented with L0 (high kinetic inductance with $L_\square = 8$ pH/$\square$) and R5 (resistor with $R_\square = 2\ \Omega/\square$) layers, respectively, in MIT Lincoln Lab SFQ5ee process, the minimum layout area of the passive reset circuit would be approximately 76 μm^2, which corresponds to approximately less than 1% area overhead as compared to the total layout area of Suzuki stack circuit. Regarding the CMOS chip, the active reset circuit should have a minor area overhead thanks to high integration densities in modern CMOS technology nodes.

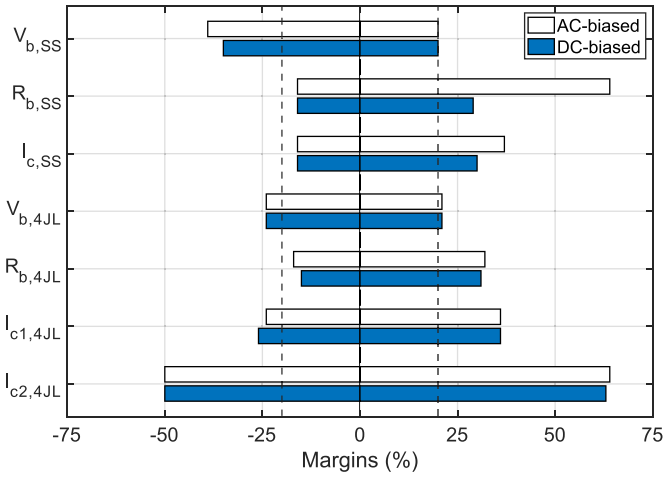

Figure 7. Simulated operating margins of the AC- and DC-biased Suzuki stack circuits. Two vertical dashed lines show $\pm$20% boundaries. The frequency is set to 1 GHz and the nominal circuit parameters are the same as in table 1.

5.6. Synchronization

The proposed DC-biased design is asynchronous assuming that the *reset* signal is applied from the feedback circuit as shown in the dash-dotted line in figure 5. In this design, the input signal can be applied at any time instance because the bias voltage is always high. Therefore, the proposed design resolves one of the key limitations of AC-biased design, as discussed in section 2.2.

5.7. Coupling effects

In a typical multi-channel Suzuki stack interface (e.g. see figure 6 in [22]), all channels are powered by a single voltage source and the bias current is distributed through the bias resistor network. In the AC-biased Suzuki stack design, the total bias current supplied by the voltage source changes from zero to a few mA (e.g. 30-channel interface would require 20 mA bias current). To reduce the influence of coupling effects, the SFQ circuits can be covered with a top Nb layer as has been implemented in [7].

In the DC-biased Suzuki stack design, the total bias current stays on the same level of a few mA (i.e. without dropping to zero every clock cycle). During the reset operation, only the current flowing through each JJ of individual channel changes from a few hundreds of μA to zero. Therefore, with the DC-biased Suzuki stack interface, the SFQ circuits do not require this top Nb layer. The absence of this shielding layer could result in greater flexibility for the design of SFQ circuits on the same chip. Alternatively, the additional Nb layer can be employed to facilitate the routing of additional signals among diverse circuit blocks on the chip.

5.8. Compatibility with existing optimization techniques

Recently, several optimization techniques have been proposed for the conventional AC-biased Suzuki stack design. These

techniques focus on optimizing the power dissipation [39] and differential signaling [15]. Due to the similar internal design and working principle of Suzuki stack circuit, these optimization techniques can also be applied to the proposed DC-biased design.

5.9. Heat load of bias cables

In a multi-channel interface circuit, several Suzuki stack circuits typically share a single power supply (i.e. $V_{b,\mathrm{SS}}$) [22]. Similarly, the 4JL gates require a separate power supply (i.e. $V_{b,\mathrm{4JL}}$). As a result, a multi-channel interface circuit requires at least two bias cables that can deliver $V_{b,\mathrm{SS}}$ and $V_{b,\mathrm{4JL}}$. In this subsection, a heat load of AC- and DC-bias cables is compared. As a case study, a 64 kb Josephson-CMOS memory that requires 30 input channels similar to [8] is considered.

The AC- and DC-bias cables are modeled and simulated in ANSYS HFSS and ANSYS Maxwell, respectively. For the AC-bias cable, a 20 cm long, 0.034″ diameter copper coaxial cable with Teflon insulation is simulated in HFSS at 4.2 K temperature. The residual-resistance ratio (RRR) of copper is 100. To capture copper's behavior at 4.2 K, its bulk conductivity is set to 6.44 GS m^{-1} [40]. The simulated S-parameter S_{12} has a magnitude of 0.9934. Thus, 0.0066 of the cable's input power is dissipated as a heat. At the operating frequency of 1 GHz, the simulated AC-bias cables dissipate 4.06 μW and 66.0 μW of heat, respectively, for the 4JL gate and Suzuki stack circuits.

For the DC-bias cable, a 20 cm long, 36 AWG twisted pair cable with polyimide insulation is simulated in Maxwell at 4.2 K. The simulated ohmic loss of the cable shows the power dissipated from the cable as a heat. For the 4JL gate and Suzuki stack DC-bias cables, the simulated loss is 7.97 nW and 34.6 nW, respectively. Therefore, the DC-bias cables dissipate three orders of magnitude lower heat load as compared to the AC-bias cables.

6. Conclusion

In this paper, a novel DC-biased Suzuki stack circuit is proposed. The proposed design includes an active reset circuit and overcomes the limitations of existing DC-biased latching drivers such as low output voltage, short on-time, and sensitivity to process parameter variations, making it suitable for Josephson-CMOS memory applications. The DC-biased Suzuki stack circuit is compared with the conventional AC-biased design. The proposed DC-biased design can provide similar output voltage and parameter margins, 2.05 times higher maximum frequency, asynchronous operation, less coupling effects, compatibility with existing optimization techniques, and lower heat load of bias cables as compared to the AC-biased design. However, the trade-off is the 2.04 times higher power dissipation. This higher power dissipation can potentially be mitigated by existing power optimization techniques.

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Data availability statement

No new data were created or analysed in this study.

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