Built-In Self-Test of SFQ Circuits Using Side-Channel Leakage Information

Yerzhan Mustafa, *Graduate Student Member, IEEE*, and Selçuk Köse, *Member, IEEE*

***Abstract*— Cryogenic testing and verification of single-flux quantum (SFQ) circuits consist of various challenges, such as limited number of input–output pins, flux trapping, and cooling power constraints. Developing design for testability (DFT) techniques for SFQ circuits, which address these challenges, is an important research area. In this work, a built-in self-test (BIST) methodology of SFQ circuits is proposed, which focuses on a novel way of the readout of test signals by using side-channel leakage information. The side-channel leakage can exhibit the dependence of internal data (logical "1" and "0") on the power consumption. By measuring the variations in the power supply of an SFQ circuit at room temperature, the information about internal test signal states can be extracted with the proposed BIST methodology. As a case study, a rapid SFQ (RSFQ) 4-to-2 priority encoder circuit is considered. The existing Josephson junction (JJ)-based stuck-at fault model is applied with the proposed BIST methodology. The proposed BIST design is compared with a conventional shift register-based readout circuitry. The proposed BIST design can provide 79% lower static power consumption and 65% lower layout area. In addition, other advantages and drawbacks of the proposed design are discussed, such as yield, number of pins, testing time, interpretation of test results, and hardware security.**

***Index Terms*— Built-in self-test (BIST), cryogenic testing and verification, design for testability (DFT), SFQ-to-dc (SFQ/dc) converter, side-channel attack, single-flux quantum (SFQ) circuits.**

I. Introduction

SINGLE-FLUX quantum (SFQ) logic is a type of Josephson junction (JJ)-based superconducting digital logic family that can operate at extremely high switching frequency (tens to hundreds of GHz) and consume significantly low energy per switching activity, in the order of 10^{-19} J [1], [2], [3], [4]. Such characteristics make this technology a promising candidate for beyond-CMOS large-scale data centers and cloud computing [4]. In addition, SFQ technology can be used in a superconducting quantum computing system as a scalable and energy-efficient in-fridge control and readout circuitry [5], [6].

Information is represented in pulsed-based signals in SFQ logic. Since the presence (absence) of an SFQ pulse corresponds to a logical "1" ("0"), the existing test and verification techniques developed for CMOS technology cannot be directly applicable to SFQ circuits. There has been a number of studies investigating design for testability (DFT) techniques. These techniques include test point insertion and set/scan chains [7], [8]; JJ-based stuck-at fault detection models [9]; structural and defect-oriented testing [10], [11]; automatic test pattern generation (ATPG) paradigm for dynamic timing verification and path delay fault testing [12]; overflow, pulse-escape, and pattern-sensitive fault models [13]; and on-chip high-frequency testing using pseudorandom binary sequence (PRBS) generator [14], [15], [16], [17].

A built-in self-test (BIST) is a DFT technique that allows the circuit under test to perform self-testing by using specific hardware and/or software components [18]. This technique can enable testing of circuits that are difficult (or even impossible) to access through external pins located on chip (e.g., embedded memories [18]). Alternatively, the BIST is useful when the number of pins dedicated for testing is limited.

In this article, a novel BIST methodology for SFQ circuits is proposed that leverages side-channel leakage mechanism to extract the information about readout test signals without requiring any output pins. This side-channel leakage mechanism in SFQ circuits was uncovered in [19] to implement malicious attacks on superconducting quantum computing systems. It has been found that by measuring the variations in the power supply of an SFQ circuit at room temperature, the applied input bits to specific logic cells, namely, SFQ-to-dc converters, can be decoded. Instead of using this side-channel leakage information for malicious purposes as in [19], this work proposes an alternative perspective on using this information in the area of DFT and BIST. Although the proposed BIST methodology focuses only on the readout of test signals, it can also be combined with other DFT techniques, such as test point insertion and set/scan chains [7].

The proposed BIST design consists of the insertion of SFQ-to-dc converters, which are the output interface circuit based on a toggle (T) flip-flop. The SFQ-to-dc converter was originally proposed in [20] and is still commonly used in high-speed digital data links [21], [22], [23] as well as superconducting qubit control and readout circuitry [6], [24]. In this work, the SFQ-to-dc converter circuit is used, because it has the largest side-channel leakage signal as compared to other SFQ logic gates [19].

The following are the key contributions of this work.

1) A novel BIST methodology for SFQ circuits using side-channel leakage information is proposed.

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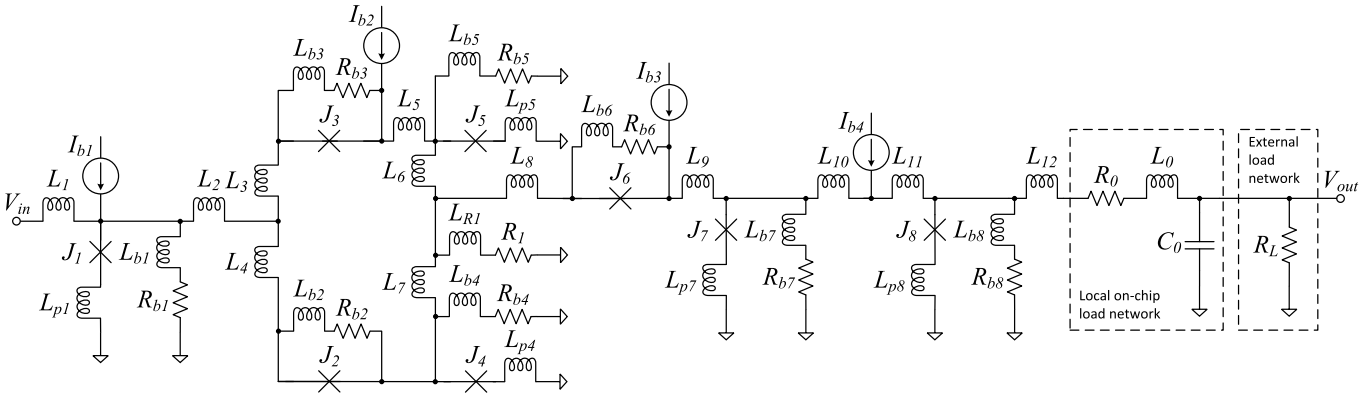

Fig. 1. Schematic of an SFQ-to-dc converter. The circuit parameters are available in [25].

By connecting SFQ-to-dc converters to the test signals and monitoring the variations in the power dissipation at room temperature, a test engineer can identify the correct/incorrect operation.

2) As a case study, a rapid SFQ (RSFQ) 4-to-2 priority encoder is considered. By manually inserting faults in this circuit (using circuit-level simulations) and applying the proposed BIST methodology, the locations of these faults are determined. In addition, possible limitations in more complex SFQ circuits are discussed.
3) The effects of thermal and switching noise as well as process parameter variations on the side-channel leakage signal are analyzed.
4) The primary reasons for why the proposed testing methodology can be classified as BIST are discussed.
5) The proposed BIST design is compared with a conventional shift register-based readout circuitry in terms various parameters, such as power consumption, layout area, number of pins, clock distribution network, testing time, interpretation of test results, and security.

The rest of this article is organized as follows. The side-channel leakage mechanism in SFQ-to-dc converters is explained in Section II. The proposed BIST methodology is presented in Section III and compared with a conventional shift register-based design in Section IV. Conclusions are drawn in Section V.

II. Overview of Side-Channel Leakage in SFQ-to-DC Converters

A side-channel leakage mechanism in SFQ circuits, particularly, SFQ-to-dc converters, has been uncovered for the first time in [19]. The key concepts and findings of this leakage mechanism that has been presented in [19] are briefly discussed in this section.

The standard SFQ logic cells, such as AND, OR, and NOT gates, produce an SFQ output pulse (in the case of a logical "1") that is around 1 mV in amplitude and 2-ps duration. Such a short switching has a minor effect on the power supply variations resulting undetectable side-channel leakage. On the other hand, the SFQ-to-dc converter circuit has a unique type of switching, where the output junction constantly switches (i.e., produces a set of SFQ pulses) during one clock cycle.

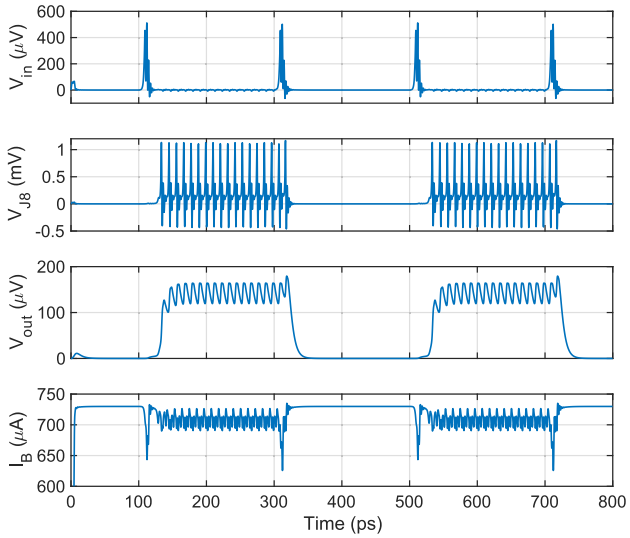

Fig. 2. Simulation results of an RSFQ SFQ-to-dc converter. I_B is the total bias current supplied by the voltage source $V_B = 2.6$ mV. The local and external load networks are set to $R_0 = 50\ \Omega$, $L_0 = 100$ pH, $C_0 = 200$ fF, and $R_L = 150\ \Omega$ (see Fig. 1 for notation).

As a result, the side-channel leakage signal can be observed in SFQ-to-dc converters [19].

The schematic of an SFQ-to-dc converter is depicted in Fig. 1. This circuit is designed based on SuperTools/ColdFlux RSFQ cell library [25] and MIT Lincoln Laboratory's 10-kA/cm^2 process, including the postlayout (extracted) circuit parameters. The working principle of the SFQ-to-dc converter, which is realized in RSFQ logic style, is shown in Fig. 2. The simulation results are obtained using JoSIM tool [26]. The output of an SFQ-to-dc converter switches in a toggled/latched manner. In particular, the output voltage V_{out} transitions from either high to low or low to high when the input SFQ pulse (i.e., logical "1") is received, as shown in Fig. 2. Such type of switching is caused by the T flip-flop connected to the dc SQUID (superconducting quantum interference device) in Fig. 1. As demonstrated in Fig. 2, the bias current I_B has different values depending on the state of the output voltage V_{out} (i.e., low- and high-voltage states). In particular, when V_{out} is low (high), the average I_B is equal to 730 μA (708 μA), which corresponds to 22-μA difference. This difference is mainly caused by the output junction J_8 (see Fig. 1 for

notation). By measuring the bias current of RSFQ SFQ-to-dc converter, one can identify the transitions of its output voltage and the applied SFQ input signals. Therefore, there is a side-channel leakage that carries information related to the input signals in the form of variations in the bias current.

When more than one SFQ-to-dc converters are connected to the same power delivery network, it is possible to identify the total number of outputs that are in the high state by looking at the side-channel leakage information. In this work, this number is referred to as Hamming weight (HW) of SFQ-to-dc converters' output states and will be used in the proposed BIST methodology in Section III.

The effects of thermal (4.2 K) and switching noise on the side-channel leakage have been studied in [19]. The following is a brief summary of two noise sources.

A. Thermal Noise

Thermal (a.k.a. Johnson–Nyquist) noise is an electronic noise generated by resistive elements. In RSFQ circuits, the main source of thermal noise is bias resistors and shunt resistors of JJs. Due to the random nature, this type of noise can affect the individual measurements of the bias current I_B. Nevertheless, due to the Gaussian distribution, the effect of thermal noise can be reduced by averaging (or using low-pass filter). For example, by averaging the measured trace of bias current over 100 ps, the effect of thermal noise can be limited to ± 2–3 μA [19].

B. Switching Noise

In complex SFQ circuits, multiple logic gates are connected to a single power supply. Since the side-channel leakage is desired to be measured from SFQ-to-dc converters, the remaining logic gates (e.g., AND, OR, and NOT) generate the switching noise in the power supply that may degrade the side-channel leakage signal. As uncovered in [19], the SFQ-to-dc converter has the largest side-channel leakage signal (around 22 μA) as compared to other SFQ logic gates. As a result, similar to the thermal noise, the effect of switching noise on the side-channel leakage signal can be suppressed with sufficient averaging [19]. Therefore, the detection of side-channel leakage information in SFQ-to-dc converters can be assumed feasible in a realistic setup.

A similar side-channel leakage mechanism in ERSFQ-based SFQ-to-dc converter has also been studied in [19]. Although this article focuses on RSFQ logic style [1] during the following case studies, the proposed BIST methodology can also be applied for ERSFQ circuits [27].

III. Proposed BIST Methodology of SFQ Circuits

In this section, the proposed BIST of SFQ circuits using side-channel leakage information is detailed. The general test structure and methodology are presented in Section III-A. A pass/fail classification algorithm is proposed with an example (case study) circuit in Section III-B. The JJ-based stuck-at fault model is considered in Section III-C. The intuition behind the proposed testing methodology and justification why this methodology can be classified as a BIST are discussed in Section III-D.

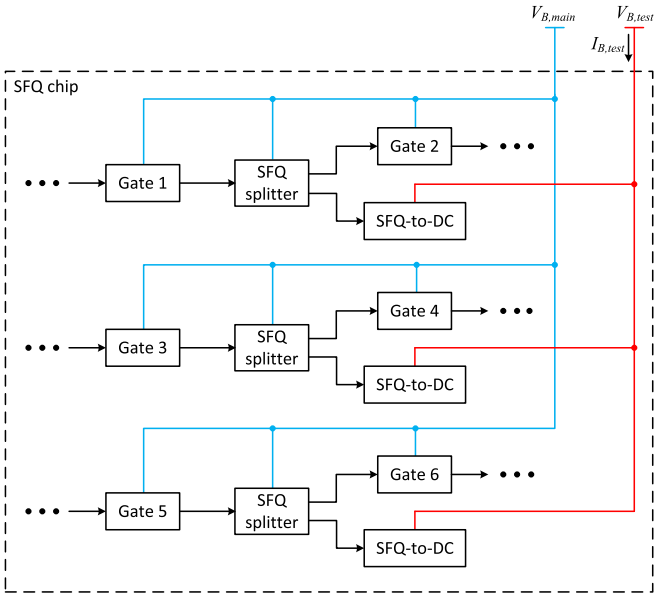

Fig. 3. Block diagram of the test signal readout using the SFQ-to-dc converters. The main and test bias networks are shown for RSFQ logic style.

A. Test Signal Readout Using SFQ-to-DC Converters

The proposed BIST methodology exploits the side-channel leakage mechanism of SFQ-to-dc converters, which is discussed in Section II. A block diagram of the proposed test signal readout is shown in Fig. 3. To read out a test signal between two consecutive SFQ gates, one SFQ splitter and one SFQ-to-dc converter are required. It should be noted that the output terminal of SFQ-to-dc converter is not connected (i.e., floating). Such configuration does not have a significant effect on the side-channel leakage signal as will be demonstrated in Section III-B.

The proposed testing circuit consists of two power delivery networks. In RSFQ logic style, these networks are for the following: 1) the main bias voltage $V_{B,\text{main}}$, which powers the original SFQ circuits and testing SFQ splitters and 2) the test bias voltage $V_{B,\text{test}}$, which powers the SFQ-to-dc converters, as shown in Fig. 3. Two power delivery networks are implemented for two main reasons: 1) to reduce power consumption during normal operation by turning off $V_{B,\text{test}}$ and 2) to minimize the impact of switching noise from $V_{B,\text{main}}$ on the side-channel leakage signal in SFQ-to-dc converters.

Since all SFQ-to-dc converters are connected to $V_{B,\text{test}}$, it is possible to measure the variations in the bias current $I_{B,\text{test}}$ and extract information about the test signals (Fig. 3). Specifically, the HW of SFQ-to-dc converters' output states can be determined. This HW information is used as a metric to classify whether the circuit operates correctly or not in Section III-B.

SFQ circuits operate at cryogenic temperatures (e.g., liquid helium at 4.2 K). However, the power supply ($V_{B,\text{main}}$ and $V_{B,\text{test}}$) is often generated at the room temperature and delivered through cryogenic cables to the SFQ chip. Such configuration is caused by the limited cooling power at 4.2 K, which is around 1–1.5 W [28]. Therefore, we can assume that $V_{B,\text{test}}$ is supplied from room temperature electronics, and the test signal readout can be performed by measuring

$I_{B,\text{test}}$ at room temperature. For example, *Octopux*, which is an automated setup for testing superconducting (including SFQ) circuits [29], can supply $V_{B,\text{test}}$ on a dedicated pin and measure its bias current $I_{B,\text{test}}$. Due to the data acquisition rate of up to 2 MS/s [29], this testing equipment can allow only low-frequency measurements. Note that $V_{B,\text{main}}$ can be generated from any thermal zone (e.g., room temperature, 77 K, and so on) and does not affect the testing results.

B. Pass/Fail Classification

Since all SFQ-to-dc converters' output states are initially low, which is expected when $V_{B,\text{test}}$ has just been powered up and can be controlled by a test engineer, it is possible to identify the correct waveform/trace of HW for a given input sequence. If the test circuit does not operate correctly, some of the SFQ-to-dc converters may not switch due to the absence or presence of SFQ pulse. As a result, the HW trace would be different from the trace obtained during simulations. A pass/fail classification algorithm, which uses the proposed test signal readout information, is proposed, as shown in Algorithm 1. The proposed algorithm records the bias current $I_{B,\text{test}}$ and converts it into HW trace, which can later be compared with the reference trace. This algorithm can be used during the mass production of chips. For instance, if the measured HW trace is different from the reference trace, which can be obtained from ideal simulations, the chip under test can be classified as failed and discarded.

Algorithm 1 Pass/Fail Classification

Input: Test vector, simulated/reference Hamming weight (HW) trace for the given test vector, number of traces n.
Output: 'Pass' or 'Fail'.
Step 1: Turn ON the bias voltage $V_{B,main}$.
Step 2:
for $k \leftarrow 1$ to n **do**
  Turn ON the bias voltage $V_{B,test}$.
  Apply the test vector to the circuit-under-test (CUT).
  Record the bias current $I_{B,test}(k)$.
  Turn OFF the bias voltage $V_{B,test}$.
Step 3: Calculate the average of the measured $I_{B,test}$ traces.
Step 4: Convert the averaged $I_{B,test}$ trace to the HW trace.
Step 5: Compare the measured HW trace with the reference:
  if traces are identical **then**
    Output 'Pass'
  else
    Output 'Fail'
Step 6: Turn OFF the bias voltage $V_{B,main}$.

To better illustrate the process of obtaining the HW trace, let us consider an arbitrary circuit, such as an RSFQ 4-to-2 priority encoder, that is depicted in Fig. 4. The working principle and possible applications of this circuit have been discussed in [30]. In this case study, the proposed BIST methodology is applied to readout the three test signals, A, B, and C, as depicted in Fig. 4.

The simulation results of an RSFQ 4-to-2 priority encoder with three test signals are shown in Fig. 5. In this figure,

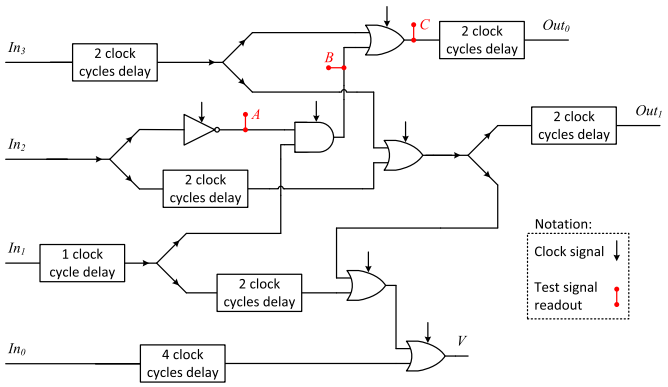

Fig. 4. Schematic of an RSFQ 4-to-2 priority encoder with three test signals A, B, and C. The design is taken from [30].

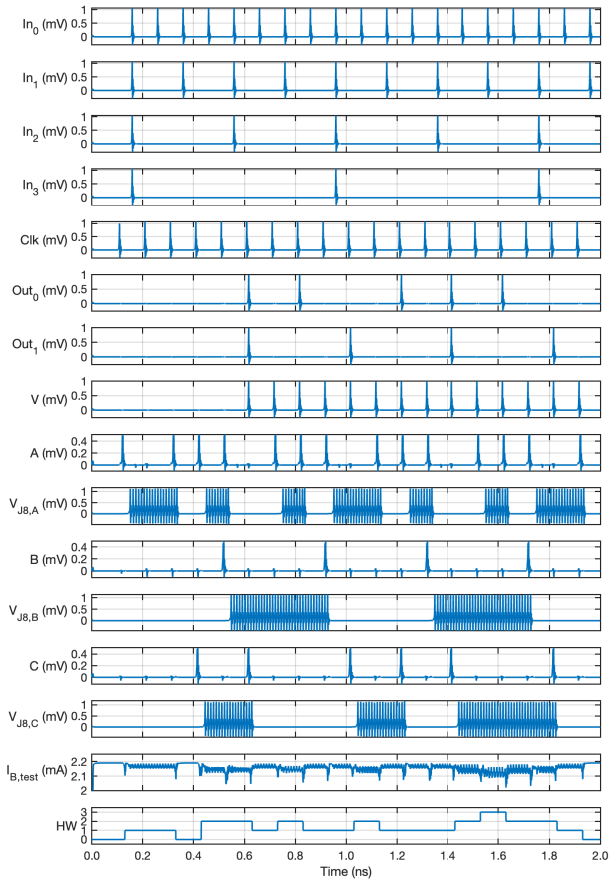

Fig. 5. Simulation results of an RSFQ 4-to-2 priority encoder with three test signals A, B, and C. For each test signal, one SFQ splitter and one SFQ-to-dc converter are connected as per the proposed BIST methodology. All SFQ gates are simulated using SuperTools/ColdFlux RSFQ cell library [25] and MIT Lincoln Laboratory's 10-kA/cm^2 process.

$V_{J8,i}$ refers to the voltage on output junction J_8 (see Fig. 1 for notation) of the SFQ-to-dc converter connected for the readout of test signal i. Hence, when J_8 is switching, the output voltage state of the corresponding SFQ-to-dc converter can be classified as high and vice versa.

During the static operation (i.e., no input signals are applied), each SFQ-to-dc converter consumes 730 μA of bias current, making the total bias current $I_{B,\text{test}} = 3 \times 730\ \mu\text{A} = 2.190$ mA. As mentioned in Section II, when RSFQ SFQ-to-dc converter switches to the

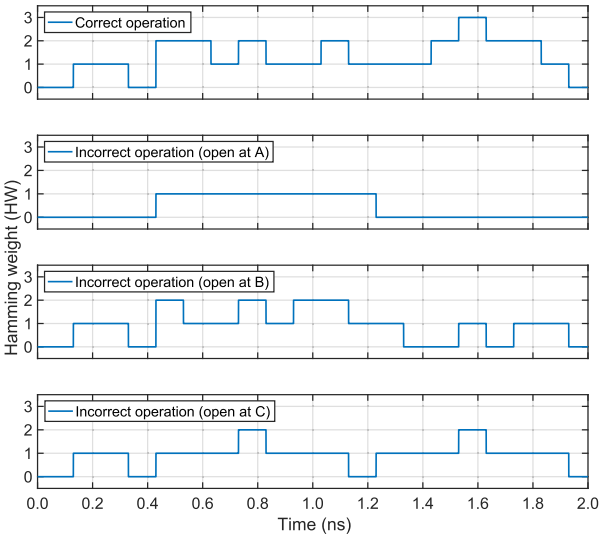

Fig. 6. Comparison of the extracted HW from the bias current $I_{B,\text{test}}$ of the RSFQ 4-to-2 priority encoder. The applied input signals are the same as in Fig. 5.

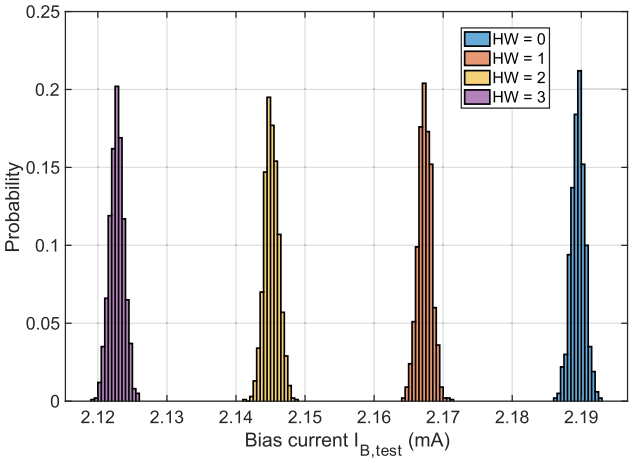

Fig. 7. Histogram of the simulated bias current $I_{B,\text{test}}$ of three SFQ-to-dc converters with thermal noise (4.2 K). $I_{B,\text{test}}$ is averaged over 100-ps time interval and recorded 1000×.

high output voltage state, the corresponding bias current drops by approximately 22 μA. In fact, such a drop in the bias current scales linearly with the number of converters that are in the high state. For example, when all of the three RSFQ SFQ-to-dc converters are in the high state, the $I_{B,\text{test}}$ drops by around $3 \times 22 = 66$ μA. The same behavior can be observed in $I_{B,\text{test}}$ waveform, as shown in Fig. 5. By measuring $I_{B,\text{test}}$, a test engineer can map the drops in the bias current to the HW of the SFQ-to-dc converters' output states, as shown in the lowermost trace in Fig. 5. In particular, if $I_{B,\text{test}} = 2.190$ mA-22 μA $= 2.168$ mA, the HW is 1. Similarly, if $I_{B,\text{test}} = 2.190$ mA-66 μA $= 2.124$ mA, the HW becomes 3. Such mapping corresponds to Step 4 in Algorithm 1.

The HW traces for both correct and incorrect operations are demonstrated in Fig. 6, where the same circuit is simulated under various fault conditions. In particular, three open circuit faults are separately inserted right before the test signals A, B, and C (Fig. 4). The open circuit fault can model the physical disconnection of signal line and/or incorrect operation of the preceding SFQ logic gate, where no SFQ pulses are produced.

To study the effect of thermal noise on the side-channel leakage signal, the $I_{B,\text{test}}$ of three SFQ-to-dc converters is recorded 1000× and averaged over 100-ps time interval. The thermal noise is inserted by setting the temperature and bandwidth parameters to 4.2 K and 10 THz, respectively, in JoSIM tool [26]. The histogram of the simulation results is depicted in Fig. 7. For a fair comparison, each combination of HW value (i.e., 0, 1, 2, and 3) is simulated equal number of times. As shown in Fig. 7, all four HW distributions are distinguishable from each other. The largest probability peaks are located at 2.123, 2.145, 2.168, and 2.190 mA, which corresponds to roughly 22-μA difference and coincides with the previous discussion. In addition, there is no overlap between these distributions, making the $I_{B,\text{bias}}$ and HW information mapping accurate even in the presence of thermal noise. Therefore, with 100-ps averaging time interval, one measurement trace (i.e., $n = 1$) would be sufficient for Algorithm 1.

When the SFQ chip is fabricated, its bias current could deviate from the nominal design value due to the process parameter variations. To study the effect of these variations on the side-channel leakage signal, each circuit parameter of an SFQ-to-dc converter is swept assuming ±20% variation. It is determined that the bias resistors R_{b3} and R_{b4}, which set the bias current I_{b3} and I_{b4} in Fig. 1, and the critical current values of J_7 and J_8 have the largest effect of the side-channel leakage. In particular, the side-channel leakage signal deviates at most by $+12$ and -9 μA from the nominal value of 22 μA. In the presence of the local parameter variations, the side-channel leakage signals could be more difficult to detect. Nevertheless, with the continuous advancement of SFQ fabrication processes, where the circuit parameter variations are reduced, the proposed BIST methodology can be assumed feasible. Alternately, as a subject of the future research, one may create an SFQ circuit that can generate similar side-channel leakage signal while being less susceptible to the process parameter variations.

It should be noted that 22-μA variation in the bias current $I_{B,\text{test}}$ could be detected by using, e.g., *Octopux* testing setup, which has an accuracy of 0.5 μA at ±5-mA scale [31]. In addition, the detectable side-channel leakage in CMOS circuits is in the order of nA, which is three order of magnitude smaller than in SFQ circuits [19], [32]. If the current probe at room temperature has a limited resolution (i.e., less than 22 μA) or there is additional noise due to coupling effects, it is possible to further increase the side-channel leakage signal by connecting multiple SFQ-to-dc converters to a single test signal. Furthermore, one can insert another type of SFQ/CMOS interface circuit, such as Suzuki stack (a.k.a., Josephson latching driver) [33], [34], instead of the SFQ-to-dc converter. Due to the larger output voltage, the Suzuki stacks generate side-channel leakage signals in the order of 50 μA [35].

C. Fault Detection

The test vector generation is essential for the successful detection of faults. In the proposed BIST methodology,

the test signal information is contained in the HW trace. Due to the toggled/latched switching of SFQ-to-dc converters, the existing test vector generation algorithms cannot be directly used with the proposed BIST methodology. To solve this issue, the test vector, which is originally designed for the conventional readout, should be modified, as shown in Algorithm 2. By repeating each input bit within the test vector (see Step 1 in Algorithm 2), the toggled/latching switching of SFQ-to-dc converters can be transformed into return-to-zero format. As a result, the incorrect switching of SFQ logic gates can be visible in the HW trace.

Algorithm 2 Fault Detection With the Proposed BIST Methodology

Input: Test vector from the fault model with conventional readout, netlist of the circuit-under-test (CUT), number of traces n.
Output: 'No faults are detected' or 'Fault is detected'.
Step 1: Modify the test vector by repeating each input bit (*e.g.*, $10100 \rightarrow 1100110000$).
Step 2: Simulate CUT with the modified test vector.
Step 3: Record the bias current $I_{B,test}$.
Step 4: Convert the recorded $I_{B,test}$ to the HW trace ($HW_{reference}$).
Step 5: Run Algorithm 1. Input the modified test vector, $HW_{reference}$, and n.
if Algorithm 1 outputs 'Pass' **then**
  Output 'No faults are detected'
else
  Output 'Fault is detected'

Algorithm 2 can be used with the existing fault detection models. As an example, let us consider the JJ-based stuck-at fault detection model for SFQ logic [9]. The stuck-at superconductive (SC) state fault is inserted in AND gate of RSFQ 4-to-2 priority encoder circuit. According to the fault model proposed in [9], this faulty AND gate should output the logical "1" when the inputs are $\{\text{In}_1, \text{In}_2\} = \{1, 1\}$ and $\{0, 1\}$. By using the same test signal location as in Fig. 4, Algorithm 2 is executed to detect the fault. The simulation results are shown in Fig. 8. As can be observed from this figure, $|\Delta\text{HW}|$ is nonzero at around 0.4, 1.2, 2.0, 2.8, and 3.6 ns, which coincides with incorrect switching of the AND gate (when the $\{\text{In}_1, \text{In}_2\} = \{0, 1\}$). It should be noted that the switching of other test signals A and C does not affect the fault detection, which is ensured by the modified (i.e., repeated) test vector. Therefore, the proposed BIST methodology does not degrade the coverage of the existing fault detection models, such as in [9].

Besides the fault detection, another important aspect is identifying the fault location. Since all SFQ-to-dc converters are connected to a common bias voltage $V_{B,\text{test}}$, it is difficult to identify the specific logic gate, where the fault is located. By analyzing the changes in HW trace at the certain time instances, it is, however, possible to localize some faults. For instance, let us consider the same example as in Section III-B

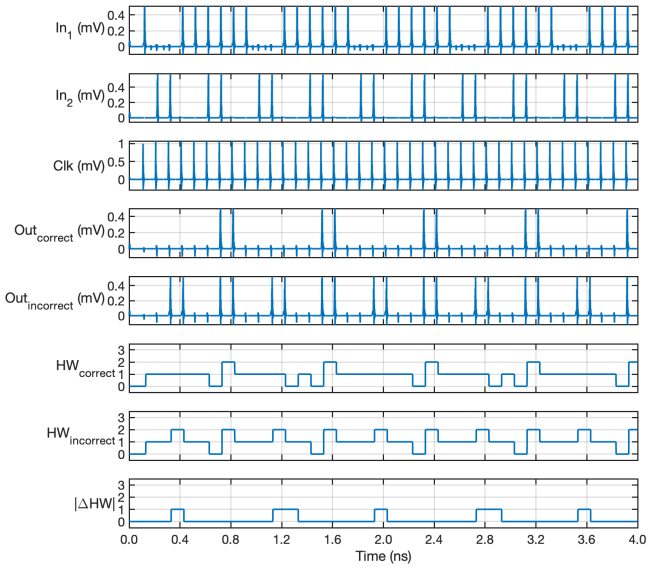

Fig. 8. Fault detection with the proposed BIST methodology. The stuck-at SC fault is inserted in J_{12} of AND gate (see notation in [25]) in RSFQ 4-to-2 priority encoder. Incorrect subscript corresponds to the circuit with fault. $|\Delta\text{HW}| = |\text{HW}_{\text{correct}} - \text{HW}_{\text{incorrect}}|$.

(Fig. 6). By carefully analyzing the correct operation in Fig. 5, it can be observed that the HW values between 0.13 and 0.43 ns only depend on the test signal A. When the fault is located before A, the HW trace might be incorrect during this time interval, as shown in the second subplot of Fig. 6 (i.e., open circuit at A).

By comparing the third subplot of Fig. 6 with the correct operation, it can be observed that the HW trace is the same between 0.13 and 0.53 ns. After 0.53 ns, the HW trace is no longer correct. From Fig. 5, $V_{J8,B}$ starts switching at around 0.53 ns. Therefore, the drop of HW value from 2 to 1 at this time instance signifies the fault before the test signal B (in our case, open circuit at B). Using a similar reasoning, the location of open circuit at C can be determined by comparing the fourth subplot of Fig. 6 with the correct operation. In this case, the difference starts at 0.43 ns, which is the same time when $V_{J8,C}$ starts switching in Fig. 5. Therefore, by carefully examining the HW trace, it is possible to identify the location of faults in this case study. However, in more complex SFQ circuits, the proposed BIST methodology might not precisely locate the circuit faults. For example, the incorrect operation could be undetected if a pair of SFQ-to-dc converters incorrectly switch in a complementary manner at the same instance of time. Nevertheless, due to the toggled/latched switching of SFQ-to-dc converter, its output voltage state has a memory effect. As a result, the error can propagate through subsequent clock cycles and might be detected in the recorded HW trace. Further research is necessary to identify the optimal test signal readout insertion and generalized algorithm that maximizes the probability of identifying the fault locations. In addition, more than one $V_{B,\text{test}}$ voltage source could be used to power SFQ-to-dc converters.

Due to the superconducting nature, SFQ circuits may operate incorrectly due to the trapped flux, which is caused by the stray magnetic field. This phenomenon can present even in

the perfectly fabricated (i.e., defect-free) chips. The proposed BIST methodology can be effectively used to detect this type of fault by using Algorithm 1. For instance, if Algorithm 1 outputs "fail," the chip should be defluxed (e.g., increasing the ambient temperature above the critical value, where the material transitions from superconducting to resistive state).

D. Discussion

The proposed test signal readout using the SFQ-to-dc converters (Fig. 3) is classified as BIST for several reasons that are listed below.

1) According to [18], a BIST can allow testing of circuits that does not have direct connections to external pins. In the proposed BIST methodology, since SFQ-to-dc converters have a floating output, the only connection to an external pin is the bias voltage $V_{B,\text{test}}$, which can also be merged with the main bias $V_{B,\text{main}}$.
2) Since the SFQ-to-dc converter is switching in a toggling/latching manner, its output voltage state has a memory effect. In particular, at any given time instance, the current state (high or low) depends on the previous state. Therefore, the failure at one time instance can propagate to the subsequent measurements. Such failure propagation has been discussed in the previous section (Fig. 6). By applying a sequence of input test vectors and extracting a single HW trace, it is possible to concurrently test and identify/localize faults. This feature is one of the key components of BIST circuits [18].
3) The BIST architecture consists of a signal analyzer that receives test signals, compares with the expected/correct data, and generates pass/fail information (see [18, Fig. 3.20]). Due to the side-channel leakage mechanism, the proposed BIST methodology does not require a specific SFQ comparator. Alternatively, the information about the test signals is naturally evaluated in the form of a bias current variations (HW information) that can be conveniently and efficiently compared by a test engineer.

IV. Comparison of the Proposed BIST Methodology With Conventional Shift Register-Based Readout

The proposed BIST methodology is particularly useful when the number of pins (input, output, and bias) is limited. In this section, the proposed BIST design is compared with a shift register-based readout circuitry. The shift register-based readout circuit is a conventional approach to reduce the number of pinouts (i.e., output pins) used for testing [7]. The shift registers are used to convert a parallel input bit array into a serial format. Due to the simple design of a register cell [i.e., D flip-flop (DFF)] in SFQ technology, the shift register-based readout can provide lower power consumption and smaller layout area as compared to, e.g., a multiplexer-based readout. A block diagram of the test signal readout using shift registers is shown in Fig. 9. This readout circuit consists of SFQ splitters, DFFs, AND gates, and SFQ mergers. The *enable* signal is applied to load the test signals into storage loops of DFFs. The clock *clk* signal is set to the desired readout frequency and is limited by the testing equipment constraints.

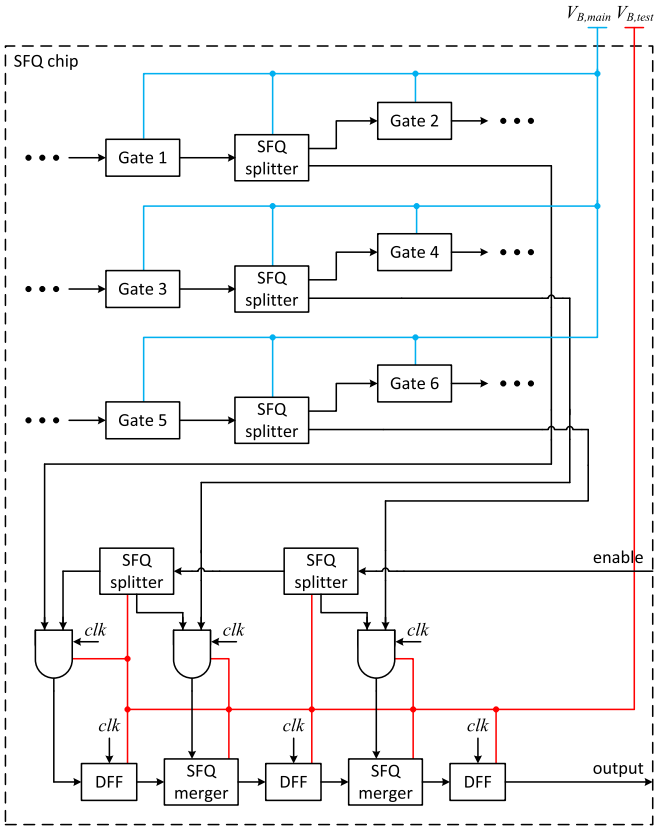

Fig. 9. Block diagram of the test signal readout using the shift registers. The main and test bias networks are shown for RSFQ logic style. The clock signals (*clk*) are only shown for DFFs and AND gates.

A. Power Consumption

The static power consumption, which is supplied by $V_{B,\text{test}}$ (see Figs. 3 and 9) of the proposed BIST (P_{BIST}) and the shift register-based (P_{SR}) designs can be expressed as follows:

$$P_{\text{BIST}} = N P_{\text{SFQ-to-dc}} \tag{1}$$

$$P_{\text{SR}} = N(P_{\text{DFF}} + P_{\text{AND}}) + (N-1)\left(P_{\text{mer}} + P_{\text{spl}}\right) \tag{2}$$

where N is the total number of test signals and P_i is the power consumption of circuit i. Note that the power consumption of the SFQ splitter, which is located between SFQ gates, is not included, since it is connected to $V_{B,\text{main}}$ in both designs. By using (1) and (2), the static power consumption of the two designs is plotted in Fig. 10. The power consumption data are calculated for the SuperTools/ColdFlux RSFQ cell library [25]. As depicted in Fig. 10, the proposed BIST design provides approximately 79% lower static power consumption for $N \geq 23$ as compared to the shift register-based design. In addition, (2) does not account for the power consumption of the clock distribution network (for DFFs and AND gates in Fig. 9), which would make the difference even larger.

B. Layout Area

The layout area requirement for the proposed BIST (A_{BIST}) and the shift register-based (A_{SR}) designs can, respectively,

be written as follows:

$$A_{\text{BIST}} = N\left(A_{\text{SFQ-to-dc}} + A_{\text{spl}}\right) \tag{3}$$

$$A_{\text{SR}} = N(A_{\text{DFF}} + A_{\text{AND}}) + (N-1)A_{\text{mer}} + (2N-1)A_{\text{spl}} \tag{4}$$

where A_i is the cell area of circuit i, which is taken from the layouts of SuperTools/ColdFlux RSFQ cell library [25]. By using (3) and (4), the total layout areas of two designs are compared in Fig. 10. Accordingly, the layout area of the proposed BIST design is roughly 65% lower when $N \geq 21$ as compared to the shift register-based design. The comparison does not include the layout area of bias, clock, and signal lines. However, one can argue that the proposed BIST design has simpler wire routing (see Figs. 3 and 9), resulting in even greater area improvement as compared to the shift register-based design.

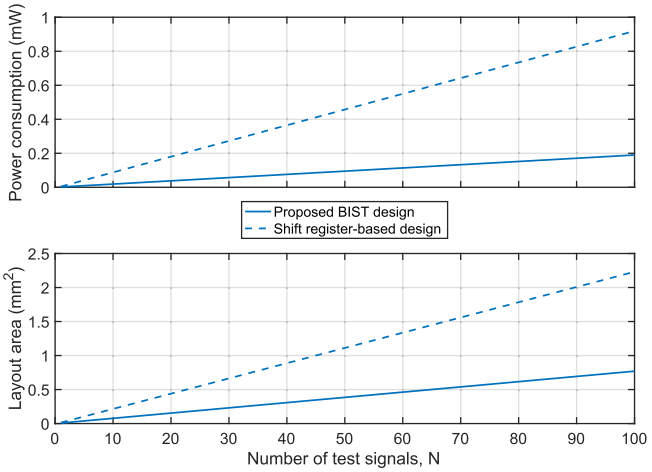

Fig. 10. Comparison of the static power consumption and layout area of the proposed BIST and shift register-based test signal readout systems.

C. Short Circuits

In the shift register-based design, the output signals of SFQ splitters should be routed to AND gates, as shown in Fig. 9. If the selected test signals are located deep inside the SFQ chip, the probability of crossing of these wires with adjacent metal layers becomes higher. As a result, the probability of short circuits between these layers is higher (i.e., resulting in the lower yield) as compared to the proposed BIST design, where SFQ-to-dc converters can be placed in close proximity to the output signals of SFQ splitters (Fig. 3).

D. Number of Pins

To implement a test signal readout, the shift register-based design requires a minimum of three pins (one for bias voltage $V_{B,\text{test}}$, one for *enable* signal, and one for *output* signal, as shown in Fig. 9). Since the proposed BIST design does not utilize the direct measurement of the output of SFQ-to-dc converters, this design needs only one pin for the bias voltage $V_{B,\text{test}}$. The readout of $I_{B,\text{test}}$ does not require a separate pin and can be extracted by measuring the voltage drop on a loading resistor connected in series to the bias pin as has been implemented in *Octopux* testing setup [31]. Furthermore, the absence of an output pin eliminates the need for an SFQ-to-CMOS converter/amplifier and coaxial cables to transmit output signals to room temperature, as required in the shift register-based design. This means that the proposed BIST design generates less heat and dissipates less power between thermal zones of the cryostat.

E. Clock Distribution Network

Each DFF and AND gate in a shift register-based design require a clock signal to propagate the information to the output pin, as shown in Fig. 9. Therefore, an additional clock distribution network should be placed and routed for this type of design. Alternatively, the proposed BIST design uses only SFQ-to-dc converters that do not need any clock signals, significantly simplifying the overall circuit design.

F. Testing Time

In the shift register-based design, after the test signals are loaded into the storage loops of DFFs, one needs to wait for N clock cycles for all bits to propagate to the output pin, as shown in Fig. 9. This delay occurs once the *enable* signal is applied. During this time, the *enable* signal cannot be applied, making the testing time to linearly increase with the number of test signals (N). The proposed BIST design allows to monitor the HW measurements in real time. As a result, multiple input test vectors can be loaded back-to-back without requiring any clearing operations (such as in DFFs). In the low-frequency test mode, the proposed BIST design is faster in terms of the testing time than the shift register-based design. However, in the high-frequency test mode (tens of GHz), the proposed BIST methodology may be limited by the measurement equipment constraints, such as data acquisition rate and resolution. This limitation is caused by the requirement to correctly distinguish HW values from the measured bias current. Therefore, a test engineer should carefully select the appropriate testing equipment for the desired high-speed testing with the proposed BIST design.

G. Interpretation of Test Results

Due to the parallel-to-serial conversion property of bit array in the shift register-based design, the information about all test signals (i.e., logical "1" or "0") can be fully recovered. At any given time instance, the proposed BIST methodology can provide only the information about HW of the test signal states. As a result, each individual test signal cannot be precisely categorized to a logical "1" or "0" from the obtained HW information. Although the proposed BIST methodology has several limitations in precisely localizing the circuit faults in complex SFQ circuits as has been discussed in Section III-B, it can be useful in a pass/fail classification during the mass production of chips.

H. Hardware Security

Since the proposed BIST methodology uses side-channel information, it is vulnerable to side-channel attacks (e.g.,

as explained in [19]). The testing circuit can be protected from malicious side-channel attacks by physically disconnecting $V_{B,\text{test}}$ after the testing is complete or using hardware obfuscation techniques, such as SFQ logic locking [30], [36], [37].

V. Conclusion

In this article, a novel BIST methodology for SFQ circuits is proposed. This methodology uses side-channel leakage of SFQ-to-dc converters, where the applied input signals can be identified by measuring variations in the power supply. By inserting SFQ-to-dc converters, the information about test signals can be obtained from the HW trace that is mapped from the recorded bias current waveform. An RSFQ 4-to-2 priority encoder circuit is considered as a case study to demonstrate the proposed BIST methodology. By analyzing the HW traces for correct and incorrect operation, the location of faults (open circuits) has been identified. As compared to conventional shift register-based readout circuits, the proposed BIST design can provide approximately 79% lower static power consumption and 65% lower layout area. In addition, the testing time, interpretation of test results, and hardware security implications of the proposed BIST are discussed.

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