

RFSoc-FPGA Realization of a Code-Multiplexed Digital Receiver (CMDR) Using 1-ADC/Quad-Channel

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ABSTRACT A 4-channel code-multiplexed digital receiver is presented for multiple-input-multiple-output (MIMO) applications targeting 5G millimeter-wave (mm-Wave) communications. The receiver employs a code-multiplexing (CM) topology where multiple channels are encoded with unique orthogonal Walsh-Hadamard codes and multiplexed into a single-channel for digitization. This approach overcomes the bottleneck of hardware complexity, cost, and power consumption in traditional multiplexing topologies by employing a single wideband analog-to-digital converter (ADC) to serve several channels. The article presents an end-to-end testbed to demonstrate the effectiveness of the proposed Code-Multiplexed Digital Receiver (CMDR) that consists of 1) ultrawideband (UWB) tightly-coupled dipole array (TCDA), 2) a custom-designed encoder circuit board (ECB), and 3) a Radio-Frequency System-on-Chip (RFSoc) field-programmable gate array (FPGA) for encoding and decoding. The code sequences were generated at a maximum clock frequency of 400 MHz. Extensive experimental measurements were performed and test results were validated using performance metrics such as normalized mean square error (NMSE) and adjacent channel interference (ACI). Test results showed ACI of >20 dB, NMSE = -24.592 dB and little or no degradation in signal-to-noise ratio (SNR). To the best of our knowledge, this is the highest clock frequency and ACI value for hardware validation of channel multiplexing scheme reported in the literature.

INDEX TERMS RF-SoC, FPGA, RF-sampling DAC, RF-sampling ADC, Digital Beamformer, MIMO systems, Code Domain Multiplexing, Adjacent Channel Interference.

I. INTRODUCTION

Fifth-generation (5G) architecture and future-G wireless systems aim to address the prolific growth of cellular data traffic [1], [2], [3], [4]. Sub-6 GHz and millimeter-wave (30-300) GHz frequencies are preferable due to the wider available bandwidth at these frequency ranges. High data rates at low latencies push the need for multibeam antenna technologies such as multiple-input-multiple-output (MIMO) [5] and adaptive beamforming. MIMO technique

can exploit the capability of hundreds or even thousands of antenna elements in a small physical aperture at high frequencies and account for the associated losses [6]. Therefore, MIMO techniques along with beamforming approaches can provide high gains, and interference mitigation for a robust communication link with greater spectral efficiency. However, there are several technical challenges to overcome in realizing 5G and beyond-5G wireless communication protocols [5].

A major challenge at higher frequencies is the large propagation losses. Beamforming at the transmitter and/or receiver ends can account for the path-loss. Phased arrays [8], [9], such as tightly-coupled dipole arrays (TCDAs) [10], [11] are therefore preferable antenna arrays because of their large array gain and low profile. Notably, traditional analog beamformers (ABF) employ phase shifters at the local oscillator [12] and at the RF chain [13], which increases hardware realization complexity, power consumption and associated costs. Full digital beamforming (DBF) provides greater degrees of freedom and computational capability compared to analog and hybrid-counterparts [14].

However, an added challenge for conventional DBF systems is the need for dedicated analog-to-digital converter (ADC) and digital signal processors (DSP) for every antenna element [15], [16], [17], [18], [19], as shown in Fig. 1(a), requiring N -ADCs for N -antenna system. It is remarked that the number of ADCs employed in the architecture determines the overall size, weight, power consumption and cost (SWaP-C) factor. Additionally, the number of digital input-output (I/O) pins to interface with the DSP increases with the number of RF chains.

A frequency-domain multiplexing is used in [20], where LO and IF are combined to a single cable to reduce interfacing pin counts. But this leads to discarding information while RF combining since traditional single-output phased arrays are multiple-input-single-output (MISO) systems. Hence, the requirement for I/O pins becomes a bottleneck for large number of RF chains.

A reduced hardware can be achieved by multiplexing multiple signals from different antenna elements into a single shared-path and digitize with a single wideband ADC. The major multiplexing techniques include time-division multiplexing (TDM) [21], frequency-division multiplexing (FDM) [22], [23] and code-division multiplexing (CDM) [24]. TDM scheme involves switching the antenna elements using a fast-enough analog RF-switch. The fast switching rate requirement results in non-linearities in the signal. In FDM, several challenges need to be accounted for such as phase synchronization among multiple LOs, extraction of phase offset corresponding to each element, and increased hardware complexity. Hybrid multiplexing involving both FDM and CDM approaches in multi-antenna systems can overcome the aforementioned impediments.

For MIMO systems [25], ADC power consumption is a significant concern in determining the SWaP-C factor. Although digital circuit process flow follows Moore's law, ADC power consumption merely reduced by a factor of 10 in the past decade. Therefore, this article proposed a novel receiver architecture for MIMO systems with special emphasis on reducing ADC count utilizing FDM and CDM schemes. This approach pushes most of the signal processing tasks to the high-speed DSPs reducing significant interfacing pin counts between the analog and digital components.

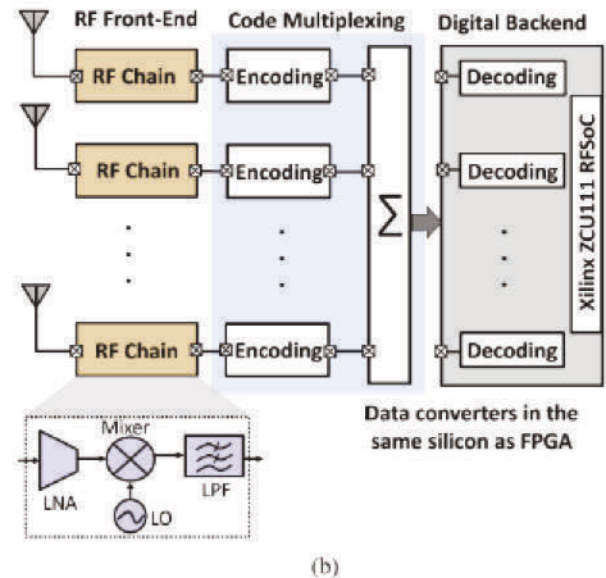
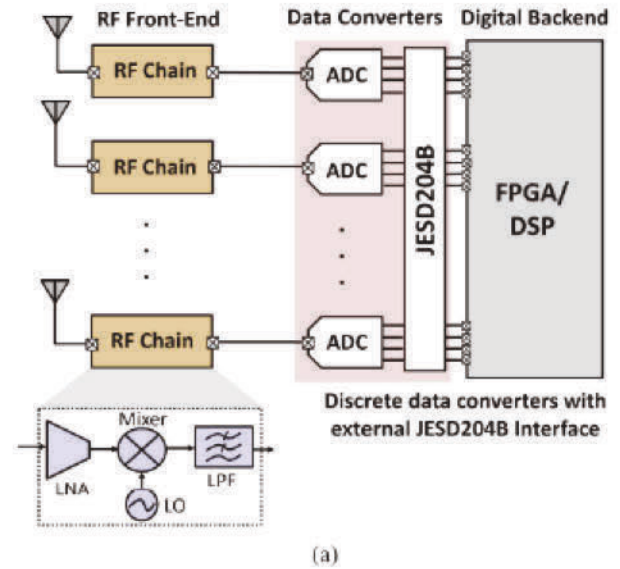


FIGURE 1. (a) Traditional digital beamforming application leads to multiple power-hungry ADC in each branch leading to large power consumption and interfacing challenges to the baseband processor. (b) Proposed CDMR architecture multiplex multiple elements into a single-path employing 1-ADC/quad channel.

There is a significant growth in the mixed-signal RF field with the integration of multiple ADCs with programmable logic (PL) on the same chip [26], [27]. For instance, RF-enabled field-programmable gate array (FPGA), such as the Xilinx RF-SoC support the combined realization of programmable digital fabrics with up to 16 high-speed ADCs and DACs on the same chip [28], [29], [30], [31] at a bandwidth of more than 1 GHz per channel [21]. Therefore, we exploit the integration capability of Xilinx's RF-SoC ADCs to multiplex N -channels into a single RF-ADC.

In this article, a novel code-multiplexed digital receiver (CMDR) front-end is presented, as shown in Fig. 1(b). This

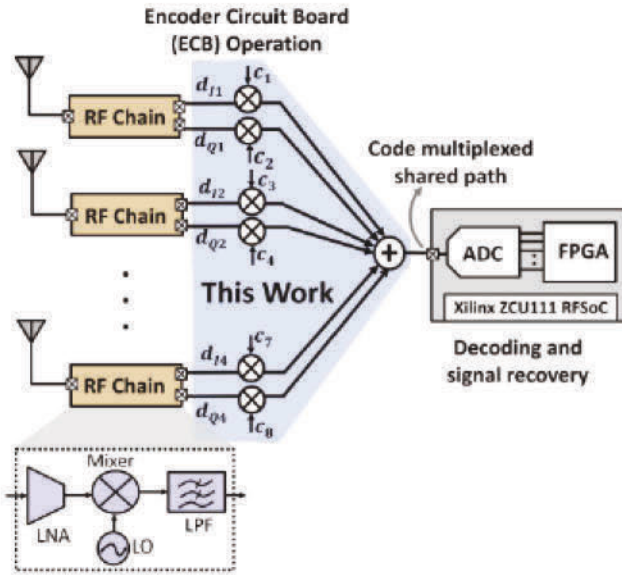


FIGURE 2. Code Multiplexing (CM) of downconverted (IF) signals using orthogonal WH codes.

enables combining multiple channels into a single shared-path and digitization using a single-ADC. This work extends our previously published work [32] that shows only two channel implementation with continuous wave (CW) tone measurements. The major contributions and novelties of this article include:

- 1) An extended hardware implementation of 4-channels to analyze the effects on power consumption.
- 2) An increased WH code length of $L_c = 64$ for better cross-correlation performance
- 3) In addition to CW tones, test measurements include modulated waveforms to investigate the effect of higher modulation order on the recovered signal quality
- 4) Normalized mean square error (NMSE) performance metric added to quantify the quality of the recovered signals in time-domain.
- 5) Matched filtering at the digital baseband to achieve adjacent channel interference (ACI) suppression in the combined shared-path.

As shown in Fig. 2, the I and Q signals are encoded with orthogonal codes and multiplexed to a single shared-path at the intermediate frequency (IF) interface. The primary objective is to extract individual channel at the digital baseband with the same code sets used for encoding. Key properties of the selected codes include autocorrelation and cross correlation, code length, and the computational complexity of generating the codes in FPGA. Ideally, the codes are expected to provide an impulse response for autocorrelation and zero cross correlation. However, in actual hardware implementation, these properties shall show deviation from the ideal behavior due to hardware nonidealities.

Second objective of this work is to minimize the ACI in a multiplexing technique (particularly code-multiplexing

in this case) which has been less explored in terms of hardware realization with off-the-shelf components. This approach allows ACI reduction in a MIMO setup using digital phase/amplitude offset calibration at the digital end. The latter is important for multiple-channel communication links as such systems become interference-limited rather than noise-limited. It is remarked that, since analog signals (received) are encoded with digital codes, input-output (I/O) port conversion stages were used to interface the two data types. Notably, spreading code impairments due to these additional hardware constraints may increase ACI particularly at higher data rates. Overall, the proposed architecture validates the feasibility of code-multiplexing multiple channels to a shared path and employ single-ADC for digitization instead of dedicated ADC/channel in traditional MIMO systems. Notably, this is the first-ever demonstration of such code-multiplexed receiver architecture to achieve high isolation at 400 MHz clock frequency.

The performance of the proposed approach is compared with state-of-the-art schemes in Table 1. This article implemented code-multiplexing approach in a reconfigurable chip (RFSoc FPGA in this work) instead of custom-designed integrated circuits, such as application specific integrated circuits (ASIC) [33], [34]. The number of elements is also extended to four, demonstrating a simplified approach of MIMO systems with reduced ADC counts.

The article is organized as follows. Different multiplexing techniques are discussed in Section II. Section III gives a description of the proposed receiver architecture and its key parameters. The design and operation of the circuit at the receiver system is given in Section IV. Next, section V provides digital baseband signal processing and signal recovery procedures. Section VI presents measurements of the complete receiver system.

II. COMPARISON OF DIFFERENT MULTIPLEXING SCHEMES

A. TIME-DIVISION MULTIPLEXING (TDM)

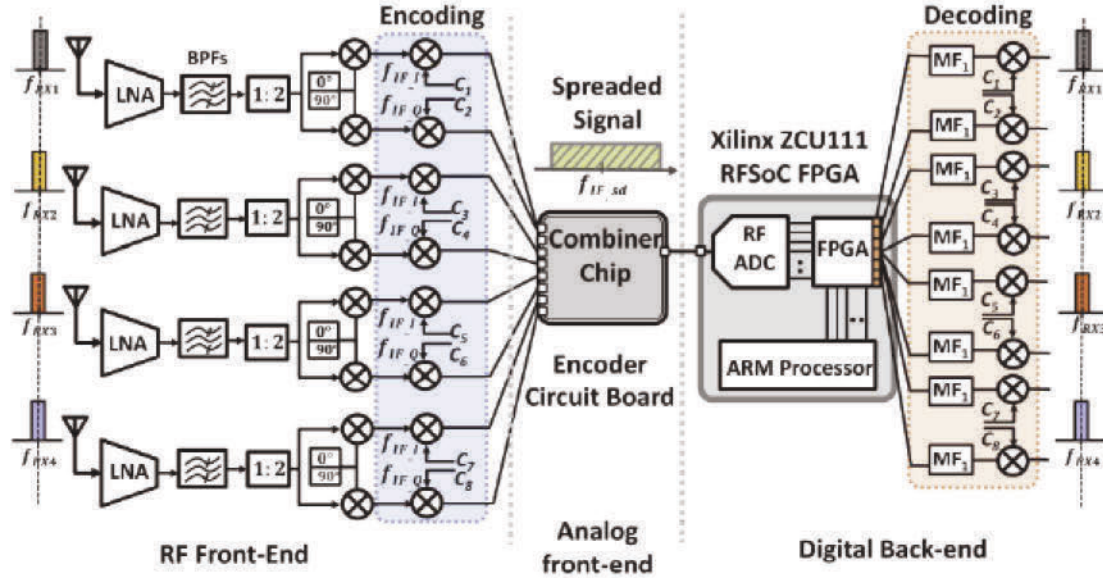
In TDM, individual antenna elements are switched to a single RF channel for a certain time period using analog switches. Synchronization mismatch between multiplexing and demultiplexing leads to clock jitter especially with high switching rate. Another challenge is the SNR degradation due to signal reception for only $1/N$ time duration, for an N -antenna system. This leads to N -fold reduction in signal energy. FDM and CDM-based systems address these issues.

B. FREQUENCY-DIVISION MULTIPLEXING (FDM)

Despite having the advantage of using 1-ADC per shared group of channels, this scheme still requires N radio-frequency front-ends (RF-FEs) mounting LNAs, LOs, mixers and filters. Generating multiple closely offset LOs is complicated and may result in injection locking. Additionally, any adjacent channel interferer would corrupt the desired channel signal quality. Finally, practical nonideal filtering

TABLE 1. Performance Comparison With the State-of-the-Art Multi-Antenna Receiver Architecture With Multiplexing Schemes

Ref.	Function	Tech.	Freq.(GHz)	No.of Elem.	Multiplexing	Isolation(dB)
[25]	Nulling	45nm SOI	27-41	4	X	X
[14]	Nulling	65nm	27-29.75	4	X	X
[33]	MIMO	180nm	5.4	2	Freq.Domain	X
[34]	MIMO	180nm	5.25	2	Code Domain	X
This Work	MIMO	RFSoc FPGA	2.14	4	Code Domain	20


FIGURE 3. Proposed code-multiplexed digital beamformer with shared-IF path.

necessitates guard frequency intervals between adjacent spectra, consequently increasing the total occupied bandwidth. On the contrary, CDM approach can address this spectrum inefficiency.

C. CODE DIVISION MULTIPLEXING

Unlike the TDM and FDM schemes, this approach allows the desired signal and interferer spectra to overlap. Same set of codes are used to encode and decode individual channels. The desired signal can be easily recovered even in the presence of strong adjacent channel interferer (ACI). Due to overlapping spectra, data signal is not truncated in time domain, hence no loss in SNR is incurred.

III. PROPOSED CODE-MULTIPLEXED DIGITAL RECEIVER (CMDR)

This section presents the receiver architecture, orthogonal coding scheme, hardware components, and the digital baseband processing unit.

A. RECEIVER ARCHITECTURE DESIGN

The proposed receiver architecture for code-multiplexing is shown in Fig. 3 with the detailed mechanism of encoding and decoding. Four uncorrelated signals are initially captured by the four antenna elements in the array. Although current

test bed considers a 4-channel MIMO configuration, the presented hardware set-up can be extended to any multi-channel application in general. This is because the CM is being performed at an intermediate frequency (IF). Specifically, the signals received by the antenna in each channel are amplified using low-noise amplifiers (LNAs). Then the signals are passed through bandpass filters (BPFs) to reject out-of-band frequency components. This step also prevents leakage from the local oscillator (LO) to the downconverting module. The individual signals are then downconverted to an IF level using RF-FE.

The baseband signal from each signal path is then encoded with orthogonal codes generated by the field programmable gate array (FPGA) module, increasing the baseband signal bandwidth. The spread signal (encoded) bandwidth is a multiple of the original baseband signal i.e., $BW_{spread} = L_c \times BW_{baseband}$, where L_c is the code length and $BW_{baseband}$ is the bandwidth of the baseband signal. The spread signals are then combined using the combiner chip on the fabricated encoder board. Selection of the codes, fed to the encoder board for the encoding/decoding process, is a critical aspect of this work.

B. ORTHOGONAL PROPERTIES OF CODE SEQUENCES

Different classifications of spreading codes can be found in the literature including pseudo-random noise (PN) codes,

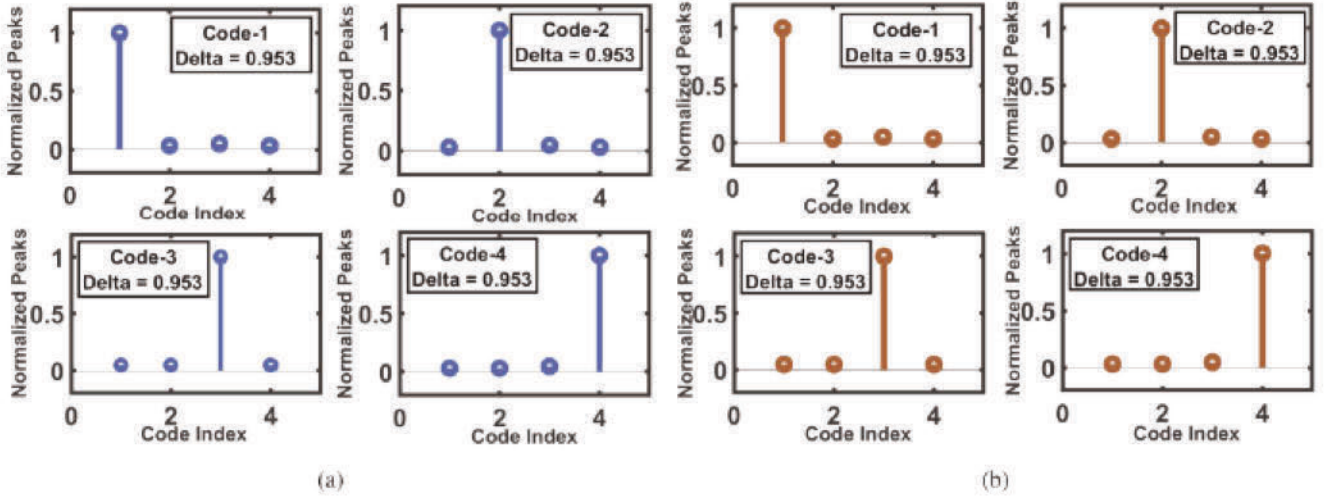


FIGURE 4. Orthogonal properties of the WH codes showing (a) cross-correlation and (b) auto-correlation of the WH codes.

maximal-length codes (ML), Kasami codes (KC) and Gold codes (GC) [35]. In [24], it has been proved with simulations that the codes employed should be robust to perform code-multiplexing without SNR degradation. Robust codes consist of the following properties: 1) code sequences are made up of bit strings, 2) autocorrelation value of “1” (ideally), 3) fully orthogonal, i.e., a cross-correlation value of “0” ideally, and 4) equal number of “1” and “0” to avoid DC component. A detailed analysis of the performance superiority of WH codes over other codes can be found in [24], [36], [37], [38]. The mentioned works report minimal degradation in SNR due to code-multiplexing. In [36], theoretical study and simulations were performed with synchronous WH codes and asynchronous Gold codes (GC). Performance metrics such as bit error rate (BER) lead to the comparison between these two code pairs using BPSK modulation. Among these code sets, Walsh-Hadamard (WH) code proves to be the best candidate for CMDR since they lead to negligible SNR degradation according to the previous studies in [24], [36], [37], [38].

WH sequences of length N are obtained from the rows of an $N \times N$ Hadamard matrix H_N . For this work, a WH code length of 64 was chosen and the codes were generated by the matrix

$$H_{2N} = \begin{bmatrix} H_N & H_N \\ H_N & -H_N \end{bmatrix} \quad (1)$$

where $2N$ refers to the code length and provides the maximum number of possible orthogonal codes. The total number of orthogonal codes are classified into two groups, basis and non-basis codes. Out of these, $1 + \log_2(2N)$ are denoted as basis codes and the rest as non-basis codes. Hence, in this work, number of basis codes = $1 + \log_2(64) = 1 + \log_2(2^6) = 7$.

The orthogonality of the employed codes at the desired clock frequency is a key feature of the approach. Fig. 4 shows the orthogonality (in terms of cross-correlation and

autocorrelation) of the optimally chosen WH code sequences. Indeed, the code correlation process should yield a single narrow and sharp auto-correlation peak. An accurate extraction of the decoded signal is ensured only when the codes are synchronized. Therefore, it is critical to ensure excellent synchronization process. To achieve perfect synchronization, we must ensure that the chosen code sequence provides minimal cross-correlations by accounting for the small time shifts introduced due to the hardware non-linearities. Spreading codes with minimum cross-correlation values leads to minimum SNR degradation [25].

C. EFFECT OF SPREADING CODES ON SYSTEM PERFORMANCE

In comparison to the conventional code-division multiplexing (CDM) technique, our proposed scheme performs encoding and decoding operations both within the receiver chain. So, both the signal and noise in each path shall spread simultaneously. Both the encoded signal and the noise signal from all the paths are combined into a single shared-path. Therefore, a system evaluation is performed in the following subsections with two different scenarios: 1) proposed 4-channels and 2) increased number of channels (> 4 channels).

1) SYSTEM EVALUATION FOR 4-CHANNELS

At the digital back-end, the spread signals are decoded by multiplying them with the same code sequence. So, at the k th signal path, the decoded signal is given by:

$$s_{dd,k}(t) = \underbrace{s_{d,k}(t)c_k(t)c_k(t)}_{\text{Desired Signal}} + \underbrace{n_{d,k}(t)c_k(t)c_k(t)}_{\text{Noise at the } k_{th} \text{ path}} + \sum_{i=1, i \neq k}^{N_c} \left(\underbrace{s_{d,i}(t)c_i(t)c_k(t)}_{\text{Interfering Signals}} + \underbrace{n_{d,i}(t)c_i(t)c_k(t)}_{\text{Interfering channel noise}} \right) \quad (2)$$

where $s_{dd,k}(t)$, $s_{d,k}(t)$ refer to decoded signal and desired signal at the k_{th} desired path, and $c_k(t)$, $c_i(t)$ refer to the corresponding codes at the desired and interfering paths respectively. In the above, $n_{d,k}(t)$ and $n_{d,i}(t)$ represent additive white Gaussian noise at the desired and interfering paths, respectively. k refers to the desired signal path and $i = 1, 2, 3, \dots, N_c$ representing all the interfering signal paths. The first two terms refer to decoded signal in the desired channel and its associated noise from the k th signal path respectively. The later two terms are the co-channel and inter-channel interference signals.

When the code sequences are synchronized, the orthogonal properties of the codes must yield

$$\int_0^{T_d} c_k(t) \cdot c_k(t) dt = 1 \quad (3a)$$

$$\int_0^{T_d} c_k(t) \cdot c_i(t) dt = 0 \quad (3b)$$

where, c_k and c_i are the code sequences in the desired and interfering paths respectively, for $i \neq k$.

Eventually, based on (3a) and (3b), (2) reduces to

$$s_{dd,k}(t) = \hat{s}_{d,k}(t) + \hat{n}_{d,k}(t) \quad (4)$$

Finally, the desired signal is decoded with the associated noise in the receiver chain. A step-by-step derivation of signal model from (2) to (4) can be found in [28].

2) SYSTEM EVALUATION FOR >4 CHANNELS

The effect on achieving ACI suppression by incorporating more number of channels must be addressed to evaluate the scalability of the system. It is important to mention that with increased number of channels in such a code-multiplexing technique, the system becomes interference-limited rather than noise-limited due to increase in power level from the interfering channels. Instead of SNR, the system has to be evaluated with the quantification metric signal-to-interference plus noise ratio (SINR).

Hence, for our system, the SINR at the output of the matched filter (that is after decoding the desired channel) is given by:

$$SINR_{CMDR} = \frac{P'_{d,k}}{\sum_{i=1, i \neq k}^{N_c} (P'_{d,k} + N'_{d,i}) + N'_{d,k}} \quad (5)$$

where, $P'_{d,k}$ and $N'_{d,k}$ are the decorrelated signal ($s'_{d,k}$) and noise signal ($n'_{d,k}$) powers through the k_{th} path, respectively. $P'_{d,i}$ and $N'_{d,i}$ represent the inter-channel signal [$\sum_{i=1, i \neq k}^{N_c} (P'_{d,k})$] and noise [$\sum_{i=1, i \neq k}^{N_c} (N'_{d,i})$] powers due to the cross-correlation between the spreading codes, respectively. This implies that, as the number of channel (signal paths) increases, signals and noise from the additional paths shall leak more and more into the desired (k_{th}) path. Notably, $N'_{d,i}$ in (5) shall increase and contribute to the degradation in SINR value. Therefore, it can be concluded that extending the number of channels shall increase the ACI, leading to

SINR degradation and increasing computational complexity of decoding the desired channel from the shared-path. Referring to (9) in the Appendix, effect of increased number of interfering channels on the decoded signal at the k th path can be expressed as:

$$s_{dd,k}(t) = \hat{s}_{d,k}(t) + \hat{n}_{d,k}(t) + \sum_{i=1, i \neq k}^{N_c} \hat{s}_{d,i} + \hat{n}_{d,i} \quad (6)$$

where $\hat{s}_{d,k}(t)$, $\hat{n}_{d,k}(t)$, $\hat{s}_{d,i}(t)$, and $\hat{n}_{d,i}(t)$ represent decoded signal at the desired channel, corresponding noise at the desired channel, interferences from adjacent channels, and corresponding noise contribution from the adjacent channels, respectively.

D. DIGITAL BASEBAND PROCESSING UNIT

A past challenge was the capturing and sampling of large bandwidth signals within the dynamic range of an ADC. However, the recent availability of high-speed ADCs [30] has provided the means to overcome this issue. Specifically, the chosen ADCs have a sampling frequency of more than twice the chip rate, i.e. $2 \times BW_{code}$, satisfying the Nyquist sampling criterion, where BW_{code} = bandwidth of the WH codes. Further, to prevent aliasing from adjacent channel signals, we chose to oversample the received signal [21]. Since multiple channels are combined before digitization, interference and signal leakage from adjacent channels are expected to be the performance determining factor instead of SNR. After digitization by the high-speed ADC, the signals are decorrelated at the digital back-end using matched filters. It is remarked that the orthogonal properties of codes allow for decoding of the received signal path without compromising SNR. After decorrelation, suitable signal processing is performed to recover the desired signal properties. For instance, digital beamforming is realized by digitally applying amplitude weights and suitable phase delays in the signal path. This can be done as a post-processing step to generate several concurrent beams across the desired band. For the following measurements, de-correlation and phase estimation was performed using MATLAB, while FPGA was used for code generation.

IV. HARDWARE REALIZATION OF THE PROPOSED RECEIVER

This section details the hardware components used in the experimental demonstration. Fig. 3 (Section III(A)) gives the architecture for the proposed receiver, including the antenna array elements, encoding concept, encoded signal outcomes, mixed-signal device (ADC) placement, and signal decorrelation at the FPGA.

A. XILINX ZCU111 RFSOC FPGA

The hardware used in this demonstration as the DSP is one of the first generation of RF-SoC devices from Xilinx [30], [31]. Specifically, the XCZU28DR chip incorporates eight 12-bit RF-ADCs with a sampling rate of 4.096 GSPS, and eight

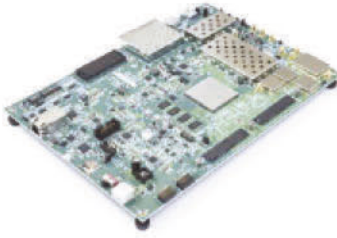


FIGURE 5. Zynq UltraScale+ RFSoC ZCU111 FPGA evaluation board.

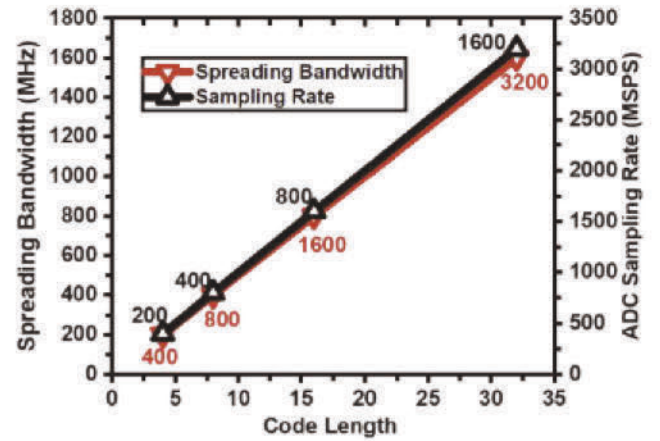
TABLE 2. Device Contents of ZCU111 FPGA Fabric

Component	Value
RF-ADC (12-bit, 4.096 GSPS)	8
RF-DAC (14-bit, 6.554 GSPS)	8
System Logic Cells	930K
33Gbps Transceivers	16
Subcarrier Spacing	15 KHz
Maximum I/O pins	371
Memory	60.5 Mb
DSP slices	4,272

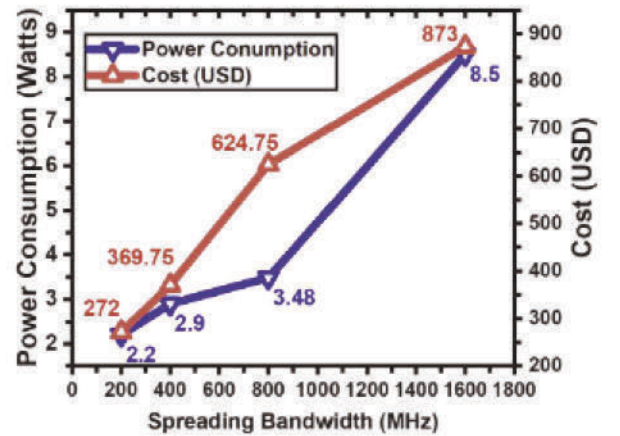
14-bit RF-DACs and ARM-based processor system in a single platform. Also, the chip has a large number of logic cells, DSP slices and registers, as well as 16 32.75 Gb/s transceivers [39]. A photo of this baseband unit is depicted in Fig. 5 and Table 2 lists the contents of the FPGA fabric. Signal processing and conditioning performed by the FPGA includes: 1) on-board clock generation; 2) WH code generation; 3) decoding the encoded signals; and 4) recovering the received signal information (phase and amplitude). The FPGA simultaneously generates the required clocks for all digital modules using an on-board reference clock to minimize phase jitter and phase mismatches. A detailed resource utilization report along with power consumption and chip area usage is included in Section IV.

One of the main motivations of using RF-SoC data converters is to minimize power consumption and cost of the overall system implementation. Fig. 6(a) depicts the direct relationship between the signal bandwidth and sampling rate requirements of discrete data converters. The plotted data has been accumulated from commercial off-the-shelf (COTS) components. Notably, with the increase in WH code length, bandwidth of the multiplexed signal (spreading bandwidth) increases. Hence, required ADC sampling rate increases proportionally. Associated cost and power consumption by the discrete converters increases accordingly which can be deduced from Fig. 6(b).

Discrete data-converter requires JESD204 IP interface for FPGA communication. Digitization using discrete data converters involves both power consumption of the data converters and JESD204 transceiver interface protocol. Fig. 7(a) shows the high power consumption of transferring data between radio-frequency front-end (RFFE) and digital front-end (DFE). Minimum 1 W of power per four lanes is required for the I/O pins in a quad transceiver on the SoC devices from



(a) Relation between bandwidth and ADC sampling rate requirements with respect to the WH code length



(b) Power and cost analysis of ADCs with respect to the spreading bandwidth of the multiplexed signal

FIGURE 6. Estimation of power consumption and costs per unit of discrete data converters. Increase in code length and spreading bandwidth, SWaP-C requirements increases proportionally.

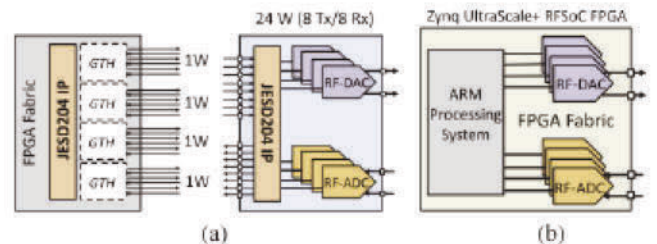


FIGURE 7. Effectiveness of using RF-sampling data converters for interfacing RF front-end (RFFE) with digital front-end (DFE) using (a) JESD204 IP protocol and (b) without using JESD204 IP.

Xilinx [22], [23]. On the contrary, direct RF-sampling data converters [37], [38] push most of the analog/RF signal processing to the digital domain providing smaller footprint, less power consumption and software programmability as shown in Fig. 7(b). Hence, this work leverages RF-ADC in Xilinx

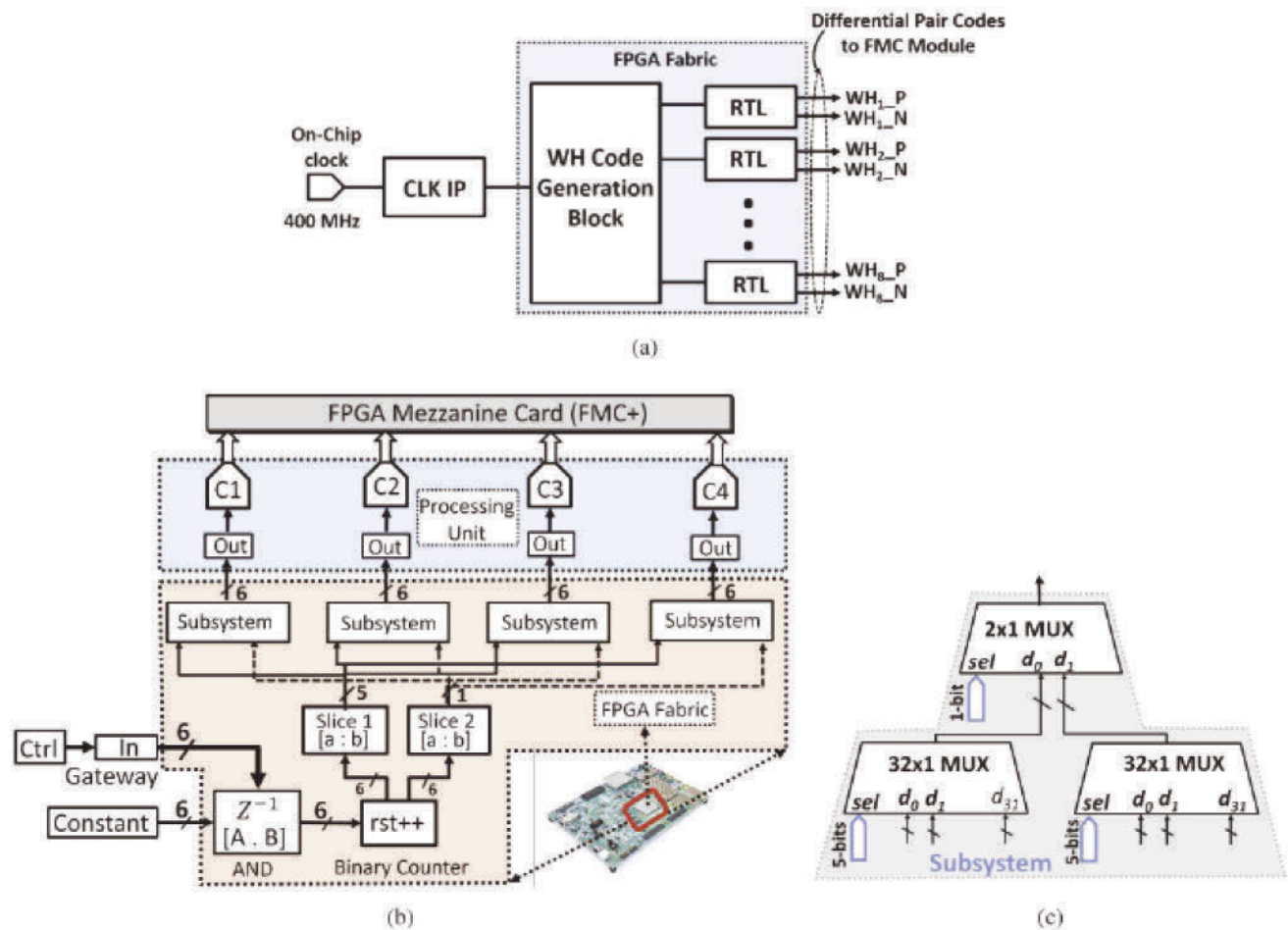


FIGURE 8. (a) Top level digital circuit diagram for generating the WH codes, (b) detailed circuitry inside the WH code generation block, and (c) inside circuitry of the subsystem in (b). The circuit was designed using System Generator and later bitstream was generated to program the xczu28DR FPGA chip for the implementation and synthesis of the code generation circuitry.

ZCU111 RFSoc device, eliminating the need for external I/O interfaces (JESD204). This comes with additional benefits of less number of required clocks to drive the JESD204 interfaces, reduced routing complexity of the clocks on the PCB, and synchronizing the links.

B. DIGITAL CIRCUIT DESIGN FOR WH CODE GENERATION

1) CIRCUIT IMPLEMENTATION ON FPGA FABRIC

The implemented circuit to generate the WH codes is depicted in Fig. 8. Commonly available blocks such as binary counter, slices, multiplexers, and several others are noted. This system diagram and signal flow is designed using System Generator simulation tool. Xilinx System Generator has an add-on library *Xilinx blockset* to replicate fixed-point behavior in Simulink simulation with the same bit-accurate behavior in FPGA. The Xilinx toolbox allows us to transport the design in Fig. 8 for a hardware/software co-simulation and generate bitstream for synthesizing in the FPGA fabric. The design is implemented and synthesized using Vivado IDE software. As can be seen in the circuit diagram (Fig. 8), the control (Ctrl) block at the input defines the data

type in the simulation environment. The gateway block converts the simulink data type, boolean in this case, to Xilinx fixed/floating point data type. Finally, the binary data from the constant block generates the bits that ultimately form the code sequence.

A logical block performs digital logic operations between the data bits and the control bits. The 6-bits logical output is then sliced into two different configurations, 5-bits and 1-bit, both of which act as select pins for the MUXs inside the subsystem blocks. Slicing of the bits is necessary because of availability of maximum 32-bit multiplexer (MUX) in System Generator environment. Finally, gateway blocks convert the fixed/floating point input data types into fixed-point in this case, compatible with Simulink. It is remarked that only the blocks between the "Gateway In" and "Gateway Out" are synthesized in the FPGA fabric which is shown in the shaded region.

2) RESOURCE UTILIZATION AND POWER CONSUMPTION

Hardware resource utilization by the synthesis of the digital circuit on the RF-SoC listed in Table 3. It is clearly seen that

TABLE 3. FPGA Resource Utilization Results (XCZU28DR) for the Synthesized Design in Fig. 8

Resource	Available	Utilization	Utilization %
LUTs	425280	3	<1
Flip-Flops	850560	12	<1
I/O pins	347	20	5.76
BUFG	696	2	0.29

TABLE 4. Custom-Designed Encoder Circuit Board (ECB) Components

Component	Part Number	Frequency Range
Multiplier Chip	ADL9351	0-2 GHz
RF Transformer	TC1-1-13M+	4.5-3000 MHz
Power Combiner	JCPS-8-10+	5-1000 MHz

the implemented design has efficient utilization of the FPGA resources, a major advantage of the proposed design. Notably, less than 1% of the resources are used, except for the I/O pins (6%).

C. FPGA CLOCK AND CODE GENERATION

Two major tasks were performed by the FPGA: encoding the received waveforms and decoding the recovered digitized signals. Decoding and recovery of the original signal information were implemented by code blocks C1 to C4 as shown in Fig. 8. These code block IPs were programmed using VHDL programming language in Vivado IDE software tool. The recovered signals from each signal path are mapped to their physical location in the antenna array for beamforming.

The converters within a single tile share the clocking and data infrastructure, so the sample rates and latency are fixed. Since we have used only 1 ADC in this experiment, latency is not our primary concern. Each tile in RFSoc has the option to use its own PLL to generate the RF converter sampling clock on-chip. These on-chip RF PLLs help to avoid high frequency sample clocks routing on board.

D. CUSTOM DESIGNED ENCODER CIRCUIT BOARD

The generated codes are then accessed through the FMC pins. An FMC module (FMC Vita 57.1) from HiTech Global was plugged into the FMC pins on the ZCU111 development board. These are then directly subjected to the custom-designed encoder board where the multiplexing operation occurs and is discussed in the following subsections.

Printed circuit board (PCB) layout of the 6-layered encoder board is shown in Fig. 9(a). Layer 1 and layer 6 are used for the analog RF signal traces and digital code signal traces respectively. Power supply source traces for the circuit are assigned to Layer-4 to maintain isolation from noise by the source. This ensures minimum cross-talk between the signal traces and the supply noise sources. The other three layers provide the necessary grounding and robustness of the board to support extensive hardware sources such as coaxial cables. Layer and routing trace thicknesses were carefully chosen to

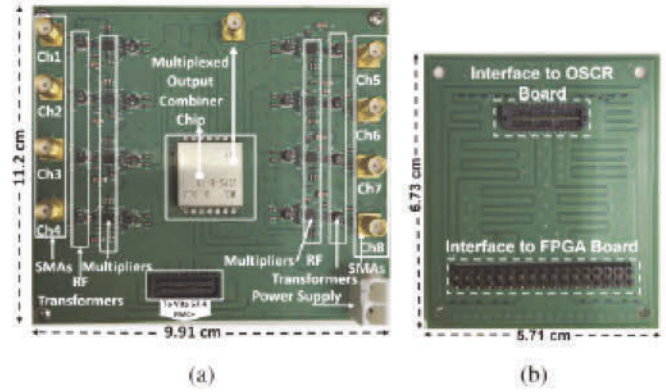


FIGURE 9. Custom-designed and fabricated adapter board showing (a) two sets of pin sockets that connects the encoder circuit board to the FPGA board and (b) differential-pair routing traces to minimize the cross-talk and interference.

maintain a characteristic impedance of 50 Ohm. Table 4 lists all the components mounted on the ECB.

V. MEASUREMENT SETUP

This section gives a detailed description of the CMDR experimental setup to validate the concept. Specifically, we explain the implementation setup and individual hardware components, including the receiver antenna array, encoder board circuit operation, and the digital signal processing within the FPGA.

A. FOUR-CHANNEL RECEIVER HARDWARE SETUP

The experimental setup for evaluating the receiver architecture performance is shown in Fig. 10. The primary objective of this experiment was to minimize adjacent channel interference (ACI) in a MIMO beamforming radio system. The latter is important for multiple-channel communication links as such systems become interference-limited rather than noise-limited. Prior to the experiment, a comprehensive power budget analysis was carried out to ensure that no device operates in the nonlinear region and in a manner to degrade the required SNR level. A simplified block diagram for the measurement setup is shown in Fig. 11. In order to successfully recover the desired signal a minimum SNR is required. Evaluation of the recovered signal quality at the digital baseband and the resulting SNR is elaborated in [28] (Section III).

For the implemented prototype, only off-the-shelf components were used to perform the experiment and generate the RF signals. At the transmitter side, an Agilent vector signal generator was used to generate four CW signals with a transmit power of +10 dBm each. Bandpass filters were also used to prevent possible harmonics from reaching the transmitting horn antenna. A power amplifier (PA) of 38 dB gain was also required at the transmitting side to compensate for space and cable loss.

At the receiver side, an 8×8 ultra-wideband (UWB) antenna array was used. For proof-of-concept demonstration

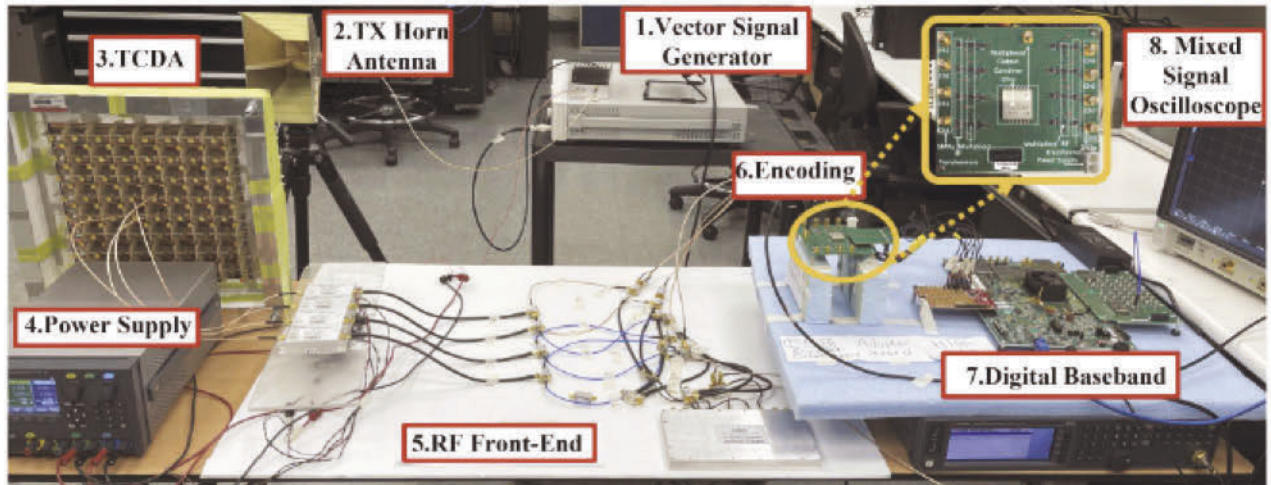


FIGURE 10. Measurement setup of the four-channel hardware prototype of the CMDR system showing (1) vector signal generator as the baseband transmitter signal generator, (2) transmitter horn antenna, (3) receiver antenna array (TCDA), (4) power supply for the LNAs and PA, (5) RF front-end (low-noise amplifiers (LNAs), mixers, bandpass filters (BPFs), signal generator (LO), power splitter), (6) encoder board, (7) Xilinx RFSoc FPGA as the digital baseband processor, and (8) a mixed-signal oscilloscope.

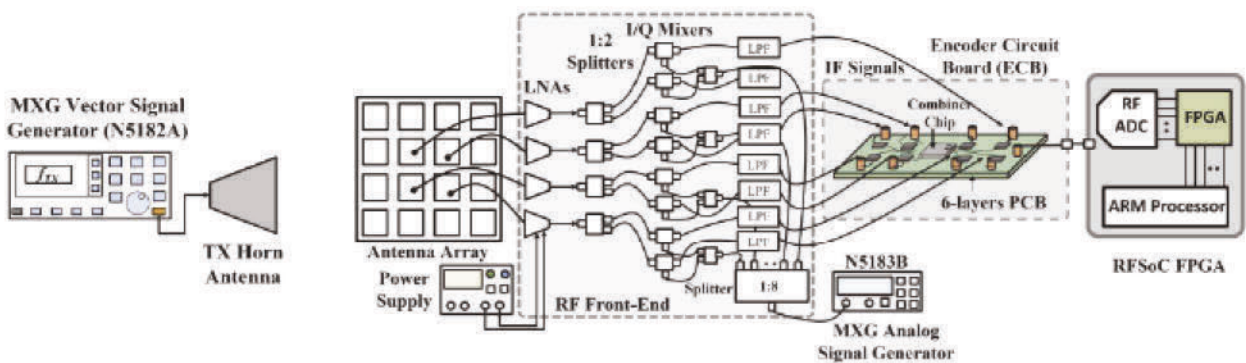


FIGURE 11. Simplified block diagram representation of the measurement setup for measurements and data acquisition.

only 4 center elements of the array were excited. Each of the antenna elements was followed by an LNA to compensate for cable and propagation losses and increase signal strength. Special low-loss cables were used for connecting the antenna and the CMDR digital back-end. To preserve symmetry between channels, phase matched equal length cables were used for each path at the receiver side. Notably, a Keysight analog signal generator was used as the local oscillator (LO) and a 1:4 power splitter distributed the signal generator output to the four LO inputs of the mixers.

Subsequently, all four channels were downconverted (from X-band) to an intermediate frequency (IF) of 1 MHz, 1.5 MHz, 1.9 MHz and 2.4 MHz, corresponding to channel-1, channel-2, channel-3 and channel-4 respectively. This approach can be extended to any downconverted intermediate frequency (IF)/baseband (BB) frequency range. However, with increase in frequency, ADC sampling rate requirements increase proportionally. It is important to mention that due to limited availability of hardware components in the laboratory,

the authors decided to perform measurements using the mentioned frequencies (1 MHz, 1.5 MHz, 1.9 MHz, and 2.4 MHz). The maximum frequency that the authors could generate using the laboratory setup is 10 MHz from the arbitrary signal generator. Depending on the availability of high-speed ADC and walsh-hadamard (WH) code generator, suitable baseband bandwidth can be computed. Hence, the proposed approach is independent of signal carrier frequencies and modulation bandwidth.

We can still do the same measurement using 4 independent antennas. The reason for using the TCDA is that it provides >20:1 instantaneous BW, and we can customize our test scenarios (RF/mmWave test freq) to operate within any band. However, this is outside the scope of the current manuscript. Dealing with analog design circuitry as well as its interfacing with digital interfaces is always challenging, requiring massive engineering effort. The number of required components only for the four-channels case is a clear indicative on how complex the design of such systems is. Employing

TCDA/arrays overcome the path-loss at mm-Wave which is the end target.

After downconversion, the signals were encoded through the encoder board by multiplying with orthogonal WH codes of length 64 as generated by the RF-SoC FPGA board. The code generation circuitry was explained previously in Section III (A). Subsequently, the encoded signals were combined in the combiner chip mounted on the encoder board. The multiplexed output from the encoder circuit is then fed to a single ADC, also part of the RF-SoC chip on the FPGA board. After digitization, the captured data from the FPGA were post-processed to perform channel leakage suppression and signal recovery. The selection of the WH code sequence was verified experimentally to yield maximum auto-correlation and minimum cross-correlation for all 4 code sequences. This was demonstrated earlier by the correlation plots in Fig. 4.

A Keysight mixed-signal oscilloscope (with a maximum sampling rate of 20 Gsa/s and 10-bit ADC) was used to observe the code sequences, received and recovered signal information (phase and amplitude). A third-order Chebyshev filter is used as the low pass filter (LPF) and is usually implemented in the digital domain. However, for this work, it is implemented in MATLAB for subsequent measurements in Section VI.

Since the analog signals are encoded with digital codes in this experiment, several input-output (I/O) port conversion stages were used to interface the two signal types. Notably, spreading code impairments due to hardware constraints may increase the ACI and even worsen the situation at higher data rates. A 1-bit digitizer was therefore used to clean up the high frequency signal and minimize their correlation with the spreading codes. Also, differential signals were used to maintain the desired voltage swing and low noise required by the analog components in the encoder board.

VI. MEASUREMENT RESULTS

The main objective of the measurements is the faithful recovery of the phase and amplitude information of received signals after orthogonal encoding/decoding. As the signal chain includes both passive and active elements, the latter can contribute to the noise floor of the system. Therefore, before the measurement, a comprehensive power budget analysis was carried out to ensure that no device operates in the nonlinear region to avoid degrading the SNR.

A. VALIDATION USING CW-TONE

The first set of measurements include frequency-domain spectral contents of the desired signal and interference signals in each channel as shown in Fig. 12. We observe >20 dB isolation between the desired channel and the interfering ones. As noted, the degradation in ACI value is attributed to synchronization issues, component nonlinearities and possible hardware impairments. Especially, the large number of cables and several stages of I/O pins can cause impairments. Indeed, the achieved ACI is more than sufficient to recover the original

TABLE 5. Comparison of Signal (BPSK Modulated) Quality Between Received and Recovered Signals in Terms of NMSE (dB) Values for Different Sample Sizes

Chan No.	NMSE(dB)			
	$M=40,000$	$M=60,000$	$M=80,000$	$M=100,000$
1	-23.2105	-22.4112	-22.5255	-22.4548
2	-19.8520	-20.0994	-19.8470	-19.9593
3	-24.5920	-23.8556	-23.9606	-23.7916
4	-19.8478	-20.0927	-19.8418	-19.9525

signals. But, given the knowledge of the impairments, these can be removed via added filtering to increase SNR.

A comparator circuit was used to remove the higher frequency signal and minimize their correlation with the spreading codes. For beamforming, after the encoded signals are digitized, they are decorrelated with the same WH code sequences applied at the analog stage and the phase delay is extracted. The phase difference between the received and recovered signals is due to the cables involved and hardware nonlinearities. Since the cable delays and nonlinearities are known apriori, these differences can be compensated via filtering. This is done using a custom-designed filter as an IP-core in Vivado IDE software tool.

B. VALIDATION USING BPSK-MODULATED SIGNALS

The second set of measurements include system validation using modulated signal. In this case, a BPSK-modulated RF signal is used in each of the four channels. Fig. 13 shows the data acquisition setup, encoded signal, and the recovered signals in each of the channels. Fig. 13 shows just a portion of the measured data (100,000 samples) for better visualization of the quality of the recovered signals compared to the received signals in each of the channels. Hence, sample number of "0" corresponds to the starting point of the section that we want to present within our measured data set. Notably, the time-domain overlapping of the received and recovered BPSK modulated signals in most of the signal points gives an indication that the signal information (phase and amplitude) has been decorrelated correctly. The mismatches at some points could be attributed to hardware nonlinearities and component losses which makes maintaining the required SNR challenging.

In order to quantify the convergence behavior of the recovered signal to the received one in each channel, normalized mean square error (NMSE) in dB is computed as:

$$\text{NMSE (dB)} = 10 \log_{10} \left(\frac{\sum_{n=1}^M |\hat{y}(n) - y(n)|^2}{\sum_{n=1}^M |y(n)|^2} \right) \quad (7)$$

where $\hat{y}(n)$ is the recovered signal in each channel, $y(n)$ is the received signal at the RF-FE, and M is the number of samples used to calculate the NMSE values. The computed NMSE values are listed in Table 5 showing the variations in the NMSE values for different sample sizes. The discontinuity in the NMSE values is attributed to the hardware nonidealities and

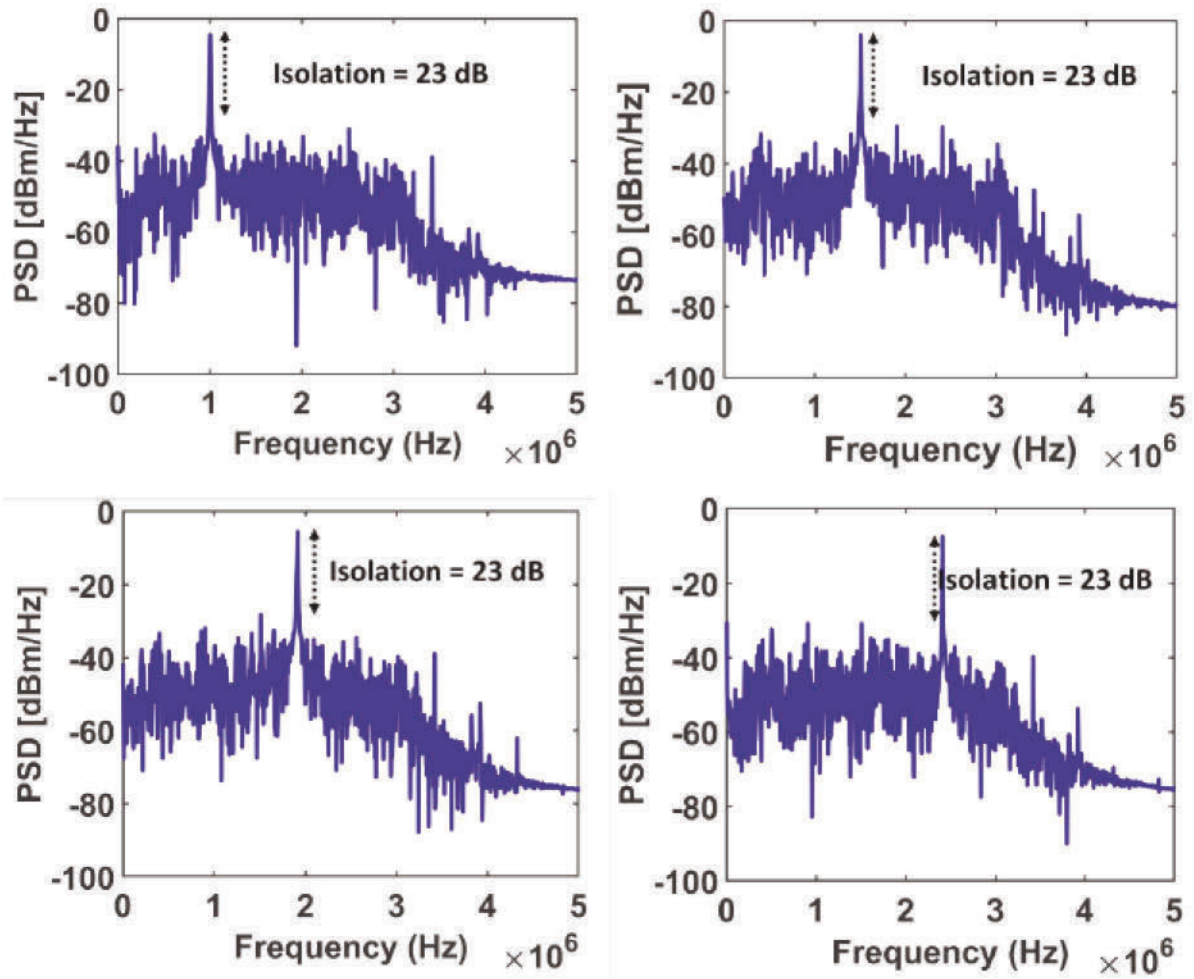


FIGURE 12. Spectral components of the four received signals demonstrating the suppression of the adjacent channel-leakage. The highest peak in each of the plots represents the desired channel signal power level; other peaks refer to interfering channel signals. The plots show ACI values of >20 dB isolation between the desired channel and the interfering channels, validating the proposed 4-channel CMDR system prototype.

calibration issue with the acquired data set. The WH codes generated from the VIVADO IDE software tool is downloaded as a bitstream to the FPGA. The captured code sets in the measurement setup shall reflect hardware nonidealities since both the code and analog signals are propagating through all the coaxial cables and custom designed circuit boards. Hence, the data set used to compute the NMSE values show some deviations in Table 5.

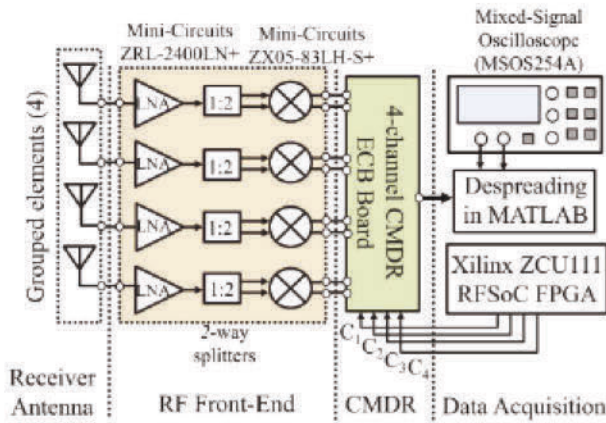
C. VALIDATION USING HIGHER ORDER (16/64/256-QAM) MODULATED WAVEFORMS

This section describes the system validation using higher order modulation schemes. In particular, a QAM (quadrature amplitude modulation) modulated waveform is employed to validate the robustness of the proposed receiver architecture. As previously mentioned, encoding and decoding operations are both performed on the received signals, a simplified system diagram is shown in Fig. 14. Two test points (TP) are considered: 1) TP-1: received symbols after the wireless channel, and 2) TP-2: decoding operation on the demodulated

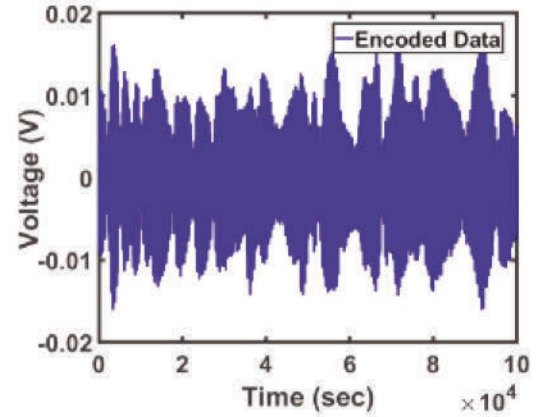
symbols. Error vector magnitude (EVM) is used as a figure of-merit to estimate the demodulation accuracy of the decoded symbols. Root mean square (RMS) form of the EVM can be expressed as:

$$EVM_{RMS} = \sqrt{\left(\frac{\frac{1}{P} \sum_{r=1}^P |S_{ideal}(r) - S_{act}(r)|^2}{\frac{1}{P} \sum_{r=1}^P |S_{ideal}(r)|^2} \right)} \quad (8)$$

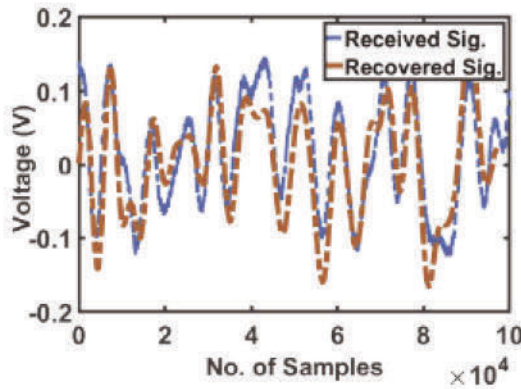
where $S_{ideal}(r)$ is the normalized ideal constellation point, $S_{act}(r)$ is the normalized actual symbol from the measurement setup, and P is the number of symbols in the constellation. 16-QAM, 64-QAM, and 256-QAM modulated waveforms are used for system validation. The EVM specifications for 5G base stations based on 3GPP 38.104 standard [40] are summarized in Table 6. The in/quadrature-phase (I/Q) symbol constellation points in each of the test points are shown in Fig. 15, where the red and blue constellation points represent the reference QAM symbols and recovered symbols after successful decoding process, respectively. The corresponding EVM values in each test points for the modulation schemes



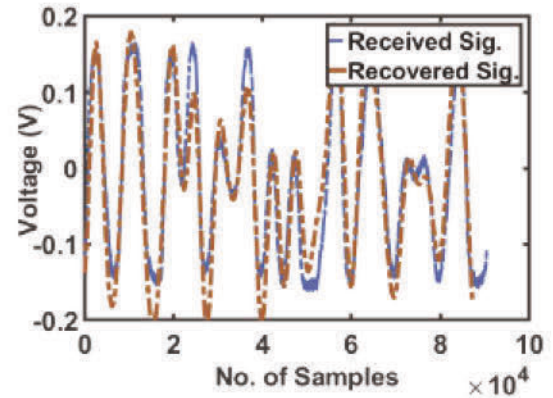
(a)



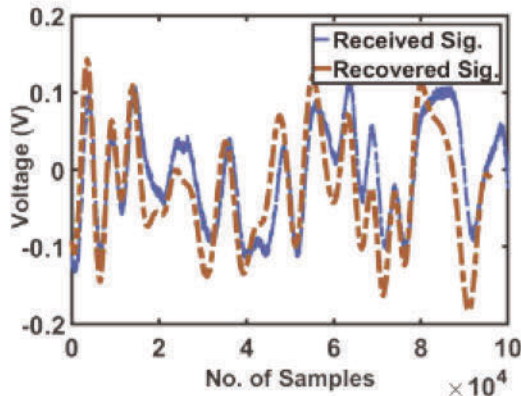
(b)



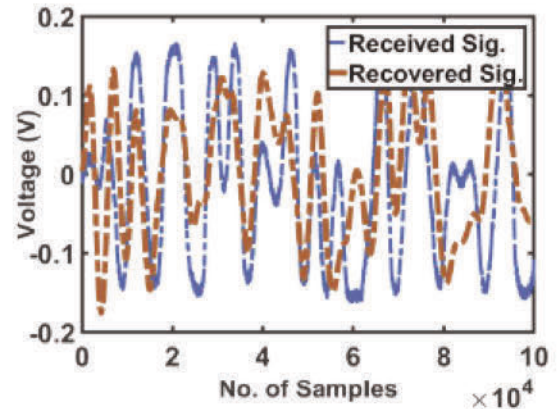
(c)



(d)



(e)



(f)

FIGURE 13. (a) Data acquisition setup to capture measurement data at the receiver front-end by the mixed-signal oscilloscope (MSOS254 A), (b) encoded (4-channels) signal at the CMDR. Time-domain comparison of a portion of the received signals (100 000 samples) and recovered signals is shown at (c) channel-1, (d) channel-2, (e) channel-3, and (f) channel-4, respectively. The received signals are indicated with blue color and the recovered signals are indicated with red color.

are tabulated in Table 7. Notably, Table 7 shows the proposed architecture achieves an RMS EVM of 5.11% after decoding the received symbols for the 16-QAM modulation case, which satisfies the EVM requirement of the 3GPP TS 38.104 standard. Similarly, in case of the higher modulation orders of

64-QAM and 256-QAM, the system maintains an RMS EVM of 6.81% and 3.57% at decoding the received symbols, respectively. The achieved results clearly demonstrate the potential of the presented system to be compatible with 5G and beyond communication systems.

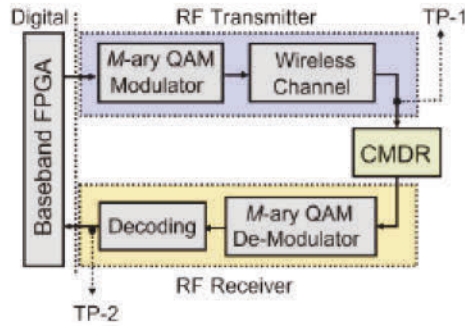


FIGURE 14. Simplified system diagram in the simulation setup for two different test points using 16, 64, and 256-QAM modulated waveforms.

TABLE 6. EVM Requirements for Different Modulation Schemes for 5G Base Stations According to 3GPP 38.104 Standard

Modulation Scheme	EVM Requirement(%)
16-QAM	12.5
64-QAM	8.0
256-QAM	3.5

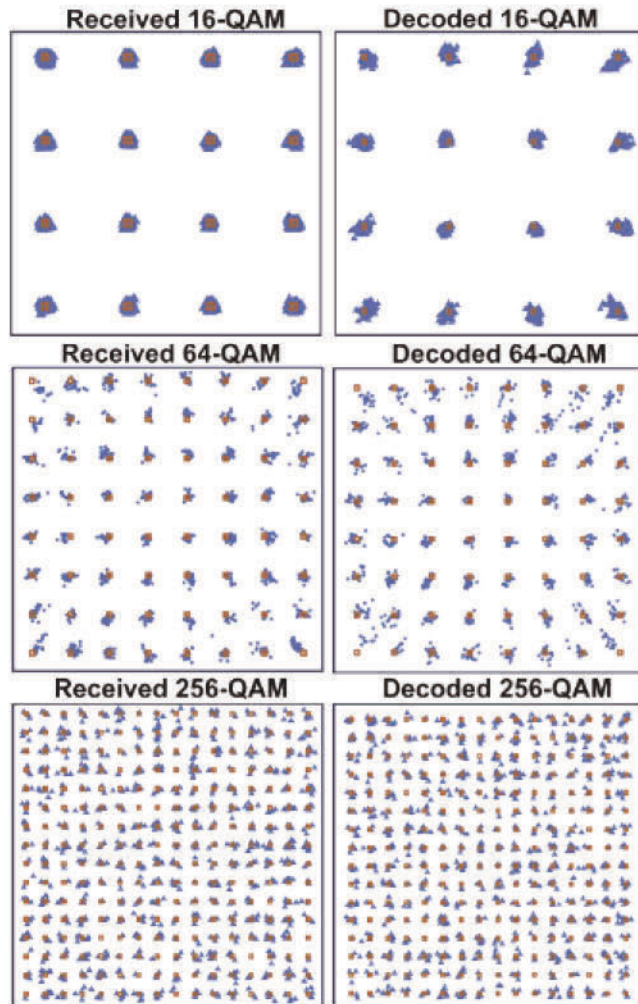


FIGURE 15. IQ constellation plots for two different test points using (a) 16-QAM, (b) 64-QAM, and (c) 256-QAM modulated waveforms.

TABLE 7. Performance Evaluation in Terms of EVM for the Test Case Scenarios of Fig. 14 Using 16, 64, and 256-QAM Modulation

EVM (%)	16-QAM		64-QAM		256-QAM	
	TP-1	TP-2	TP-1	TP-2	TP-1	TP-2
RMS	4.02	5.11	5.75	6.81	3.41	3.57
Peak	10.76	15.01	18.78	20.75	8.37	8.58

VII. CONCLUSION

In this article, a low-cost and low power coding-based receiver architecture was demonstrated for wideband antenna array beamforming. The beamforming receiver architecture was based on using Walsh-Hadamard codes to reduce the number of ADCs, resulting in significant power reduction and hardware implementation complexity. We also showed that the inclusion of the WH codes have little to no appreciable degradation in SNR requirement after successful decoding of the received signals. The orthogonality of the employed coding scheme was verified by computing the auto-correlation and cross-correlation plots. Adjacent channel interference suppression of >20 dB was achieved. EVM measurements are also included for higher order modulation schemes of 16-QAM, 64-QAM, and 256-QAM to demonstrate the robustness of the proposed system for 5G communication systems. Notably, the FPGA generated codes at 400 MHz employing a Xilinx RF-SoC data converter. To the best of the author's knowledge, this is the first time that such high data rates with high isolation have been demonstrated in a receiver system using code-multiplexing techniques.

APPENDIX

The decoded signal at the k th path in (2) is passed through a matched filter with impulse response

$$h_k(t) = \frac{1}{T_d} s_{d,k}(T_d - t) \quad (9)$$

The output of the matched filter is given by:

$$\begin{aligned} s_{dd,k} &= s_{d,k}(t) * h_k(t) \\ &= \frac{1}{T_d} \int_0^{T_d} s_{dd,k}(t) s_{d,k}(t) dt \end{aligned} \quad (10)$$

The decoded signal at the k_{th} path is calculated by substituting (6) and (7) in (8), and given by:

$$\begin{aligned} s_{dd,k}(t) &= \frac{1}{T_d} \int_0^{T_d} s_{dd,k}(t) s_{d,k}(t) dt \\ &+ \underbrace{\frac{1}{T_d} \int_0^{T_d} s_{d,k}(t) c_k(t) c_k(t) s_{d,k}(t) dt}_{\text{Desired channel}} \\ &+ \underbrace{\frac{1}{T_d} \int_0^{T_d} n_{d,k}(t) c_k(t) c_k(t) s_{d,k}(t) dt}_{\text{Noise from Desired channel}} \end{aligned}$$

$$\begin{aligned}
 & + \frac{1}{T_d} \int_0^{T_d} \sum_{i=1, i \neq k}^{N_c} \underbrace{s_{d,i}(t) c_i(t) c_k(t) s_{d,k}(t) dt}_{\text{Interfering Channels}} \\
 & + \frac{1}{T_d} \int_0^{T_d} \sum_{i=1, i \neq k}^{N_c} \underbrace{n_{d,i} c_i(t) c_k(t) s_{d,k}(t) dt}_{\text{Noise from Interfering Channels}}
 \end{aligned} \quad (11)$$

In (6),

$$\begin{aligned}
 \hat{s}_{d,k} &= \frac{1}{T_d} \int_0^{T_d} s_{d,k}(t) c_k(t) c_k(t) s_{d,k}(t) dt \\
 \hat{n}_{d,k} &= \frac{1}{T_d} \int_0^{T_d} n_{d,k}(t) c_k(t) c_k(t) s_{d,k}(t) dt \\
 \hat{s}_{d,i} &= \frac{1}{T_d} \int_0^{T_d} s_{d,i}(t) c_i(t) c_k(t) s_{d,k}(t) dt \\
 \hat{n}_{d,i} &= \frac{1}{T_d} \int_0^{T_d} n_{d,i}(t) c_i(t) c_k(t) s_{d,k}(t) dt
 \end{aligned} \quad (12)$$

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