Instability of On-Resistance in Vertical GaN PIN Diodes under High-Temperature and Voltage Stress

Dawei Wang, Dinusha Herath Mudiyanselage, Ziyi He, and Houqiang Fu, *Member, IEEE*

***Abstract*— The ON-resistance (R_{ON}) instability of vertical GaN PIN diodes under high-temperature (up to 400 °C) and forward voltages stress were comprehensively investigated. The turn-on voltages (V_{ON}) of vertical GaN PIN diodes under high-temperature or forward voltage stress were generally stable, while the instability of R_{ON} of the devices was very pronounced under temperature and voltage stress. With temperature increasing from 25 °C to 400 °C, both R_{ON} and ideality factor showed a similar trend with large variations in decrease and increase. The decrease in the ideality factor was attributed to the transition from Shockley–Read–Hall (SRH) recombination to carrier diffusion currents, while the increase in the ideality factor was due to the activation of additional trap-assisted recombination. During the long-time temperature stress, the R_{ON} was unstable and increased for several hours at 200 °C, likely due to time-dependent thermal activation of nitrogen vacancies (V_N) in p-GaN, while the R_{ON} remained roughly constant at 400 °C. For the forward voltage stress, it was found that the shift of R_{ON} was voltage-dependent and decreased from 1.05 to 0.6 mΩcm^2 with increasing forward voltage stress due to voltage-dependent carrier accumulation. Further, increased forward voltage stress will cause the sub-turn on current due to high electric field-induced electron injection into the p-GaN layer. In addition, the device R_{ON} can also be increased by high reverse voltage biasing due to holes being driven out of the p-GaN. These results can serve as a critical reference for the reliability study of vertical GaN devices and provide guidance for the future development of robust GaN power electronics.**

***Index Terms*—GaN, vertical transistor, vertical diodes, GaN stability, p-GaN, stability testing, power electronics.**

I. Introduction

Wide bandgap GaN RF and power electronics have been widely investigated for various applications due to the excellent material properties of GaN and their superior device performance compared with traditional semiconductor Si. GaN lateral high electron mobility transistor (HEMT) based RF amplifiers are now deployed in commercial 5G communications, and GaN power HEMTs with voltage ratings from 15 V to 900 V have been recently commercialized for applications in power supplies, data centers, and fast chargers [1-3]. Vertical GaN power devices have recently attracted significant attention since they have high voltage and current handling capability, immunity to surface-related issues, less cooling requirement, smaller chip area, avalanche capability, and better scalability [4-7].

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However, the material properties of GaN, especially the p-GaN material, are significantly different from those of Si and SiC, which leads to various stability issues [8-11]. For example, for lateral GaN devices, gate-bias-induced on-resistance (R_{ON}) instability is a serious concern in p-GaN HEMTs [12-14] due to dynamic effects in the AlGaN barrier and the GaN channel under the gate [15]. For GaN metal-insulator-semiconductor HEMT (MIS-HEMT), gate dielectrics usually lead to new issues, such as bias-temperature instability (BTI) [16, 17]. For vertical GaN devices, it was found that the turn-on voltage (V_{ON}) and R_{ON} in vertical GaN Schottky barrier diode (SBD) showed instabilities under on-state forward-current stress due to the degradation of the anode/GaN interface [18] and/or the trapping/de-trapping mechanism in passivation materials. For vertical GaN P-N junctions, the instability issue under high current-induced localized heating was more pronounced [19]. These instabilities in vertical GaN devices are due to trapping or floating body effects without permanent damage to the devices. These behaviors of these devices are not well described by standard equivalent circuit models used for Si and SiC, thus causing considerable power loss in compensation circuits and degrading the system reliability [11, 20-25]. In addition, carrier trapping can significantly increase the reliability and degradation concern due to high local electric fields [10].

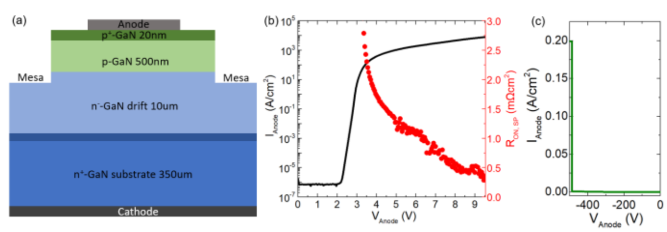

Fig. 1. (a) Schematic of the vertical GaN PIN diode. (b) Forward I-V curve and specific R_{ON} of the device. (c) Reverse breakdown curve of the device.

Vertical PIN diodes are generally preferred over SBDs for high-voltage, high-power applications due to excellent current capability and higher reliability [2]. But vertical GaN PIN diodes may exhibit instabilities under temperature and forward voltage stress, especially when the devices operate under dynamic voltages [26], due to carrier flow through highly doped p-GaN with low effective ionization of acceptors, degraded crystal quality, and high density of defects [27]. However, there is still a lack of systematic stability study of GaN vertical PIN diodes under forward bias. In this work, the effect of forward voltage and high-temperature (up to 400 °C)

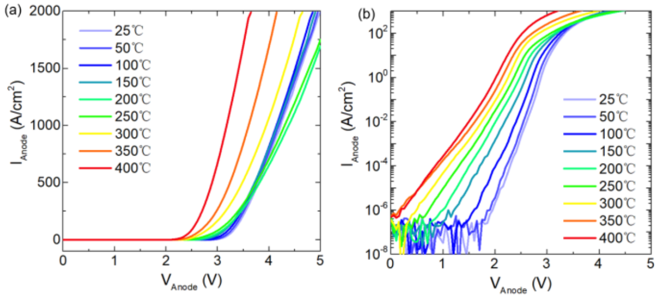

Fig. 2. Forward I-V curves of the vertical GaN PIN diode at different temperatures (a) in linear scale and (b) in semi-log scale.

stress on V_{ON} and R_{ON} of vertical GaN PIN diodes have been comprehensively investigated. This work can serve as a critical reference for the reliability evaluation of GaN vertical PIN diodes under high-temperature and voltage applications and provide guidance for the future development of reliable vertical GaN power devices.

II. Device Fabrication and Measurement

The vertical GaN PIN diodes were grown on a 2-inch n^+-GaN substrate by metalorganic chemical vapor deposition (MOCVD). As shown in Fig. 1 (a), the device consisted of a 350 μm n^+ doped GaN substrate with a Si doping concentration of 1×10^{18} cm^{-3}, a 2 μm n^+-GaN layer with a doping concentration of 3×10^{18} cm^{-3}, a 10 μm n^--GaN drift layer with a doping concentration of 1×10^{16} cm^{-3}, a 500 nm p-GaN layer with an Mg doping concentration of 1×10^{19} cm^{-3}, and a 20 nm p^+-GaN with an Mg doping concentration of 3×10^{19} cm^{-3}. The diode fabrication started with p-GaN activation under 750 °C for 30 minutes, followed by 800 nm mesa isolation via chlorine-based dry etching. The cathode metal stacks Ti/Al/Ni/Au (25/120/40/100 nm) were deposited by electron beam evaporation on the backside of the samples. The anode contacts Pd/Ni/Au (25/30/150 nm) were deposited on top of the p^+-GaN layer by electron beam evaporation, followed by rapid thermal annealing at 500 °C for 5 minutes in N_2 ambient.

High-temperature stability testing and forward-bias stability testing of these vertical GaN PIN diodes were performed. The testing of device stability under high-temperature stress was conducted using a probe station equipped with a controllable thermal chuck and Keithley 4200-SCS parameter analyzer. The forward I-V curves of the devices were measured during the temperature stress to monitor the evolution of the stress-induced parameter shift, such as V_{ON} and R_{ON}. For stability testing under forward-bias stress, the Keithley 2611A source meter was used to measure the device's forward I-V curves under forward voltages. The V_{ON} was defined as when the device current reaches 1 A/cm^2. The R_{ON} is the minimum value of dV/dI, i.e., at liner region of on-current. The measured typical I-V curve and calculated specific R_{ON} of a representative vertical GaN PIN diode at room temperature without stress are shown in Fig. 1(b). The devices had a maximum on-current density of >8 kA/cm^2, an ON/OFF ratio of $>10^9$, an ideality factor of ~2, R_{ON} of <0.5 $m\Omega cm^2$, and breakdown voltage of 487 V, which are comparable to previous reports [28-31].

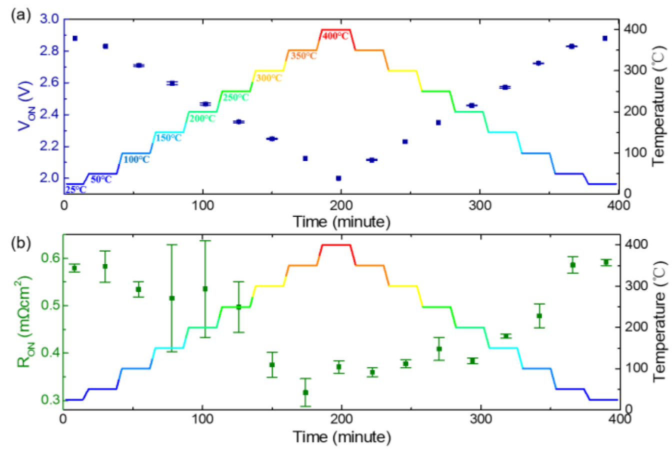

Fig. 3. (a) The V_{ON} of the vertical GaN PIN diodes under the temperature stress from 25 °C to 400 °C and the cool down process. (b) The R_{ON} of the vertical GaN PIN diodes under the temperature stress from 25 to 400 °C and the cool down process. Each temperature stage has multiple measurements.

III. Results and Discussions

A. R_{ON} Instability under High-Temperature Stress

The devices were thermally stressed from 25 to 400 °C with a step of 50 °C for 25 minutes at each temperature, where a 10-minute stabilization time was included when the temperature was changed. Several forward I-V curves of the devices were collected every 2 minutes during each temperature to monitor the evolution of V_{ON} and R_{ON}. Fig. 2(a) shows the forward I-V curves of the vertical GaN PIN diodes at different temperatures. It showed that the V_{ON} and R_{ON} of the devices varied with increasing temperatures. Fig. 2(b) shows the forward I-V curves in a semi-log scale. The extracted device V_{ON} during the whole temperature ramp-up and cooling-down process is shown in Fig. 3(a). The V_{ON} decreased from 2.88 V to 1.95 V when the temperature increased from 25 to 400 °C due to the temperature-induced barrier lowering in the depletion region [4, 29, 42-44]. Moreover, it can be noticed that the V_{ON} was stable during each temperature step. After the device was cooled to room temperature, V_{ON} recovered to the original value. Fig. 3(b)

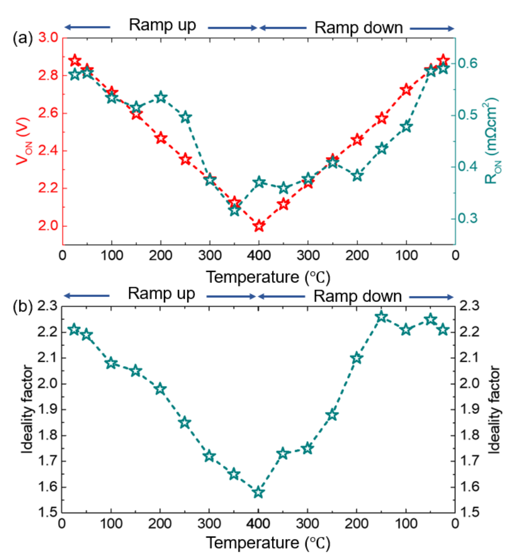

Fig. 4. (a) The V_{ON} and R_{ON} and (b) ideality factor n of the vertical GaN PIN diodes with different temperatures extracted from Fig. 2.

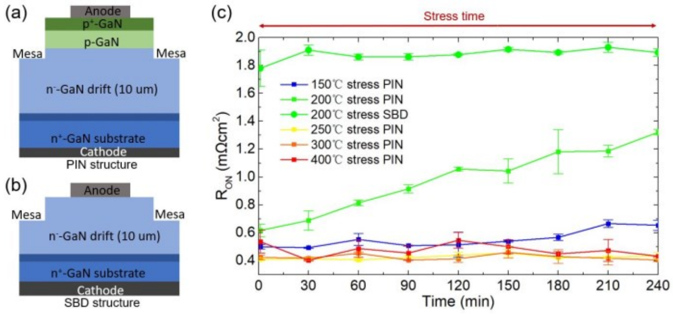

Fig. 5. Schematic of the vertical GaN (a) PIN diodes and (b) reference SBD. (c) The R_{ON} of the vertical GaN PIN diodes and SBDs under 200 °C, and R_{ON} of the vertical GaN PIN diodes at 150 °C, 200 °C, 250 °C, 300 °C, and 400 °C long-time temperature stress.

presents the extracted R_{ON} of the devices at different temperatures. The device R_{ON} generally decreased during the temperature ramp-up process from 25 to 400 °C and increased during the temperature ramp-down process. This can be explained by the conductivity change in the p-GaN. The conductivity of the p-GaN is proportional to the product of mobility and hole carrier concentration. Due to the high acceptor ionization energy and incomplete acceptor ionization in p-GaN, when the temperature increased, the concentration of free holes would increase [35]. In Fig. 3(b), the device R_{ON} could recover after the temperature was ramped down. However, it can be noticed that the device R_{ON} has a relatively longer error bar under thermal stress of ~150-250 °C during the ramp-up process, indicating an evident instability issue of R_{ON} of vertical GaN PIN structure during ~150°C-250°C. This will be discussed in detail later. The trend of V_{ON} and R_{ON} of the vertical GaN PIN diodes with different temperatures extracted from Fig. 2 is shown in Fig. 4(a). The overall trend of device V_{ON} and R_{ON} with temperature was consistent with that in Fig. 3. The extracted device ideality factor n as a function of temperature is shown in Fig. 4(b). Diodes generally have an ideality factor between 1 and 2 due to the combination of carrier diffusion and recombination processes, such as Shockley–Read–Hall (SRH) and band-to-band recombination. In addition, trap-assisted tunneling and carrier leakage can also cause an increase in the ideality factor [36-38], leading to high ideality factors of over 2. From Fig. 4(b), the ideality factor generally decreased with increasing temperature due to the transition from SRH recombination to diode diffusion current due to higher energy carriers [39]. The ideality factor also does not show symmetrical characteristics during temperature ramp-up and ramp-down process. This indicated activation or de-activation process of traps (e.g., nitrogen vacancy (V_N) [45-47]), happened at different temperature between ramp-up and ramp-down, which induced variation of trap-assisted recombination of carriers [36-38, 40-41]. For the instable R_{ON} around 200 °C, we designed another experiment to investigate the R_{ON} instability under long-time temperature stress at different temperatures for 4 hours. The extracted R_{ON} of the devices under long-time thermal stress is analyzed in Fig. 5.

In addition, to verify whether the R_{ON} shift during the stress of 200 °C was caused by p-GaN, vertical GaN Schottky barrier diodes (SBDs) were fabricated and thermally stressed for comparison. The schematics of the vertical GaN PIN diode and SBD are shown in Fig. 5(a) and 5(b), respectively. The vertical GaN SBD had the same device structure as the PIN diode except without p-GaN layers. The Schottky contact for the GaN SBD was Ni/Au (25nm/150nm). Fig. 5(c) shows the R_{ON} of the vertical GaN PIN diodes and SBD during the temperature stress. When the 250 °C, 300 °C, and 400 °C thermal stress was applied to the PIN diode, the device R_{ON} remained relatively stable during the stress. However, the device R_{ON} under 150 °C and 200 °C thermal stress increased with increasing stress time. The increasing of R_{ON} under 200 °C is more evident. On the other hand, the vertical GaN SBDs under 200 °C thermal stress showed relatively stable R_{ON}. This indicates that the observed time-dependent R_{ON} shift at ~150-200 °C for GaN vertical PIN diodes was caused by conductivity modulation of p-GaN material [48]. A series of electrical-thermal effect may modulate the R_{ON} during the long-time thermal stress. At high temperature such as 400℃, the carriers have enough energy to be released from the traps in p-GaN, resulting in stable R_{ON}. At medium temperature such as 200℃, the energy is not enough to activate the trapped electrons in p-GaN. However, the applied positive voltage during I-V curve scanning can lower the conduction band and release some electrons, thus gradually increasing the R_{ON}. It is likely that V_N in p-GaN are the activated traps, where the V_N-Mg_{Ga} complex has been identified [49-50]. The electrons can be gradually released when the temperature increases above ~200 °C and compensate the holes in p-GaN, thus reducing the conductivity of the p-GaN layer. In addition, similar effects of conductivity modulation on temperature-induced carrier instability have also been investigated in some reports of p-GaN gated HEMT devices, with identified mechanisms such as hole trap emission, carrier out-spilling [32], trapped positive charges [33], and hole injection through thermionic emission [34]. The extracted V_{ON} under 4 hours of temperature stress at 200 and 400 °C is shown in Fig. 6(a), indicating that the device V_{ON} is generally stable at high temperatures. The forward I-V curves measured at room temperature before and after the temperature stress of 4 hours are shown in Fig. 6(b). For the curves before and after the temperature stress of 200 °C, the current decrease after the stress due to the R_{ON} modulation process during 200 °C, which indicated that the R_{ON} shift cannot be recovered when the temperature stress was removed. For the curves before and after the temperature stress of 400 °C, the current has a slight increase, possibly due to the hydrogen residue driven out.

B. R_{ON} Instability under Forward Voltage Stress

Several reports have shown voltage and current stress-caused parameter shifts in GaN devices [25, 51-54]. Hole deficiency in p-GaN occurred at the beginning of the applied

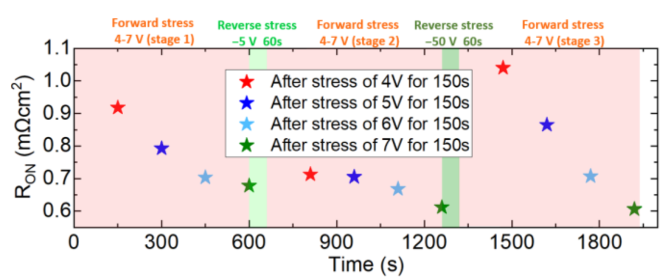

Fig. 7. (a) The testing process of device R_{ON} under the forward voltage stress from 4 V to 7 V and reverse stress of −5 V and −50 V.

voltage [25]. Trapping and de-trapping in p-GaN or n-GaN occurred during the long-time voltage stress [53, 54], and the energy level of traps can be shallow levels (0.26eV, 0.59eV, 0.71eV [55-57]) or many deep levels [26, 27]. To date, several interpretations of trapping mechanisms have been reported, such as nitrogen vacancies, carbon and hydrogen impurities, and magnesium-hydrogen complex formation [26]. It was also found from the voltage-transient method that the trapping process at different energy levels was time-dependent. And slow trapping transients can happen at room temperature in the order of a few seconds [54].

Fig. 7 shows the R_{ON} testing scheme under different forward voltage stress at the fixed time (150s) before and after reverse voltage stress. First, forward stress from 4 V to 7 V was applied to a fresh device (as stage 1), the R_{ON} were extracted during the forward stress. Then, the same experiment was repeated after the negative low voltage of −5 V and −50 V were applied to the device (as stage 2 and 3). The extracted R_{ON} with different stress time from 30s to 150s of stage 1, 2 and 3 were shown in Fig. 8(a), Fig. 8(b) and Fig. 8(c), respectively. From Fig. 8(a), It was found that the R_{ON} of the GaN PIN diode shifted under positive voltage stress, and the shift was also voltage dependent. The R_{ON} of the devices decreased from 0.92 to ~0.65 mΩcm^2 with increasing stress voltage, while R_{ON} was less sensitive to stress time. Fig. 8(b) showed that after the negative stress of −5 V, the R_{ON} of the device increased to 0.72 mΩcm^2. From Fig. 8(c), after the reverse voltage stress of −50 V, the R_{ON} of the device increased to ~1.05 mΩcm^2. The mechanism of R_{ON} shift under voltage stress can be explained from the band structure in Fig. 9. In Fig. 9(a), a fresh device has high R_{ON} due to hole deficiency in p-GaN [25]. When a forward voltage is applied, the p-GaN will be charged by hole injection, thus decreasing the device resistance. And the quantity of the injected holes depends on the applied voltage. However, when a reverse voltage is applied to the device in Fig. 9(b), the holes are driven out of the p-GaN by a high negative electric field, thus increasing the device's resistance. The V_{ON} of the device under

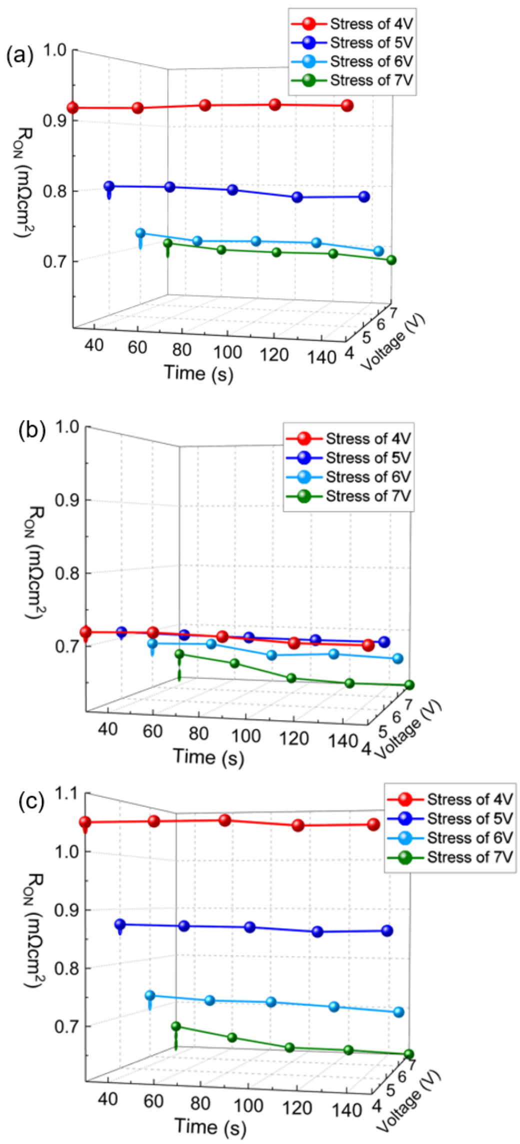

Fig. 8. The R_{ON} of vertical GaN PIN diodes under forward voltage stress from 4V to 7V with stress time from 30 to 150 s: (a) without reverse voltage stress; (b) After reverse voltage stress of −5 V. (c) After reverse voltage stress of −50V.

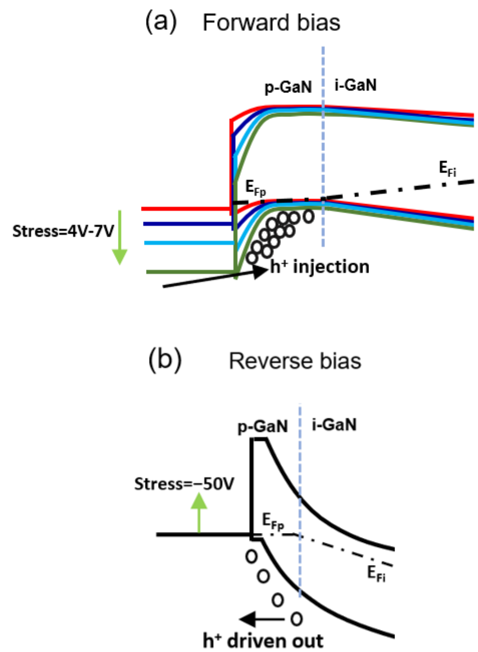

Fig. 9. Band diagram near the surface of vertical GaN PIN diode under (a) forward bias from 4V to 7V and (b) under reverse bias.

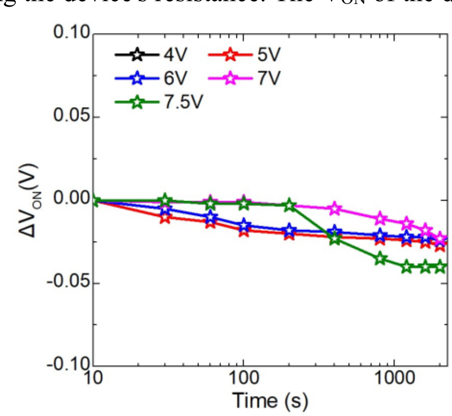

Fig. 10. The V_{ON} of the vertical GaN PIN didoes under forward voltage stress from 4V to 7.5V with the stress time of 1200s at each voltage.

positive voltage stress was also extracted in Fig. 10. It shows that the positive voltage stress does not have an evident impact on the V_{ON}, and the shift of the V_{ON} was less than 0.05 V. In addition, we also studied the effect of higher positive voltage stress on GaN vertical PIN diodes. Figs. 11 (a) and (b) show the measured forward curves under high positive voltage stress from 8.5 to 9V. From Fig. 11(a), it can be noticed that after the high positive voltage stress, the leakage current before the turn-on voltage (2.88 V) increased, especially after the stress of 8.8 and 8.9 V. From Fig. 11(b), the leakage current also increased evidently after voltage stress of 9 V. The device behavior at high forward bias can be explained by the band structure in Fig. 11(c). The drastic band bending at a high forward voltage can drive the electrons into the p-GaN region and induce an electron current before the device is turned on. No device recovery was observed after several days or by reverse stress, indicating that the transient high voltage spikes are detrimental to vertical GaN PIN diodes.

IV. Conclusion

In conclusion, a comprehensive investigation of vertical GaN PIN diode stability under thermal and forward voltage stress was presented. The device V_{ON} was quite stable under high-temperature or forward voltage stress, while the device R_{ON} showed large instabilities. With the temperature increasing from 25 °C to 400 °C, both the device R_{ON} and ideality factor first decreased, then increased with a maximum at ~200 °C and further decreased until 400 °C. The transition from SRH recombination to carrier diffusion can decrease the ideality factor, while the activation of trap-assistant recombination can increase it. During the long-time temperature stress of 200 °C, the R_{ON} was unstable, likely due to time-dependent thermal activation of V_N in p-GaN material, while the R_{ON} kept roughly constant at 400 °C since the carriers are constant. Furthermore, the shift of R_{ON} is voltage-dependent and decreased from 1.05 to ~0.6 mΩcm^2, with the forward voltage stress increasing from 4 to 7 V due to voltage-dependent carrier accumulation. If the forward voltage stress is further increased, high forward voltage stress will cause the sub-turn on current due to high electric field-induced electron injection into the p-GaN layer. In addition, the R_{ON} can also be increased by high reverse voltage biasing due to holes being driven out of p-GaN. This work provides important information on the reliability of vertical GaN PIN diodes under temperature and forward voltage stress, which is beneficial for the commercialization of vertical GaN power technology.

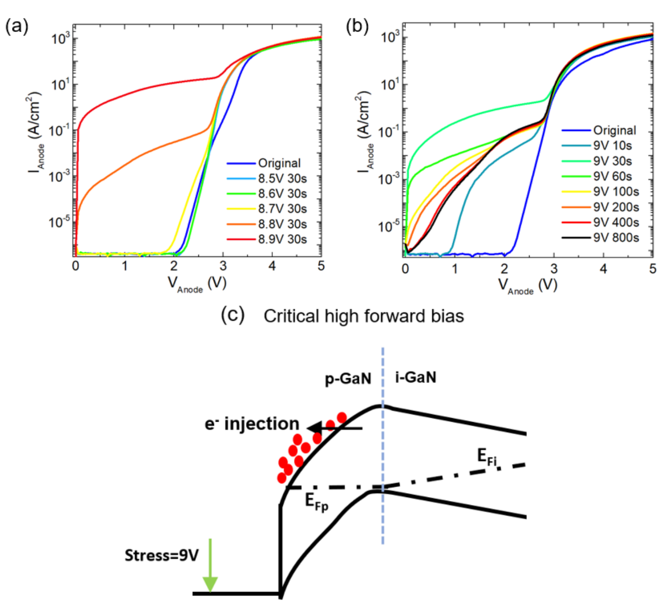

Fig. 11. (a) Forward I-V curves of vertical GaN PIN diodes after forward voltage stress of 8.5, 8.6, 8.7, 8.8 and 8.9 V. (b) Forward I-V curves of vertical GaN PIN diodes after forward voltage stress of 9 V from 10 to 800 s. (c) Band diagram of vertical GaN PIN diodes under very high forward voltage bias.

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