Low-Power Solid-State Transformers to Replace Line-Frequency Class 2 Transformers

Allen T. Nguyen, Charles R. Sullivan
Thayer School of Engineering at Dartmouth College
Hanover, NH 03755 USA
Allen.T.Nguyen.th@dartmouth.edu, Charles.R.Sullivan@dartmouth.edu

***Abstract*—Class 2 transformers are small line-frequency transformers widely used for control systems requiring 24 VAC signaling, including residential and commercial HVAC systems, industrial controls, and much more. These transformers have large standby losses, low efficiencies, large weights, and high costs. In this work, we propose a power electronic alternative in the form of a low-power solid-state transformer. We design and test two 40 VA 120 VAC to 24 VAC solid state transformers, including a two-stage and a single-stage topology. Both converters provide higher efficiencies across all load ranges compared to the Class 2 line-frequency transformers, especially at light load (5 VA) with improvements of 18.6% and 30.0%, respectively. Standby losses for the two are 417 mW and 205 mW, compared to an average of 2.8 W standby loss for 40 VA Class 2 line-frequency transformers.**

***Index Terms*—Class 2, line-frequency transformer, solid-state transformer, standby loss, light-load efficiency, low-power, AC-DC-AC, AC-AC**

I. Introduction

Line-frequency transformers (LFT) are almost obsolete in low-power ($<$ 100 W) power delivery. However, there is one scenario where low-power line-frequency transformers find significant use: control systems that require 24 VAC power and signal lines. Finding use in almost all heating, ventilation, and air conditioning (HVAC) systems, industrial control systems, doorbells, and more [1], these transformers meet "Class 2" safety requirements under UL standards [2] and the U.S. National Electric Code [3].

Although simple in construction, these transformers have major disadvantages. Low-frequency operation requires a much larger volume compared to high-frequency transformers used in power electronic converters for the same power level. In terms of construction, their volume mostly consists of copper and steel, resulting in large weights (0.5 lbs) and cost (US $10-60). In [4], testing of these line-frequency Class 2 transformers found low average efficiencies and a large average standby loss of 2.8 W. In most applications, these transformers are connected to line voltage continuously, to provide power to the control systems that power up additional equipment when needed. With these devices widely used in residential, commercial, and industrial buildings, there is tremendous potential for energy savings if the loss is reduced, especially their standby loss [5].

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One potential solution to reduce standby losses would be to substitute the core with lower loss core materials [6]–[9], as standby losses are dominated by core loss [10]. Also increasing the core area and adding more winding turns could reduce flux. Thus, it is possible to reduce standby losses by adjusting the design and materials, but with increased cost.

An alternative is to implement an isolated AC-AC switching power converter, also known as a solid-state transformer (SST) [11]–[17]. In the case of high-efficiency AC-DC switching power converters, designers use a variety of techniques to achieve low no-load or light-load loss [18], [19], often holding a DC output voltage on a capacitor to maintain the voltage as needed. Where an AC output is needed, this strategy is not directly applicable, and achieving very low standby loss will be more difficult. Nonetheless, standby losses of Class 2 line-frequency transformers are so large that an SST replacement can dramatically reduce the loss even if it can't have standby loss as low as a state-of-the-art AC-DC power supply optimized for light-load operation.

Most proposals for SST applications are at high power levels (100+ kVA) [20]–[30], where line-frequency transformers are highly efficient, making them hard to compete with. Typical applications are motivated by a need for light weight or flexible control. But at the much lower power levels of typical Class 2 transformers (20–80 VA), line-frequency transformer performance is so bad that a solid-state transformer can be designed have better efficiency by a large margin, resulting in a clear advantage even where control options and weight aren't critical.

In this work, we develop two 40 VA, 120 VAC to 24 VAC solid-state alternatives to Class 2 line-frequency transformers, assesses their performance, particularly their standby loss, and compare it with line-frequency transformer performance reported in [4]. The sections are organized as follows: Section II provides a summary of potential SST architectures considered for a Class 2 LFT replacement, discussing the design constraints that a low power SST requires. Section III and IV provides theory of operation and hardware implementation for the two architectures selected for prototyping. Lastly, Section V provides prototype experimental results.

II. Potential low-power SST architectures

Much previous work, reviewed in [11]–[17], has compared different SST topologies, especially their capabilities and

benefits for grid-level voltages and power. However, an SST designed for the same functionality as a Class 2 LFT should be low power ($<$ 100 VA) and single phase, and at the same time, inexpensive. Thus, replacement designs and SST architecture selection should reflect that.

Broadly, previous SST comparisons have split them into categories based on the number of power conversion stages [11]–[17]. Three-stage (AC-DC-DC-AC) designs [20]–[23], shown in Fig. 1, often use an input rectification stage, a secondary isolated DC-DC stage, followed by an inverter; with each stage connected by a DC link. However, in our application, the extra DC link rarely finds utility, while the large number of components and stages possibly lowers efficiency and reliability. For these reasons, three-stage topologies were not considered in this work. The focus will rather be on two-stage and single-stage designs.

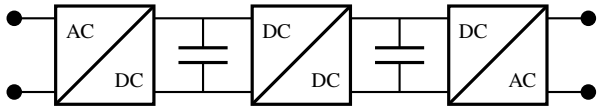

Fig. 1: Simplified diagram of a three-stage SST

Two-stage (AC-DC-AC) designs are quite similar to three-stage SSTs, but with only a single DC link and without an intermediate DC-DC converter. Depending on where the isolation barrier is placed, either in the first or second stage, two-stage designs can either have a low-voltage or high-voltage DC link [17]. A simplified diagram is shown in Fig. 2. Like three-stage architectures, flexibility in topology selection in the two stages is an advantage, as recent AC-DC stages for SST applications have been seen to achieve low THD [31] and soft-switching over an entire line cycle [32], while advanced inverter topologies, like flying-capacitor based inverters [33], potentially reduce passive component size and reduce voltage requirements for active devices as compared to standard inverters. Two-stage designs could also see reduced costs and size by using commercial off-the-shelf supplies as the first stage, as isolated AC-DC power supplies are widely mass-produced.

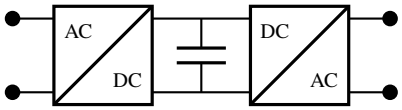

Fig. 2: Simplified diagram of a two-stage SST

Single-stage (AC-AC) designs, shown with Fig. 3, are the simplest possible SST architecture, mainly using a high-frequency (HF) transformer to step down the input voltage. The simplest operation is as follows: the input voltage is modulated to a much higher frequency; this now HF waveform is passed through a HF frequency transformer which steps down the voltage; and this HF low voltage waveform is then reconstructed to reinstate the original input frequency. This direct conversion omits the use of a DC link; consequently, input power transients are not adjusted for and are reflected to the output. Also, unlike multi-stage SSTs, some single-stage SSTs topologies require four-quadrant switching devices as they lack the initial rectification stage. An intial rectification stage and a final unfolding stage can be added to mitigate this, but at the cost of an increased component count.

Previous AC-AC SST designs have used resonant tanks [27]–[30] or phase shifted controls (in the form of a dual-active bridge [26]) to reduce otherwise large switching losses and provide bidirectional power flow. However, in this application, our main goal is simplicity and low cost. Control of the conversion ratio is not needed, as the output voltage can be unregulated, and so simple fixed-frequency, fixed-duty-cycle operation can be used, with resonance used to achieve soft switching in only part of the line cycle.

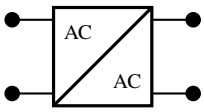

Fig. 3: Simplified diagram of a single-stage SST

Overall, the leading candidates are a two-stage architecture leveraging economies of scale and excellent light-load performance of conventional isolated AC-DC power supplies, or a single-stage design benefiting from the small number of components and potentially achieving higher efficiencies. In the following sections we develop and test designs for both.

III. AC-DC-AC Solution

A. Converter Overview and Operation

The first design (SST1) selected to prototype uses a two-stage architecture, an isolated AC-DC converter stage producing a DC voltage (V_{DC}), followed by a PWM inverter to synthesize the AC output. A simplified schematic is shown in Fig. 4.

The first stage uses a commercial off-the-shelf (COTS) power supply as the isolated AC-DC converter. The AC-DC converter can use standard techniques to achieve high efficiency at light load [18], [19], such that the standby loss of the system is limited primarily by the standby loss of the second stage (the inverter).

The inverter was selected to be a standard full-bridge topology. Other inverters were considered, including capacitor based/hybrid converters [33], but even a simple inverter can be designed to obtain a magnetics volume a tenth of the size of a LFT. Future work implementing more advanced inverters could potentially drive this volume much lower; however, increased complexity could potentially increase cost while reducing reliability. On the other end, a half-bridge inverter was also considered. The minimal number of active switches reduces gate drive complexity compared to a full-bridge; however, the capacitors have to be large to store energy at 60 Hz, whereas the input capacitor for the full-bridge can be sized only for the high-frequency current, leading us to choose the full-bridge topology.

The inverter is operated with a three-level sinusoidal pulse width modulation (PWM) control scheme; in this control

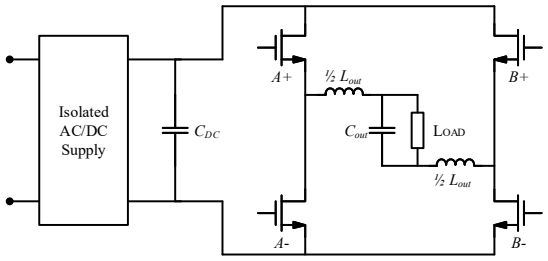

Fig. 4: Simplified schematic of SST1

scheme [34], the switches in a leg are switched in a complementary fashion with a finite deadtime to avoid any shoot through. The A leg has a duty ratio of D_A, at a specified switching frequency; similarly, the B leg has a duty ratio of D_B. This D_A is then modulated at 60 Hz to create a sinusoidal waveform. The B leg operates the same; however, the reference sinusoidal modulation waveform of D_B is phase shifted by 180 degrees compared to D_A. Thus, the voltage across the two legs is switching at twice the switching frequency, allowing for smaller magnetics. The filter inductor was also split into two separate inductors to ensure that if the load was grounded, the full-bridge switching nodes would not switch voltages at the ground potential.

The filter design is thus straightforward: the main high-frequency content is found at twice the switching frequency, and thus the designed cutoff frequency should be before that. However, during the no-load condition, low frequency voltage across the output filter capacitor introduces reactive current, potentially increasing conduction losses. Thus, lower value capacitors are preferred at the expense of a larger inductor or larger output voltage ripple.

B. Hardware Implementation

The selected COTS supply, named in Table II, supplies a DC voltage of 36 V. This requires the inverter to operate with a modulation index [34] of 0.95 to achieve an output voltage of 24 VAC. To prioritize no-load efficiency, the selected switching frequency is 100 kHz; and the PWM is operated with a deadtime of 100 ns to avoid shoot-through.

Since the filter processes both a large low-frequency current and lower amplitude high-frequency ripple current, the inductor must be designed such that it achieves low winding resistance at both these conditions. Litz wire [35] is a common solution to reduce high-frequency resistance; however, a full litz-wire wound inductor would see higher low-frequency resistance than its solid-wire counterparts. Thus, the inductor construction uses both solid wire and litz wire in parallel to achieve low winding resistance at low frequency whilst slightly increasing high-frequency resistance in the inductor [36]. Fig. 5 shows the cross-section of the inductor design. The litz wire was placed along the wall of the inductor curved away from the gap to ensure that high-frequency current sees a low resistance path. Table I lists further details of the inductor construction.

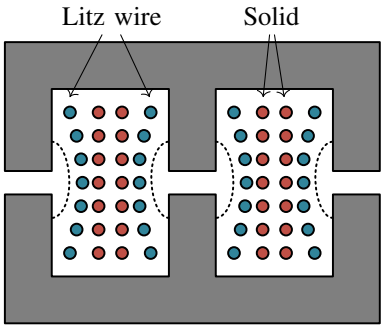

Fig. 5: Simplified cross-section of the designed inductor for SST1, the litz wire (blue) and the solid wire (red) are wound in parallel with the litz wire shielding the solid wire from the immediate fringing fields (dashed lines), the litz wire is also wound to slightly curve around the fringing fields to reduce higher frequency losses

Description	Value
Core Material	N95
Core Geometry	RM7
Winding	16 turns AWG24||100/AWG44

TABLE I: SST1 inductor specific parameters

The inductor current ripple was selected to be 250 mA and the output voltage ripple was selected to be 300 mV; these values placed emphasis on a higher value for the inductor, rather than the capacitor, reducing the reactive current produced by the output capacitor. The calculated values of the output inductor and capacitor are outlined in Table II. The selected capacitor value results in a 60 Hz reactive current of 4 mA, and an overall filter cutoff frequency of 16 kHz, well below twice the switching frequency.

Symbol	Description	Value
f_{sw}	Switching Frequency	100 kHz
V_{in}	Input Voltage	120 VAC
V_{out}	Output Voltage	24 VAC
P	Rated Power	40 VA
	COTS Supply	L6R48-360
	MOSFETs	PXN012-60QLJ
L_{out}	Filter Inductance	200 μH
C_{out}	Filter Capacitance	470 nF

TABLE II: SST1 system parameters and final measured component values

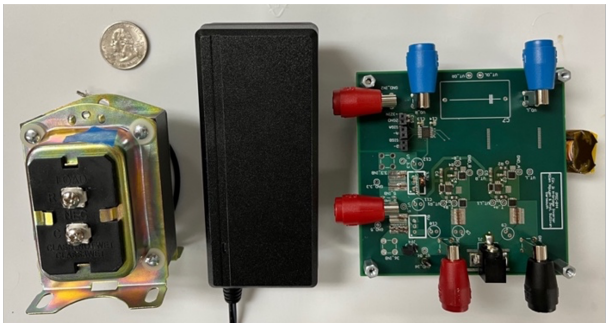

Fig. 6: Class 2 LTF (left), COTS power supply (middle), PWM inverter (right)

IV. AC-AC Solution

A. Converter Overview and Operation

The second design (SST2) is a single-stage topology, using back-to-back power semiconductors for bidirectional voltage blocking; realized by placing two power transistors in series connected by their source nodes, as in [25], [26]. It can also be implemented with single bidirectional voltage blocking switches (rather than back-to-back power semiconductors) when they become commercially available.

A simplified schematic is shown in Fig. 7, with half bridges for both the input facing and output facing terminals. Including an initial rectification and an output unfolding stage was considered to avoid the use of four-quadrant power switches, but the increase in components would potentially lower efficiency and increase solution complexity as the rectification and unfolding stages must be synchronized to the grid. Full bridges were also considered, but this would increase component count, and without the need to vary the conversion ratio, we don't need the control flexibility of a full bridge.

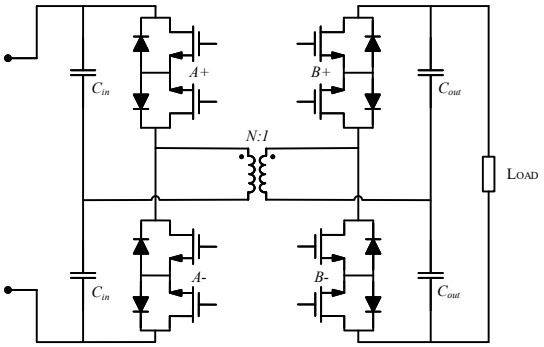

Fig. 7: Simplified schematic of SST2

The primary and secondary half bridges are operated synchronously with the duty cycle fixed to a nominal 50% at a constant switching frequency (f_{sw}). Because Class 2 LFTs have an unregulated output, there is no need to regulate the output of SST2 through varying duty cycle or f_{sw}, and this reduces the need for complex control. It also enables minimizing passive components while still achieving soft switching through most of the line cycle. Although the circuit is operated in a resonant mode similar to a series resonant or LLC converter [27]–[30], the lack of regulation allows operation like that in "DCX" unregulated isolated DC-DC converters such as [37]–[43]. As in some DCX designs, the primary side switching voltage ideally matches the secondary side switching voltage when reflected through the transformer, such that no substantial passive components are needed to buffer between different voltages or switching patterns, and a very small leakage inductance is adequate to shape the current waveform and achieve approximate ZCS operation in the secondary half bridge. The characteristic impedance of the resonant circuit, the total secondary referred leakage inductance (L_{lkg}) and the output capacitors (C_{out}), can be much smaller than the load impedance. This is in contrast to a typical series resonant converter where the tank impedance is at least on the same order as the output impedance and typically several times larger.

As in both LLC and DCX converters, zero-voltage switching (ZVS) is achieved in the primary half bridge by introducing a small carefully controlled deadtime in conjunction with a finite magnetizing current. The required peak magnetizing current ($I_{mag,peak}$) to achieve ZVS during the switching transient is a function of the input side power switches' output capacitance ($C_{pri,out}$), deadtime (t_{dead}), and the peak of the input line voltage (V_{peak}).

$$I_{mag,peak} = 2C_{pri,out}\frac{V_{peak}}{t_{dead}} \tag{1}$$

Because of the back-to-back power semiconductors (drain-to-source diode voltage blocking functionality is disabled), it is possible for the switching node voltage to be overcharged in the opposite direction. Thus, it is important to ensure that the deadtime matches closely to the transition time; too much deadtime would cause hard switching and could possibly overvoltage the semiconductors. During testing of the prototype, the deadtime was finely adjusted to ensure this.

To achieve ZCS for the secondary side switches and near-ZCS for the primary, the output capacitors are tuned to drive the current through the secondary terminals to zero, and the current through the primary terminals to the I_{mag} before the switching event. Thus the output capacitor values are selected based on matching the resonant frequency to the switching frequency.

$$f_{sw} = \frac{1}{2\pi\sqrt{2L_{lkg}C_{out}}} \tag{2}$$

If the capacitance value selected based on resonance achieves a low enough output ripple voltage, no additional output capacitance connected across the load is needed. Additional output capacitance could be used to reduce the output ripple voltage, or in the case that a larger leakage inductance led to a smaller resonant capacitor value, such that C_{out} didn't provide adequate output filtering.

The ability to use only a small leakage inductance allows using a transformer design optimized for low AC resistance without needing to make any compromises to achieve higher leakage [44].

B. Hardware Implementation

GaN devices were selected as the power switches, as they generally achieve faster switching, lower on resistance, and smaller size than their silicon counterparts [45].

The transition time for ZVS was selected as 100 ns. During testing the deadtime was altered slightly to ensure that ZVS was fulfilled during the peak input voltage condition. Using (1), with the selected input GaN devices, $I_{mag,peak}$ was calculated as 370 mA and L_{mag} was calculated to be about 570

μH ($V_{peak}/(8I_{mag,peak}f_{sw})$). Unlike in SST1, the magnetic component does not have to process any large low-frequency content. A full litz-wire design then is preferred to ensure low resistance at the desired frequency.

Following the litz-wire selection outlined in [35], Fig. 8, shows the cross section of the designed transformer. The primary turns were split and wound on both sides of the secondary winding to reduce the leakage inductance. The secondary windings were also selected to have a larger number of strands (as shown with a larger diameter in Fig. 8) to balance the conduction losses on both the primary and secondary windings. Table III lists further details for transformer construction.

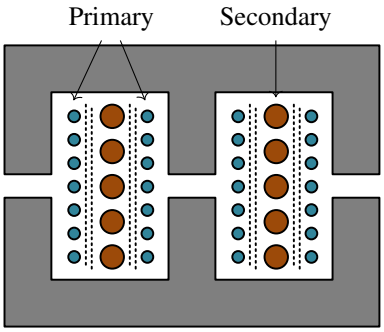

Fig. 8: Simplified cross-section of the designed transformer for SST2. The primary winding (blue) and secondary winding (red) are separated by polypropylene tape (dashed lines)

Description	Value
Core Material	N95
Core Geometry	RM8
Pri. Winding	35 turns 100/AWG46
Sec. Winding	7 turns 330/AWG46

TABLE III: SST2 transformer specific parameters

As for achieving the near-ZCS condition, the total leakage inductance referred to the secondary was measured after the construction of the transformer as 180 nH and using (2) the output capacitance was calculated to be around 7 μF; SST2 was constructed without the use of C_{load} resulting in a output voltage maximum ripple of 800 mV (in this case, worst case ripple voltage is approximated as $I_{out,peak}/(4f_{sw}C_{out})$). However, during operation the output capacitor value was tuned to achieve ZCS at the selected switching frequency.

Table IV outlines the final system parameters for SST2.

V. Experimental Verification

A. Efficiency

The performance of both converters is compared with LFT measurements from [4] in Fig. 10. Note the efficiency improvement especially across the lower load conditions; SST1 shows an improvement of 18.6% at 5 VA compared to the LFT measurements; SST2 an improvement of 30%. SST1 reaches a peak efficiency of 88.6%, SST2 a peak of 96.6%, compared to the LFT's average peak efficiency of 84.4%.

Symbol	Description	Value
f_{sw}	Switching Frequency	100 kHz
V_{in}	Input Voltage	120 VAC
V_{out}	Output Voltage	24 VAC
P	Rated Power	40 VA
	Pri. Switches	EPC2054
	Sec. Switches	EPC2052
L_{mag}	Mag. Inductance	570 μH
L_{llk}	Sec. Leak. Inductance	180 nH
C_{in}	Input Capacitance	2 μF
C_{out}	Output Capacitance	7 μF

TABLE IV: SST2 system parameters and final measured component values

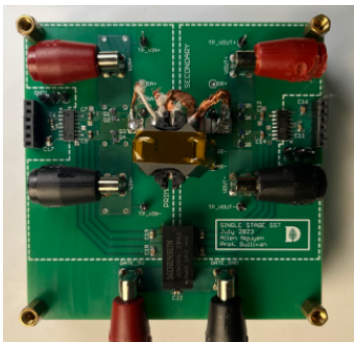

Fig. 9: Prototype SST2

Overall, the efficiency of SST2 is greater than both SST1 and the LFT's average, as the two stage design of SST1 introduces cascade losses from the COTS supply; the COTS offered a peak efficiency of 90.8% as shown in Fig. 11 when the two stages' efficiencies are separated.

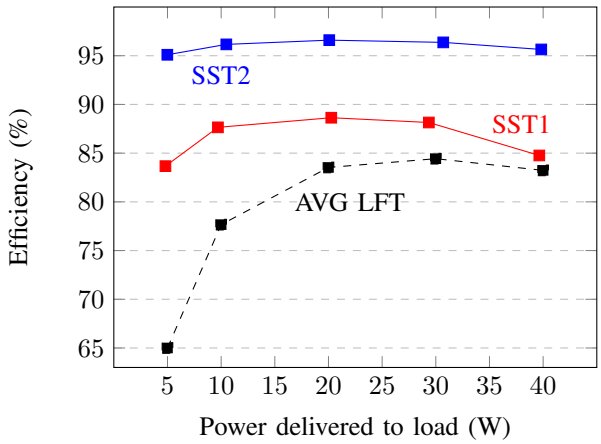

Fig. 10: Efficiency of SST prototypes compared to average LFT data from [4]

B. Power Loss

Fig. 12 shows the power loss across all load conditions. With the Class 2 LFT average standby loss measuring 2.8 W [4], SST1's measured standby loss is 14.9% of that, and SST2's is 7.3%.

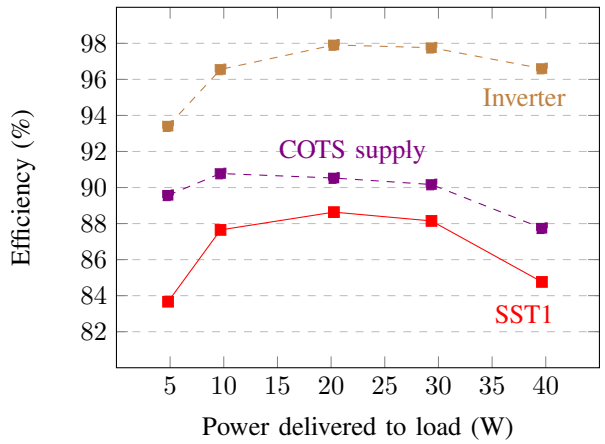

Fig. 11: Efficiency of SST1, separated into the first (COTS supply) and second stage (DC-AC), the second stage achieved a peak efficiency of 97.9%

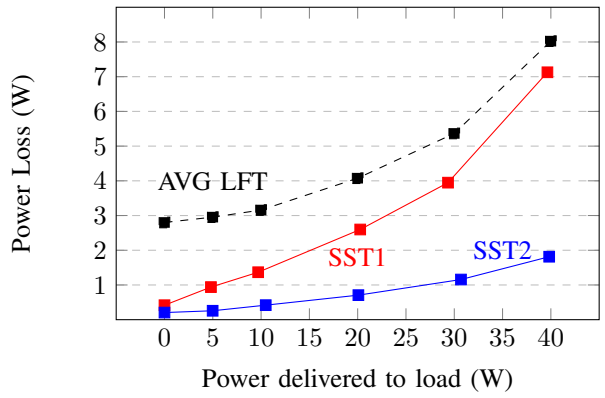

Fig. 12: Power loss of prototypes compared to average LFT data from [4]. SST1 has a standby loss of 417 mW, SST2 a standby loss of 205 mW, and Class 2 LFTs an average standby loss of 2.8 W

Estimated power loss breakdowns of SST1 and SST2 at no-load are shown in Fig. 13 and Fig. 14. Both highlight several areas for future improvements. SST1's standby loss is dominated by the switching loss, while SST2's standby loss is dominated by core loss. Given the excellent full load efficiency of SST2, it will be possible to re-balance core and winding losses in the transformer design to reduce core losses with a modest but acceptable penalty in full-load efficiency.

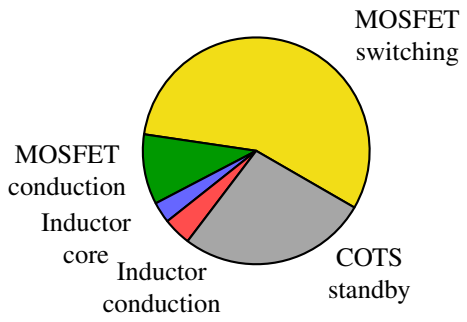

Fig. 13: Estimated standby power loss breakdown of SST1

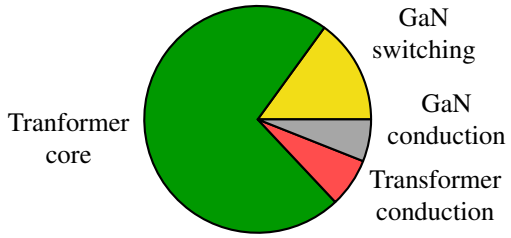

Fig. 14: Estimated standby power loss breakdown of SST2

C. Output Voltage Variation

Another advantage the SST prototypes have is stable output voltage with load variation. Fig. 15 shows the variation in voltage from the open-circuit voltage for different loads. The large variation shown by Class 2 LFTs, 12% of the open-circuit voltage at full load, requires loads to tolerate wide voltage ranges. The prototype SSTs provide an output voltage variation less than 6% across load variation.

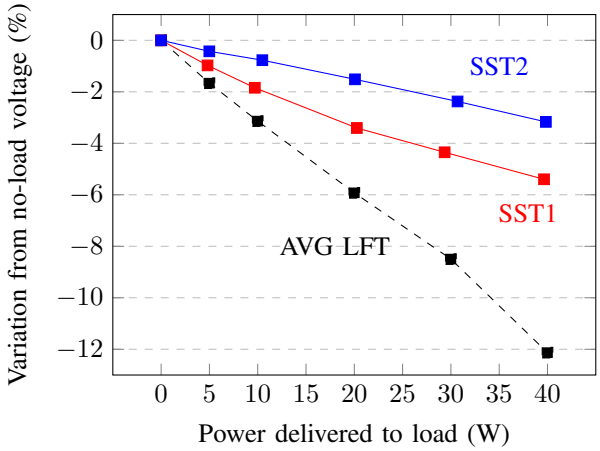

Fig. 15: Variation from open-circuit voltage over varied load current

D. Waveforms

Lastly we present images of the switching waveforms produced by SST2. Fig. 16 shows operation in the no-load condition. The primary transformer current (I_{pri}) is shown to swing to the designed magnetizing current, while the primary ($V_{SW,pri}$) and secondary ($V_{SW,sec}$) side switch node shows ZVS at the peak voltage condition.

Fig. 19 zooms in on the turn on transient. The only current in the leakage inductance during the switching transient is the magnetizing current and thus ringing is minimized without the need for snubber circuits.

Fig. 17 shows the switching waveform during full rated load. The primary current is shown to swing down to the magnetizing current before the switching transient, reducing secondary side ringing as shown in the secondary side switch node waveform (Fig. 20). The primary side switch node shows ZVS at the peak voltage condition.

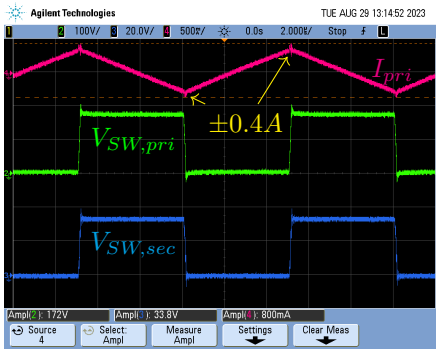

Fig. 16: Switching waveforms of SST2 with no load and at the peak of the input voltage line cycle

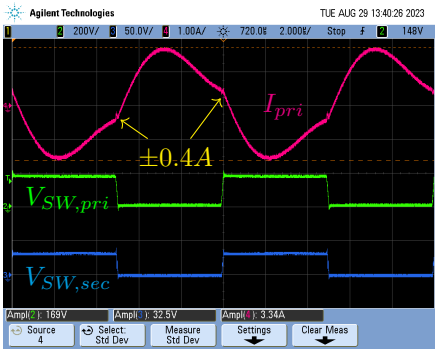

Fig. 17: Switching waveforms of SST2 with full load and at the peak of the input voltage line cycle. The primary side current through the transformer is shown to swing down to the designed magnetizing current for ZVS

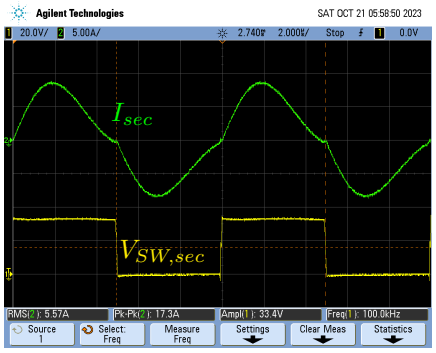

Fig. 18: Secondary side current (I_{sec}) of SST2 with full load and at the peak of the input voltage line cycle. I_{sec} is shown to swing down to zero before the switching transient, achieving ZCS

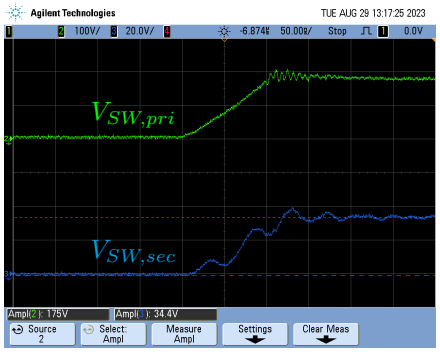

Fig. 19: Rising transient of SST2 with no load and at the peak of the input voltage line cycle

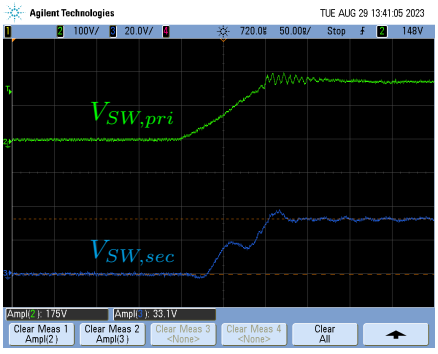

Fig. 20: Rising transient of SST2 with full load and at the peak of the input voltage line cycle

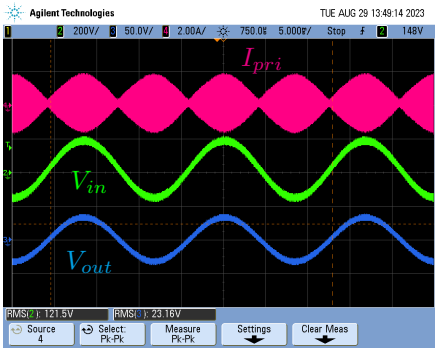

Fig. 21: 60 Hz cycle waveforms of SST1 during full load

Fig. 18 highlights ZCS on the secondary side, and lastly, Fig. 21 shows the full waveforms of three 60 Hz cycles.

VI. Conclusion

Line-frequency Class 2 transformers are found in many applications, and with an average of 2.8 W of standby loss, we see terawatt-hours of energy lost yearly across the U.S. alone. In this work we propose two solid-state transformers that achieve a standby loss 7–15% that of the standard line-frequency transformers, while also achieving high efficiencies across all load ranges. Although this result is already a huge improvement over the line-frequency transformers used now, we have also identified opportunities to further improve the performance of these designs.

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