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A New Power efficient, wide-range PWM-based MPPT circuit for Ultra-low Power Energy Harvesters

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***Abstract*—This paper presents a Pulse Width Modulation (PWM)-based Maximum Power Point Tracking (MPPT) approach suitable for low-power DC energy harvesting systems. A wide-range, low-power PWM scheme is achieved by incorporating one half-circuit of a single thyristor delay element. The proposed Thyristor-based PWM circuit achieves a wide duty cycle range of 2% to 60% while consuming 23nW to 80nW, making it an energy-efficient solution for various applications. The energy harvester attains a peak tracking efficiency of 99.9% and above 99% for a wide input power range. An integrated Power Change Detector (PCD) is proposed, which saves power by activating the MPPT circuit only when needed, reducing power consumption to 125nW. The performance is verified through simulation using 65nm CMOS technology.**

***Keywords*—PWM, Thyristor, MPPT, Energy Harvesting, Boost Converter, Tracking Efficiency, Power Change Detector.**

I. Introduction

In the Internet of Things (IoT) applications, including biomedical contexts and healthcare settings, wireless sensor nodes often rely on ambient energy sources such as photovoltaic panels and thermo-electric generators [1]. Minimizing power consumption and optimizing harvested energy utilization is essential for extending the lifespan of IoT devices [2]. Optimizing ambient energy harvesting can significantly extend battery life or support battery-free sensor nodes in IoT devices. Inductor-based harvesters, such as boost converters for low-voltage sources, provide high efficiency to fulfill IoT energy needs [3]. Fig. 1 shows a Discontinuous Conduction Mode (DCM)-operating boost converter energy harvester that uses MPPT and gate-driver circuits to match the impedance of the converter and energy source, enabling maximum power transfer and improved efficiency in low-voltage energy harvesting. PWM is an effective approach for implementing MPPT in power converters; By modifying the duty cycle, MPPT circuits optimize power extraction through impedance matching between the converter and energy source. PWM allows precise duty cycle control to adapt to varying input power, with many studies proving its efficacy for MPPT [4]–[6]. Different PWM topologies have been suggested in the literature for various applications, including energy harvesting. Analog PWM is a common technique in this field [5], [7]–[9]; It involves comparing an analog reference voltage to a periodic ramp signal using a static comparator, which enables amplitude-to-time domain conversion for PWM generation. However, this approach is power-inefficient due to the continuously

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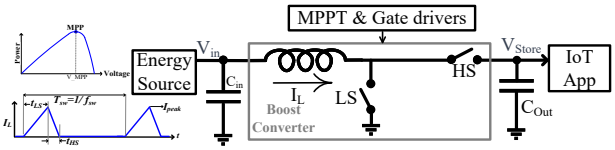


Fig. 1: Generic block diagram of an energy harvester with MPPT, and inductor current waveform.

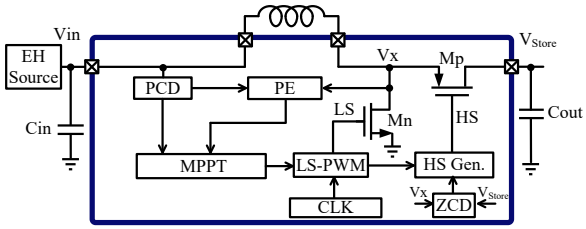


Fig. 2: Proposed energy harvesting system architecture.

active comparator and the need for large capacitors to generate wide pulses. Counter-based PWM, a digital alternative to analog PWM, uses an n-bit counter to compare a generated ramp waveform with a digital code [10], [11]. This approach ensures input code and duty cycle linearity but increases power consumption due to higher clock frequencies. A tapped delay line-based PWM offers an alternative to counter-based PWM without the need for high clock frequency [12]–[15]. This architecture uses 2^n cascaded delay elements and a 2^n-input multiplexer to select different outputs of the delay cells which is suitable for low-power applications such as energy harvesters [16]–[18]. However, it demands a distinct delay cell for each delay increment/decrement, increasing complexity and power consumption, and is susceptible to linearity issues and PVT variations due to stage variations.

We propose an efficient PWM circuit using half of a single thyristor delay element, achieving a wide duty cycle range, low power consumption, linearity, and robustness against variations. The proposed PWM circuit is utilized in the proposed energy harvester (Fig. 2) to modulate the charging time of the inductor (t_{LS} in Fig. 1) through hill-climbing algorithm, thereby performing MPPT [19], [20].

In [20], circuits related to MPPT are turned off when a maximum power point is reached. This action conserves energy and prevents fluctuations around the maximum power point. However, in these scenarios, an external, periodic trigger is required to restart the MPPT circuit for the purpose of tracking variations in input power [21]. The unpredictable nature of ambient energy necessitates a quick MPPT trigger to keep up with input power changes, which can lead to higher power losses. To counter this issue, we have proposed

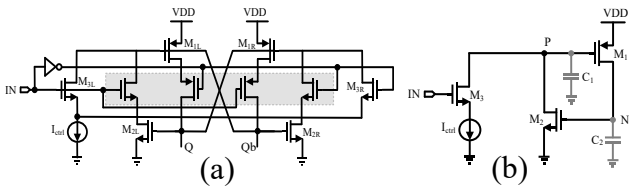


Fig. 3: (a) Thyristor-based delay element [22].(b) Core part of CMOS thyristor delay element

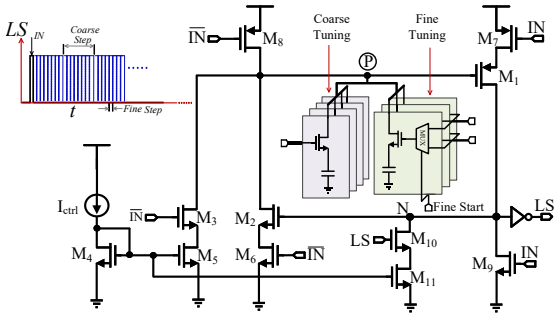


Fig. 4: Proposed LS-PWM.

an integrated power change detector (PCD) circuit that has the capability to trigger the MPPT circuit in response to unforeseen input power variations.

II. System Architecture

The proposed system architecture, as illustrated in Fig. 2 comprises a boost converter, Power Change Detector (PCD), MPPT, power estimator (PE), and low-side (LS) / high-side (HS) generation units. The LS generator is PWM-based, and the HS generator operates based on zero current detection (ZCD). The method proposed in this design involves utilizing the proposed LS-PWM circuit to control the charging time of an inductor (t_{LS}) for MPPT purposes. Therefore, t_{LS} is perturbed through the hill-climbing algorithm performed by the MPPT circuit ([19], [23]). The t_{LS} adjustment occurs in coarse and fine phases. Coarse perturbation is used at the beginning of the MPPT process to maintain tracking speed, while fine perturbation is applied in the second tracking phase to ensure high tracking precision. Implementing the proposed wide-range, low-power PWM circuit (also referred as LS-PWM in this work) allows for high tracking efficiency across a broad input power range.

To conserve power and address the issue of Maximum Power Point (MPP) fluctuation in the hill-climbing algorithm, the MPPT circuit operates in two modes: active and sleep; when MPP is achieved the MPPT-related circuits are automatically powered off. For MPPT re-activation, the system has two triggering mechanisms; an external periodic trigger and a PCD-generated trigger. In case of unpredictable, fast input power change, PCD sends a trigger to activate the MPPT-related circuitries. The PCD circuit's detection of faster input power changes allows the external trigger to be set to a slower rate, resulting in significant power savings. The ZCD circuit prevents inductor reverse current by controlling the HS generator [1]. The proposed design uses a precise current sensor [24] to monitor the inductor's peak current for

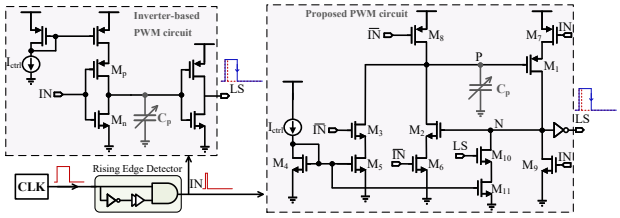


Fig. 5: Comparison setup of the proposed PWM with Inverter-based PWM

the purpose of power measurement, ensuring optimal tracking performance [23], [25].

A. LS-generator (LS-PWM)

The core part of the proposed PWM-based low-side generator (LS-PWM) circuit is a half-circuit of a thyristor-based delay element. Thyristor delay elements were used in microscale energy harvesters due to their power-efficient operation. [28] and [29] reported using thyristor-based Voltage Controlled Oscillators (VCOs) in charge pump-based energy harvesters. As shown in Fig.3(a), thyristor-based delay elements have two half-circuits, each delaying an input pulse's rising or falling edge, generating a delayed output [22]. The left half-circuit manages the rising edge, while the right half-circuit addresses the falling edge. Thyristor devices are designed to trigger upon reaching a specific conduction threshold. Thyristor-based delay components use a positive feedback mechanism to facilitate this process, involving a capacitor that gradually charges or discharges. When the voltage threshold is reached, charging or discharging accelerates due to the positive feedback mechanism. Fig. 3(b) displays the core circuit of a thyristor-based delay element. When point "P" charges to V_{DD} and point "N" discharges to ground, the thyristor (comprising M_1 and M_2) turns off. As the input signal "IN" transitions, node "P" discharges through control current I_{ctrl}. When voltage at node "P" falls below $VDD - V_{thp}$, M_1 activates, turning on and causing node "N" to charge and node "P" to discharge to ground. The discharge of node "P" starts slowly but speeds up due to the positive feedback mechanism in the loop formed by M_1 and M_2. This rapid state transition during turn-on operation minimizes dynamic power consumption, making thyristor-based delay elements ideal for low-power applications. The delay value of this circuit is

$$t_d = \frac{C_1.V_{thp}}{I_{ctrl}} + \sqrt[3]{\frac{6.C_2.C_1^2}{\kappa.I_{ctrl}^2} \cdot V_{thn}} + \delta t \tag{1}$$

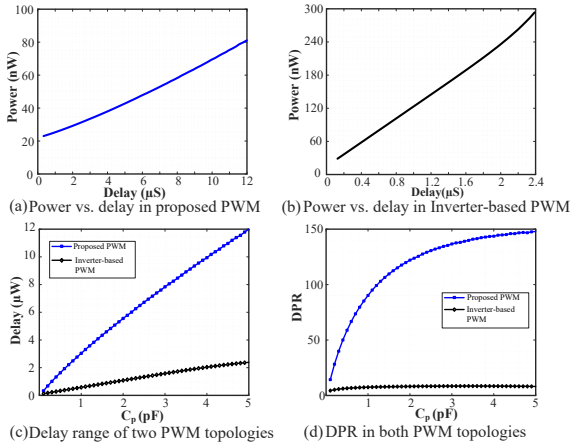
Where

$$\kappa = \mu_p.C_{ox}.\frac{W}{L} \tag{2}$$

and δt represents the regeneration time associated with the positive feedback mechanism in a CMOS thyristor. In (1), δt is the only term dependent on VDD, but its contribution is negligible compared to other parameters. Equation (1) shows a linear relationship with C_1 [22], confirmed in simulation results, making C_1 suitable for linear delay adjustment. Using a modified half-circuit thyristor delay cell, a wide-range low-power PWM circuit is introduced to leverage this property

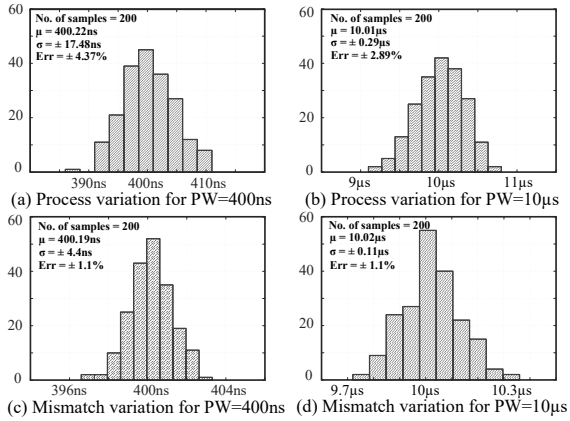
TABLE I: Comparison of PWM structures

	[16]	[26]	[27]	[11]	This Work
PWM Topology	Delay-Line based	Digital PWM	Inverter-based + Digital	Digital PWM	**Proposed LS-PWM**
Duty-Cycle Range	75% - 87.5%	N/A	40% - 85%	1% - 99%	**2% - 60%**
Switching Frequency	100 KHz	1 MHz	10 KHz	30 KHz	50 KHz
Power Dissipation	800 nW	450μW	370 nW	170 μW	23 nW - 80 nW
Process	180nm	350nm	180nm	180nm	65nm



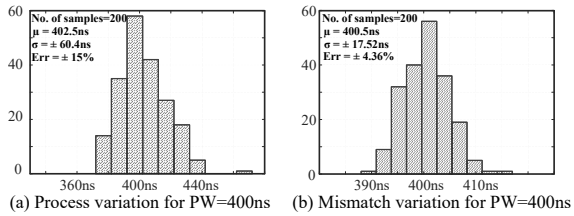
(a) Power vs. delay in proposed PWM (b) Power vs. delay in Inverter-based PWM
(c) Delay range of two PWM topologies (d) DPR in both PWM topologies

Fig. 6: Simulation results of the comparison setup in Fig. 5.



(a) Process variation for PW=400ns (b) Process variation for PW=10µs
(c) Mismatch variation for PW=400ns (d) Mismatch variation for PW=10µs

Fig. 7: Monte Carlo simulation results of the proposed LS-PWM.



(a) Process variation for PW=400ns (b) Mismatch variation for PW=400ns

Fig. 8: Monte Carlo simulation results of Inverter-based PWM.

(Fig.4). This circuit aims to adjust the falling edge delay of a narrow pulse for PWM. Transistors M_1 and M_2 form a thyristor structure, and an adjustable capacitor array at point P discharges with a copy of I_{ctrl} through the current mirror formed by M_4 and M_5. Within each clock period, transistors M_8 and M_9 precharge and discharge points "P" and "N". The proposed PWM circuit, shown in Fig.4, offers extensive delay range and low power consumption which makes it suitable for ultra-low power applications. To evaluate the proposed LS-PWM, we implemented an inverter-based PWM circuit using an "Inverter-based delay element," common in low-power applications [18], [27], [30] (Fig. 5). This delay element combines the advantages of current-starved inverter (CSI) and shunt-capacitor inverter (SCI) techniques, balancing power consumption, delay linearity, and robustness against process variation. We implemented an inverter-based PWM circuit to introduce a delay in the falling edge of a narrow input pulse "IN" (Fig.5) and compared it to our proposed PWM circuit. We observed the delay in the output pulse's falling edge and power consumption (Fig.6) for both setups. Identical supply voltage, control current, and an input pulse frequency of 50 kHz were used. Capacitor C_p varied from 50 fF to 5 pF in both circuits. The proposed circuit exhibited a significantly higher Delay-to-Power Ratio (DPR) than the inverter-based circuit, especially for long delays. Although the proposed PWM's DPR is comparable (nevertheless higher) to the inverter-based PWM's DPR for low delay values, it outperforms the inverter-based PWM in robustness against process and mismatch variations. This makes it suitable for low-power applications requiring a wide range of PWM adjustments. Monte Carlo simulations were conducted to assess the proposed LS-PWM circuit's robustness and performance against process and mismatch variations (Fig. 7). The circuit demonstrated reliability and maintained performance despite the variations, with pulse width errors of approximately ±4.37% and ±2.89% for pulse widths of 400 ns and 10 µs, respectively, with a mismatch variation of approximately ±1%. Monte Carlo simulation of the Inverter-based PWM showed 3-4 times greater errors for a 400ns pulse width(Fig. 8). The proposed PWM circuit performs coarse and fine perturbations required by the MPPT algorithm using pulse width modulation in coarse and fine steps (Fig. 9). With a switching frequency of 50kHz, the pulse width ranges from 400ns to 12μs, achieving a duty cycle range of 2% to 60% while consuming 23nW to 80nW. Table I compares the proposed PWM circuit with other state-of-the-art PWM circuits, mostly used in energy harvester systems. The table shows that the proposed LS-PWM circuit exhibits an extensive operational range while maintaining minimal power consumption.

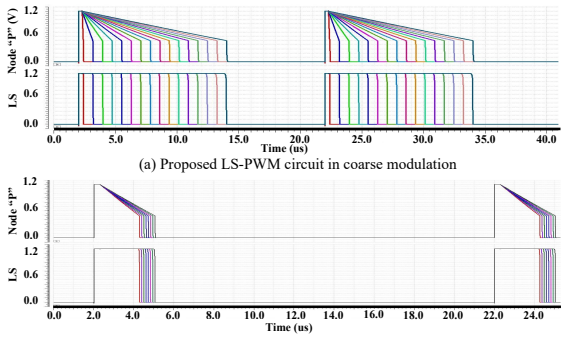
B. Power Change Detector (PCD)

Fig. 10 shows the proposed integrated PCD circuit, consisting of a switched-capacitor low pass filter (SC-LPF), two unbalanced latch-based comparators (offset introduced), and some digital gates and delay elements. The circuit uses two input paths, with the original Vin applied to comparator B and a slowed-down version of Vin fed to comparator A after passing through the SC-LPF. Under steady-state conditions, when the circuit operates at the maximum power point and input power (Pin) is constant, Vin and $SlowVin$ are equal, generating no $Tracking-Trigger$ (TT) signal. A TT signal is generated when the voltage difference between $Slow\ Vin$

TABLE II: Comparison of the whole system

	[31]	[21]	[32]	[11]	[33]	[34]	[7]	[35]*	This work*
Converter Type	Buck-Boost	N/A	CP	Boost	Boost	Boost	Buck-Boost	Boost	**Boost**
Process	150nm	180nm	65nm	180nm	350nm	180nm	180nm	180nm	**65nm**
Source	General	PV	PV&TEG	PV	PV	TEG	General	PV	**PV&TEG**
Peak MPPT Eff. (%)	94.6%	99.7%	96.2%	94.2%	99.9%	98%	98%	N/A	**99.9%**
Pin Range (W)	200μ - 50m	N/A	N/A	N/A	0.6m - 1	N/A	33μ - 1.2m	200μ - 20m	**0.5μ - 4m**
Vin Range (V)	60m - 5	0.53 - 2.51	0.4 -1.7	N/A	N/A	50m - 500m	2 - 7.2	100m - 1.5	**20m - 1.5**
MPPT Method	AIB-MPPT	HC	HC	HC	SRE-FOCV	CEPE	P & O	ET-FOCV	**Modified HC**
MPPT Power (W)	35μ	25μ	5.1μ	19μ	0.792μ	6.12μ	9μ	N/A	**125n**
MPPT Automated On/Off	None	Only Off	None	Only Off	None	None	None	None	**On & Off**

* Simulation-based



(a) Proposed LS-PWM circuit in coarse modulation

(b) Proposed LS-PWM circuit in fine modulation

Fig. 9: Pulse width modulation of the proposed LS-PWM

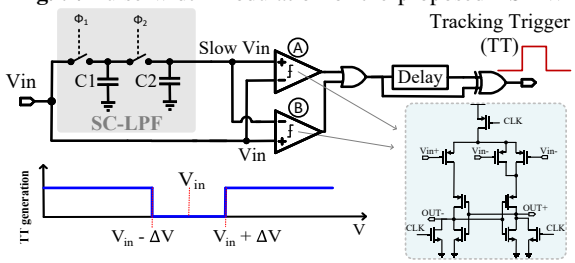


Fig. 10: Power change detector (PCD) for automatic MPPT activation.

and Vin surpasses $\pm\Delta V$, which is the offset voltage introduced by the comparators. When input power changes and consequently Vin deviates from $SlowVin$, either comparator A or B switches from low to high, producing a TT pulse to activate the MPPT tracking. In contrast to a conventional window comparator using fixed external voltages for upper and lower thresholds, this configuration applies dynamic threshold voltages determined by Vin and the comparators' introduced offset voltage (ΔV). Comparator A sets the upper threshold (Vin + ΔV), while comparator B establishes the lower threshold (Vin - ΔV). A 5mV ΔV is set by incorporating an intentional offset via an extra finger added to the comparators' differential inputs. The PCD circuit generates an MPPT activation trigger but does not participate in tracking. In the PCD circuit, the comparators operate at a lower clock frequency than the harvester's main clock, making it possible to detect input power fluctuations. The clock frequency of the comparators can be adjusted based on the anticipated power change rate for a specific application.

III. System Evaluation

The post-layout simulation results of the proposed MPPT, using a foundry-provided noise model, are presented in Fig. 11. The integrated PCD generates a trigger pulse (TT)

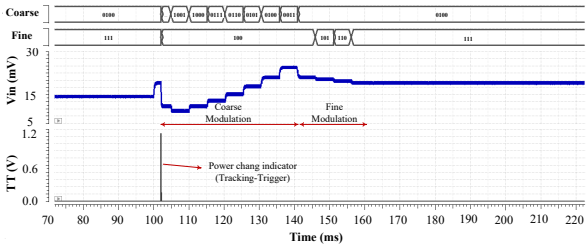


Fig. 11: Post-layout simulation result showing MPPT operation.

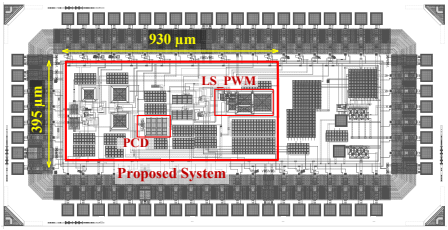


Fig. 12: Proposed System layout.

to activate the MPPT circuit upon detecting input power changes. The tracking process is initiated with coarse and fine steps produced by the proposed LS-PWM. After reaching the Maximum Power Point (MPP), circuits revert to sleep mode. MPPT efficiency data indicate high tracking efficiency (up to 99.9%) across different input power levels. During perturbations, the circuit's peak power consumption is 2.16µW (with P_{in} at 4mW) and 125nW in steady state. The layout of the prototype chip, including the proposed energy harvester, is shown in Fig. 12. Table II compares the proposed system and various state-of-the-art methods in the field. The comparison table shows that the proposed LS-PWM-based MPPT circuit effectively tracks energy sources over a broad power and voltage range, with high tracking efficiency (above 99% for 0.5µ to 4m) and a peak efficiency of 99.9%. Incorporating the proposed PCD and an automated tracking algorithm contribute to the circuit's low power consumption in the steady state.

IV. Conclusion

In this paper, we introduced a highly energy-efficient, wide-range PWM circuit and evaluated its performance both independently and as part of an MPPT system. When integrated within the MPPT circuit, the proposed LS-PWM was the key factor contributing to the high tracking efficiency across an extensive input power range. Furthermore, we presented an integrated PCD that automatically activated the MPPT circuit, leading to significant power savings.

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