A 254 nW 20 kHz On-chip RC Oscillator with 21 ppm/°C Minimum Temperature Stability and 10 ppm Long Term Stability

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***Abstract*—This paper presents a temperature compensated RC oscillator (TC-RCO) designed in 130 nm CMOS technology using regular V_{TH} transistors. The TC-RCO uses constant transconductance (g_m) biasing for first order temperature compensation. Device mismatch based offset correction and delay compensation techniques in the comparator are used to improve temperature instability by cancelling out second order effects. The oscillator achieves a minimum temperature stability down to 21 ppm/°C for a temperature range of -20 to 100 °C. In the lowest power mode, the oscillator consumes 254 nW power from a 1 V supply. The TC-RCO is operated in two modes, a low power mode that consumes an average of 254 nW and a high stability mode that consumes an average of 345 nW. A duty-cycling technique is used to correct offset after four cycles of oscillation. The oscillator exhibits long term stability of 10 ppm after 1 s integration time.**

***Index Terms*—RC Oscillator, ultra-low power, temperature compensation, offset correction, Allan deviation.**

I. Introduction

SINCE its conception, IoT has been touted as the next wave of connectivity with exponential growth prospects. IoT devices spend a large portion of their time in inactive or idle mode to save power while remaining active only for a short duration. To maximize idle time while remaining functional in a larger interconnected IoT network, these systems require a precise clock to synchronize and wake-up the system at regular intervals. An ultra-low power (ULP) oscillator is often used for this purpose. Crystal oscillators are conventionally used as they are able to provide very stable clock while consuming only a few nano-Watts of power [1], [2]. However, crystal oscillators use several off-chip passive components which increases the area and cost of IoT devices. This has increased the demand for ULP, high stability on-chip oscillators. However, realizing highly stable on-chip oscillators require additional compensation techniques as conventional CMOS shows large variation with respect to process, temperature, and voltage (PTV). Further, oscillators also suffer from long-term stability issues such as random walk/run of frequency. Since synchronization is a longer duration activity in IoT devices, a low long-term stability can result in restricted synchronization capability. Typically, on-chip oscillators require high temperature stability, low variation with power supply, and ULP operation, and a higher long term stability.

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This work is supported in part by National Science Foundation (NSF) under grant IIS 2014556, and National Institutes of Health (NIH) under grant HHS/1UF1NS107694-01 (*Corresponding Author: Aatmesh Shrivastava*)

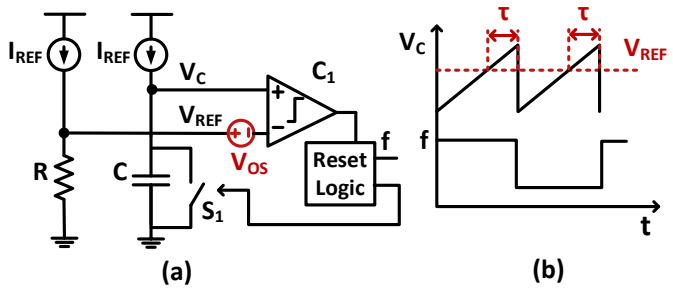


Fig. 1: (a) Conventional RC oscillator topology (b) Timing diagram for conventional RC oscillator

Several methods of generating a stable on-chip oscillator have been reported in literature. These include gate leakage based oscillators [3], [4], RC oscillators [5]–[7], and LC oscillators. LC oscillators are more suitable for high frequency applications to keep passive device sizes practical. The gate leakage oscillators presented in [3], [4] consume lower power, in the pW range, but can only generate frequencies of < 10 Hz. Gate leakage can also show significant temperature variation, hence, transistors with opposite gate leakage temperature coefficients are used for temperature compensation. Moreover, gate leakage does not show high stability against process variations.

RC oscillators can be a better alternative for realizing on-chip oscillators due to their low cost of implementation. However, RC oscillators generally suffer from high frequency variation. This is due to the variability in CMOS process to realize and R and C. Circuit components like resistors and capacitors vary with both process and temperature. Circuit sub-blocks like comparators also suffer from non-idealities which affect the frequency stability of the oscillator. Additional measures are needed to achieve high frequency stability as well as long term stability. Offset compensation of comparators is utilized in [8], [9] to overcome frequency instability resulting from transistor mismatch. In [9], [10], resistors with opposite temperature coefficients are used to cancel out temperature variation of resistance. In [11], a relaxation RC oscillator with a local supply that tracks threshold voltage is presented. The oscillator design in [12] achieves temperature compensation

by cancelling out the CTAT delay of the comparator using polysilicon and diffusion resistors to calibrate the PTAT slope of the RC core. It uses a common gate (CG) topology for comparator design which has lower gain and does not compensate for mismatch in currents. It achieves a lower average stability of 94 ppm/°C and long-term stability of 58ppm.

In this paper, we present an ULP temperature compensated RC oscillator (TC-RCO) with leakage control and offset correction to achieve high frequency stability. The design is carried out using nominal threshold voltage (V_{th}) transistors and a single polysilicon resistor to keep the design cost low. To achieve high frequency stability, the variation in delay of the comparator is made to oppose the variation in circuit components R and C. The 2^{nd}-order temperature compensation is achieved using an n-MOS capacitor as a load to the comparator. Further, the current source mismatch can also impact the stability of the clock source. It can be removed by switching the current source used for biasing V_{REF} [9]. The proposed design also uses same current source for generating the reference voltage and for charging the capacitors, eliminating the current mismatch related issues. It achieves an average stability from 21-49 ppm/°C across 4-chips and a long-term stability of 10ppm. The TC-RCO works in two power modes, and achieves the best long term stability while operating in the high power mode. The paper is organized in the following manner. In Section II, conventional RC oscillators and their limitations are discussed. The TC-RCO circuit design is discussed in Section III. Measurement results are analyzed in Section IV, and Section V concludes the paper.

II. Conventional RC Oscillators

Fig. 1-(a) shows a conventional RC oscillator. It consists of a capacitor being periodically charged and discharged by a current reference. The capacitor voltage rises linearly until it reaches a reference value, V_{REF}. Comparator C_1 trips when V_C crosses V_{REF}, discharging the capacitor through switch S_1. The capacitor voltage waveform is shown in Fig. 1-(b). The frequency of oscillation, f is given by

$$f = \frac{I_{REF}}{2CV_{REF}} \tag{1}$$

where V_{REF} is generated by the voltage drop across a resistor R. Therefore, f is given by

$$f = \frac{1}{2RC} \tag{2}$$

The oscillator design, however, suffers from high process, voltage, and temperature (PVT) variation due to the variation of circuit components, R and C across design corners. The second order effects which give rise to frequency instability are described below.

1) Comparator Offset: The comparator suffers from offset due to the manufacturing related mismatch between the transistors. The input-referred offset, V_{OS} of the comparator affects the frequency of oscillation as follows

$$f = \frac{I_{REF}}{2C(V_{REF} + V_{OS}(T))} \tag{3}$$

The offset resulting from transistor mismatch is a temperature dependent parameter, leading to a temperature instability in the output clock. In [9], [10], [13], the comparator offset is removed to reduce temperature dependency of the output frequency. In [8], self chopping technique is presented to cancel the frequency drift caused by offset. In [9], the comparator polarity is reversed once every cycle to eliminate the offset. In this work, the offset of the comparator is compensated by dividing its operation in two phases. In the offset correction phase, an offset storage capacitor is connected in negative feedback to the comparator input. We divide one of the comparator input into two branches. The amplifier in the comparator self-corrects the offset using its large gain through negative feedback. Compared to the conventional auto-zeroing technique, this technique does not require additional nulling amplifier. The storage capacitor holds the voltage required for zero offset.

2) Comparator Delay: The comparator delay directly adds to the time period of oscillation. Hence, the delay needs to be a small fraction of the time period of the oscillator. The time period T_o of the oscillator is given by,

$$T_o = 2RC + 2\tau(T) \tag{4}$$

where τ is the delay of the comparator. The delay itself is a temperature dependent parameter. It increases with rise in temperature owing to the reduced transistor mobility at high temperatures. Reduction in power consumption of the comparator also increases the comparator delay, making τ an even bigger influence on the output frequency. High power comparators have been used to reduce the delay. In [14], [15] comparator delay is compensated to decrease temperature instability. In [15], the comparator and the digital blocks are designed such that their delays have opposing temperature coefficients. The inherent delay of the comparator has been used for temperature compensation with a CTAT comparator delay design in [12] to achieve a temperature stability of 94ppm/°C. In our TC-RCO circuit, the comparator delay variation is also made to oppose the temperature variation of R and C. However, this is done by biasing the comparator in the sub-threshold region with a PTAT (proportional to absolute temperature) current and loading it with an n-MOS capacitor such that the delay decreases with temperature. A detailed circuit analysis is presented in Section III-C.

3) Resistor and Capacitor Temperature Coefficient: The frequency of oscillation is given by

$$f = \frac{1}{2R(T)C(T)} \tag{5}$$

The variation in circuit components R and C with temperature effects the frequency of the oscillator. In most CMOS technologies, on-chip resistors show a large variation with temperature. In comparison, the temperature coefficient of capacitors is around 35 ppm/°C [16]. In order to cancel the

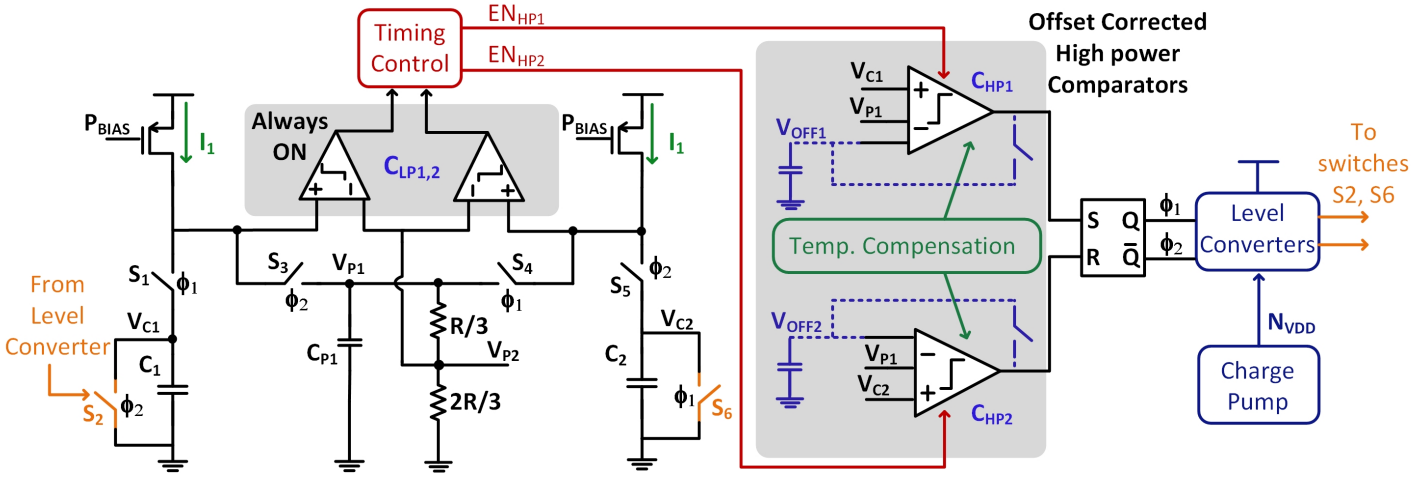


Fig. 2: Temperature Compensated RC Oscillator architecture. Switches S_2 and S_6 are leakage controlled using the negative power supply.

effect of temperature dependence of resistors, two resistors with opposite temperature coefficients have been used. In [5], a polysilicon resistor and a diffused resistor are used which have opposite temperature coefficients. In [9], temperature compensated on-chip resistors are used to remove the linear temperature dependence. In this work, the temperature dependence of the resistor is cancelled by the opposing temperature dependence of the comparator delay. Only polysilicon resistors with a positive temperature coefficient are used in the TC-RCO.

4) Leakage Current: Another important factor that contributes to temperature dependence of the oscillator frequency is the leakage current in the switch S_1 in Fig. 1-(a), especially at high temperatures. The leakage in the switch increases exponentially with temperature. To reduce the power consumption, current references in the nA range are conventionally used, making leakage currents a much larger fraction of I_{REF}. The effect of leakage on period of oscillation becomes worse for lower currents. Several methods to reduce leakage currents have been explored. High V_{th}, thick oxide switches are generally used to reduce switch leakage. A negative body bias can also be used for n-MOS switches to increase the threshold voltage and reduce leakage. However, the process requires triple n-well technologies. Additionally, the increased threshold voltage increases the time it takes for the switch to turn on.

As the power consumption of an oscillator is reduced, the delay and leakage currents both increase, resulting in a trade-off between power and temperature stability. Larger resistors are also required to generate the same V_{REF}, which can often result in a larger area.

III. Temperature Compensated RC Oscillator

Fig. 2 shows the block diagram of the TC-RCO. Two MIM capacitors C_1 and C_2 of 2 pF each are charged and discharged periodically to generate the output clock f_{CLK}. The reference voltage V_{P1} is generated by the same current source that is used to charge the capacitors. The current source is a PTAT source, shown in Fig. 3-(a). In this architecture, transistor M_1 is K-times larger than M_2. The top current mirrors from M_3 and M_4 ensures that $I_{M1} = I_{M2}$ which can be written as,

$$I_{S0}exp(\frac{V_{GS,2} - V_{th,2}}{\eta V_T}) = K \cdot I_{S0}exp(\frac{V_{GS,1} - V_{th,1}}{\eta V_T}) \quad (6)$$

Since $V_{GS,2} - V_{GS,1} = I_{PTAT}R_{CS}$ and ignoring the body effect due to small voltage drop, we can further write the equation as

$$exp(\frac{I_{PTAT}R_{CS}}{\eta V_T}) = K \quad (7)$$

Therefore, the current in each branch of the current source is given by

$$I_{PTAT} = \frac{\eta V_T ln(K)}{R_{CS}} \quad (8)$$

where K is set to be 8, and R_{CS} is 5-bit programmable 6.8 MΩ polysilicon resistor. The current depends on the thermal voltage, V_T to give a PTAT current source. The simulated current waveform is shown in Fig. 3-(b). We use power-up signal, typically provided by the power management unit during power up, to start-up the current source. Fig. 3-(a) also shows the start-up technique. A low-leakage p-MOS transistor, M_{SU} is added between V_{DD} and N_{BIAS}. During power-up, M_{SU} is ON to pull the current source away from its other operating point. However, after power up gate of M_{SU} goes to V_{DD} to turn-off this circuit that takes the current source to the correct operating point. To overcome mismatch related issues for the current source, long and wide transistors were used that were carefully laid out using common centroid matching technique.

To achieve low power consumption, the TC-RCO uses four comparators. The resistor used to generate the reference voltage is split into two to generate V_{P1} and V_{P2}, with $V_{P2} < V_{P1}$. The low power comparators $C_{LP1,2}$ are always on. They are used to detect the capacitor voltages $V_{C1,2}$ crossing V_{P2}. The low power comparator ($C_{LP1,2}$) has higher delay but is set to have an earlier trip point of $2/3 \times V_{P1}$. Once $C_{LP1,2}$ trips, then the higher power comparator $C_{HP1,2}$ is enabled. Since $C_{LP1,2}$ trip point is $2/3 \times V_{P1}$, or $2/3 \times T$ ideally,

$C_{HP1,2}$ is on for $1/3 \times T$. Hence, for a 31.6 kHz clock, the high power comparator is enabled for about 5.27 μs before the V_{C1},V_{P1} trip point. The higher delay of $C_{LP1,2}$ does not impact the clock period due to its early trip point. The power consumption is reduced by utilizing low power comparator for larger duration of the clock period and high-power comparator for smaller duration. However, higher performance is maintained by utilizing $C_{HP1,2}$ when the comparator is expected to trip. The high power comparators $C_{HP1,2}$ trip when $V_{C1,2}$ cross V_{P1}. $C_{HP1,2}$ are disabled when $V_{C1,2} < V_{P2}$ to save power. $C_{LP1,2}$ outputs are fed to the Timing Control block which generates the control signals to enable $C_{HP1,2}$. The Temperature Compensation block and offset correction control the variation of frequency with temperature, and are only used for the high power comparators. The offset correction in the high power comparators is achieved through a negative feedback technique, which is discussed in more detail in Section III-A. The level converter and the charge pump are used to generate a negative bias to control the leakage in switches.

The TC-RCO addresses the nonidealities described in Section II which lead to temperature instability. The oscillator operation is divided into two phases, and is described below.

1) Phase ϕ_1 operation: In phase ϕ_1, switches S_1, S_4, and S_6 are on, and capacitor C_1 is charged from the PTAT current source. Capacitor C_2 is discharged to the ground through switch S_6. Comparator C_{HP2} is disabled during the entire phase. Phase ϕ_1 operation is now further divided into two parts. During $V_{C1} < V_{P2}$ (phase ϕ_{1-A}), low power comparator C_{LP1} is used to compare V_{P2} and V_{C1}. The low power comparator consumes 23 nW power from a 1V supply, and the high power comparator C_{HP1} is disabled. C_{HP1} is enabled once C_{LP1} trips to save power. The Timing Control Block generates the control signal EN_{HP1} to enable C_{HP1}. In the second part of phase ϕ_1 operation (phase ϕ_{1-B}), the comparator C_{HP1} senses the voltage V_{P1}, and trips when V_{C1} crosses V_{P1}. The comparator output sets the SR latch, generating the first phase of the clock, which is fed back to control the switches. By using two comparators, the high power comparator is disabled and consumes no quiescent current in phase ϕ_{1-A}. The leakage current in the high power comparators is 210pA at 25^{o}C. The reduction in power consumption is greater for higher V_{P2} as C_{HP1} is enabled for a shorter duration. In this work,

$$V_{P2} = \frac{2}{3} V_{P1} \tag{9}$$

The offset and delay of the comparator C_{LP1} do not contribute to the clock frequency. The offset of the high power comparator C_{HP1} is compensated in phase ϕ_{1-A} once every four cycles. The delay compensation and offset correction is described in the next section.

2) Phase ϕ_2 operation: Phase ϕ_2 operation is symmetrical to phase ϕ_1 operation. Switch S_3 is now used to generate voltage V_{P1}. Comparator C_{HP1} is disabled in the entire phase, and C_{HP2} is enabled in ϕ_{2-B} ($V_{C2} > V_{P2}$). Similar to phase ϕ_1 operation, the offset of C_{HP2} is compensated once every four cycles during ϕ_{2-A}. The comparator output resets the SR latch, generating the second phase of the clock. The two phase operation of the clock helps in achieving 50% duty-cycle for the clock. The additional comparator pair does not increase the power because only one C_{HP} is active in one phase while the other is off. Further, the two phase operation this way averages the current from two current sources, effectively biasing the resistor and charging the capacitor with same current. This eliminates current mismatch related issue in the clock source.

The PTAT current source is used to charge the capacitors and bias the comparators. The PTAT current also generates reference voltage V_{P1}, which also rises linearly with temperature, ignoring the temperature dependence of the resistor itself. Hence, the frequency of oscillation f_{CLK} is given by

$$f_{CLK} = \frac{I_1}{2C_1 V_{P1}} \tag{10}$$

Since I_1 and V_{P1} are both linearly dependent on temperature, f_{CLK} is independent of temperature. V_{P1} is generated alternatively through switches S_3 and S_4, by the same current sources used to charge the capacitors $C_{1,2}$.

The TC-RCO is operated in two power modes. Since the current generated by the PTAT current source is programmable through R_{CS}, the power consumption and the reference voltage level ($V_{P1,2}$) can be varied. In the low power mode, R_{CS} is set to 12MΩ, with V_{P1} at 110 mV. In high power mode, R_{CS} is decreased, increasing the power consumption. Since V_{P1} is linearly proportional to I_1, varying the bias current does not affect the frequency. $V_{P1} = I_1 R$ and hence, the clock frequency is given by

$$f_{CLK} = \frac{1}{2C_1 R} \tag{11}$$

The simulated waveforms for the TC-RCO are shown in Fig. 4. Table I shows the power breakdown of the TC-RCO sub-circuits in the low power mode. The process variation of the TC-RO can be addressed using conventional calibration methods. The split resistor R can be trimmed without varying the ratio of V_{P1} and V_{P2} to obtain the desired frequency.

A. Offset Correction

The offset of the comparator is temperature dependent, leading to a second order temperature instability. The TC-RCO works in two phases, as shown in Fig. 2. The operation of the oscillator in phase ϕ_1 is described here. The low power comparator C_{LP1} is always enabled. C_{LP1} is a low power comparator with a large delay, which senses the capacitor voltage and compares it with V_{P2}. During this time, the high power comparator C_{HP1} is disabled, saving power. Once the voltage on the C_1 crosses V_{P2}, C_{LP1} trips, and C_{HP1} is enabled. C_{HP1} detects V_{C1} crossing V_{P1}. Since the tripping point and delay of C_{LP1} is not critical to the frequency, its offset is not corrected. Comparators $C_{LP1,2}$ are designed such that

$$V_{P2} + V_{OFF,LP} < V_{P1} \tag{12}$$

where $V_{OFF,LP}$ is the input offset of the comparators $C_{LP1,2}$, and V_{P2} = 2/3V_{P1}.

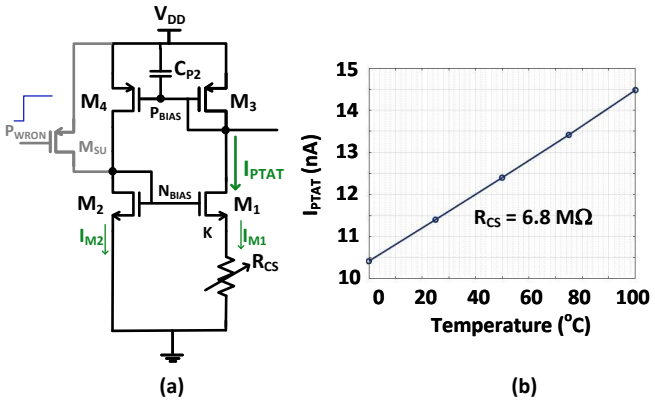


Fig. 3: (a) PTAT current source and (b) simulated current waveform for PTAT current source.

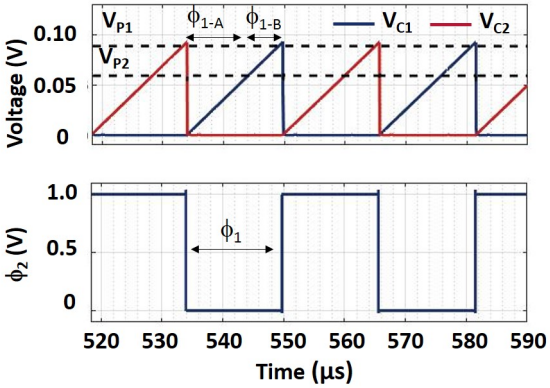


Fig. 4: Simulation results showing charging and discharging of capacitors C_1 and C_2 in the TC-RCO.

The complete schematic of the offset corrected comparator is shown in Fig. 5. The offset of $C_{LP1,2}$ is simulated with process and mismatch variation and is shown in Fig. 6. The resistors generating $V_{P1,2}$ are configurable using 3-bit binary control. For nominal operation, V_{P1} is set to 162 mV, and V_{P2} is set to 108 mV.

The input offset of C_{HP1} is corrected in phase ϕ_{1-A}, when $V_{C1} < V_{P2}$. The negative input transistor of the comparator is split into two parallel transistors with N = 6 and N = 2 fingers. During offset correction, the positive input transistor is connected to V_{P1}, and the offset storage capacitor C_{OFF1} is connected in a negative feedback configuration to the input. When there is no mismatch in the comparator, then V_{OFF1} is equal to V_{P1}. During comparison, the equivalent voltage required for zero output offset is stored on C_{OFF1}. Once C_{LP1} trips, the positive input of C_{HP1} is connected to V_{C1} for comparison. Hence, the offset is corrected before C_{HP1} starts the comparison operation.

In this operation, the high power comparator is enabled during the entire half cycle. This raises the power consumption of the oscillator. To lower the power consumption, the offset is corrected only once every four cycles. During the first three cycles, C_{HP1} is disabled while C_{LP1} is in its comparison phase. It is enabled only in phase ϕ_{1-B}. In the fourth cycle, C_{HP1} is enabled during the entire phase $\phi 1$, for correction, and then for comparison. The control signals to enable $C_{HP1,2}$ are generated by the Timing Control Block, shown in Fig. 7. The simulated control signals for C_{HP1} are shown in Fig. 8.

TABLE I: Power Breakdown of Oscillator Sub-Circuits

Block name	Power (nW)
$C_{HP1,2}$	82
$C_{LP1,2}$	46
Timing Control + Offset correction	66

B. Leakage Currents in Switches

The leakage current in switches increases exponentially with temperature. The leakage in the switches controlling the offset correction operation directly impacts the frequency of oscillation. The capacitors $C_{OFF1,2}$ hold the charge for three consecutive cycles for offset correction. The leakage of switches directly connected to the offset storage capacitor causes $V_{OFF1,2}$ to drift. Fig. 9-(a) shows the drift in the voltage of V_{OFF1} before offset correction is applied with the number of cycles waited for offset correction. Once offset correction is applied, the level of V_{OFF1} comes back to its initial value. It drifts due to leakage and is brought back to its initial level by offset correction circuit. We chose offset correction after every 4-cycles in the final chip implementation. The error increases as the charge is held for increasing number of clock cycles. In the design implementation of the clock, we selected correcting offset every 4-cycles. Offset correction every 16 cycles shows an addition 7mV drift which can drift the output frequency by about 4%. This would result in a slight reduction in energy per operating frequency. Additionally, the device leakage will play a bigger role in determining the output frequency if offset correction every 16-cycles was performed. We chose offset correction every 4-cycles to reduce the impact of leakage current on output frequency.

The leakage in the switches is controlled by providing negative gate voltage during the off time of the switches. The negative voltage is generated using a negative voltage charge pump shown in Fig. 10-(a). The charge pump produces a negative voltage of -200 mV, while consuming 5.8 nW power. The negative voltage is provided to a level shifter to generate voltage swing between V_{DD} and N_{VDD}. The level shifter schematic is shown in Fig. 10-(b). All switch control signals in the offset correction circuit are first fed to level shifters to generate negative V_{GS} to control switch leakage. The level shifters do not carry steady state DC current, and hence contribute little to the power consumption of the oscillator. Simulation shows a power consumption of 1.1nW for the level shifter at 32 kHz frequency of oscillation. The leakage controlled switches are shown in Fig. 5. All switches are designed with nominal V_{th} transistors. Fig. 11 shows the oscillation frequency without the generation of N_{VDD}. The leakage in the switches rises exponentially with temperature, resulting in an increase in frequency.

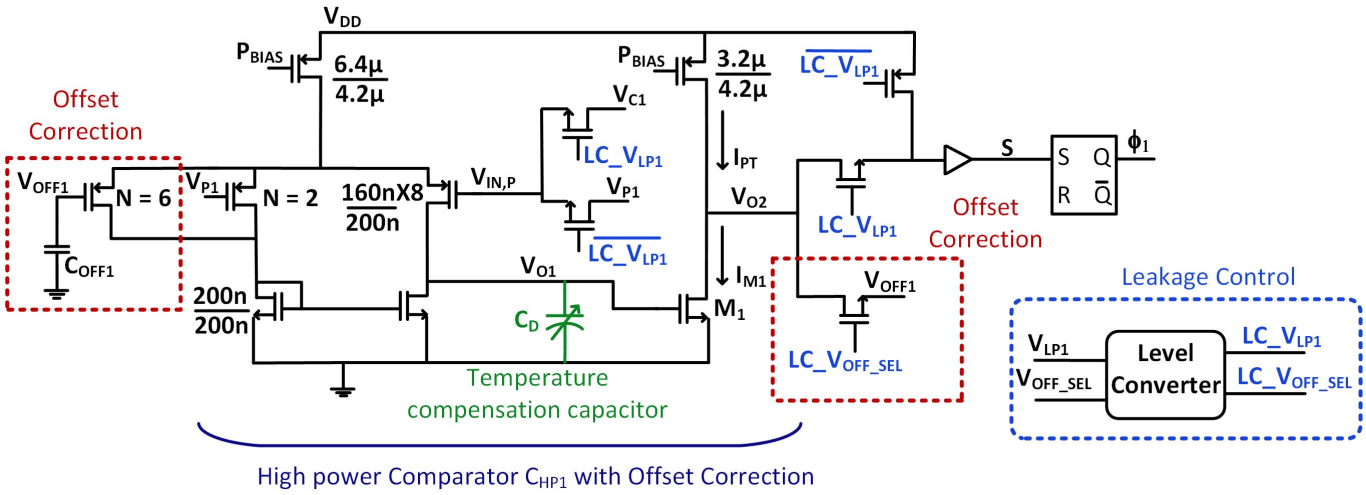


Fig. 5: Offset Correction of high power comparator C_{HP1} in phase ϕ_1.

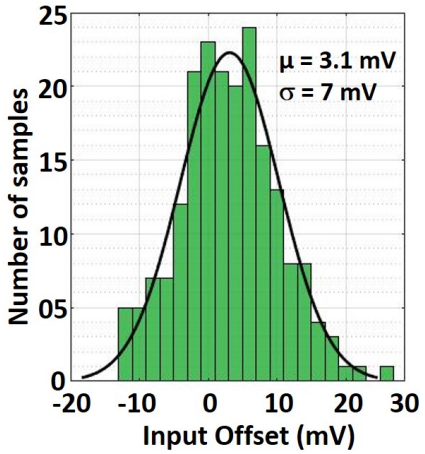


Fig. 6: Monte Carlo simulation showing input offset voltage of C_{LP1} after 200 runs with process and mismatch variation.

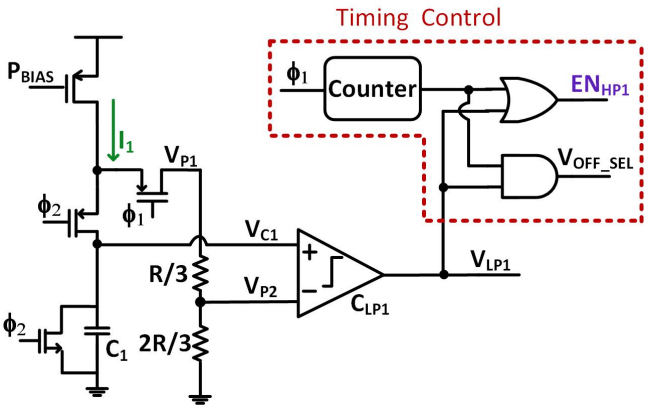


Fig. 7: Schematic of TC-RCO in phase ϕ_1 showing generation of timing control signals to switch on C_{HP1}.

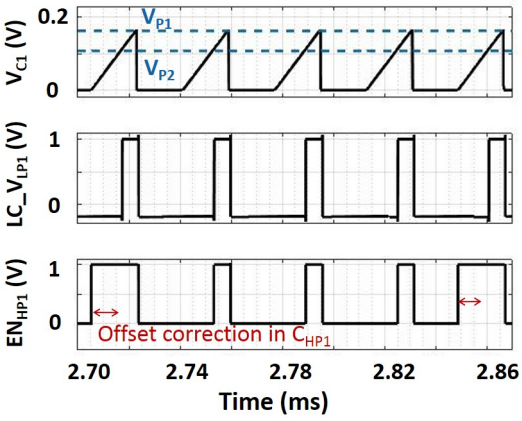


Fig. 8: Simulated waveforms showing offset correction of high powered comparator C_{HP1} once every four cycles.

C. Comparator Delay

The comparator delay directly adds to the time period of the oscillator. Generally, large power comparators are used to make the delay a smaller component of the time period. The delay can degrade the temperature performance of the oscillator as it itself varies with temperature. The low power comparators C_{LP1} and C_{LP2} do not contribute to the time period of oscillation, and the variation in delay with temperature does not effect the overall temperature stability of the oscillator. The low power comparators $C_{LP1,2}$ have a large delay of 834 ns, while the delay is reduced to 210 ns for the high power comparators $C_{HP1,2}$. Since voltage V_{P2} is set to be 2/3 V_{P1}, $C_{LP1,2}$ are designed such that

$$\tau_{LP} < \frac{1}{3}\frac{T}{2} \tag{13}$$

where τ_{LP} is the delay of $C_{LP1,2}$. Hence, only C_{HP1} and C_{HP2} are compensated for delay variation. Fig. 5 shows the schematic of the high power comparator. The comparator is biased with a PTAT current source. Transistor M1 is biased in the sub-threshold region, such that

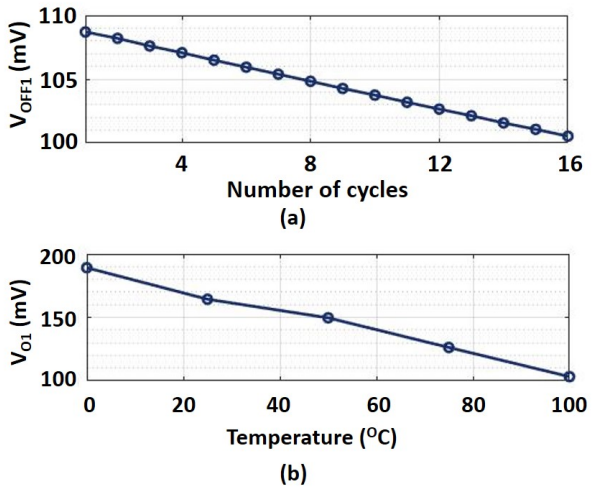


Fig. 9: Simulation results showing (a) drift of voltage V_{OFF1} with number of cycles waited before offset correction and (b) variation of V_{O1} with temperature.

$$I_{M1} = I_S \exp\left(\frac{V_{O1} - V_{th}}{\eta V_T}\right) \tag{14}$$

where I_S is the sub-threshold saturation current, η is the sub-threshold ideality factor, and V_T is the thermal voltage. The comparator trips when $I_{M1} \geq I_{PT}$, and the tripping point of the comparator is calculated as

$$V_{O1} = V_{th} + \eta V_T \ln\left(\frac{I_{M1}}{I_S}\right) \tag{15}$$

2^{nd}-order compensation: We used n-MOS capacitor C_D as shown in Fig. 5 for 2^{nd}-order compensation. Threshold voltage V_{th} decreases with increase in temperature. I_{M1} and V_T both increase linearly with temperature, while I_S increases exponentially. Hence, overall, V_{O1} decreases with temperature, resulting in delay of the comparator also decreasing with temperature. The delay of the comparator thus results in a PTAT response in oscillation frequency.

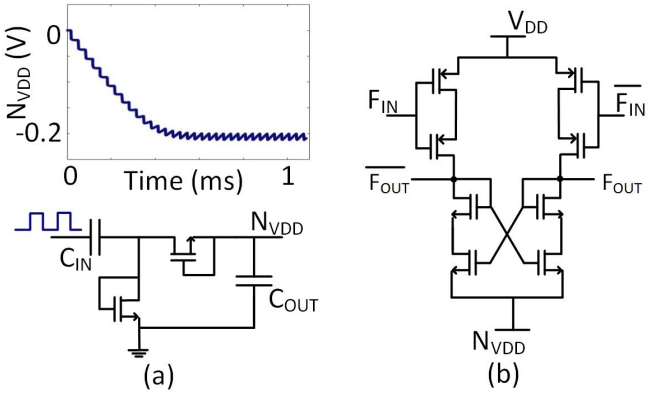


Fig. 10: (a) Negative voltage charge pump (b) Level shifter

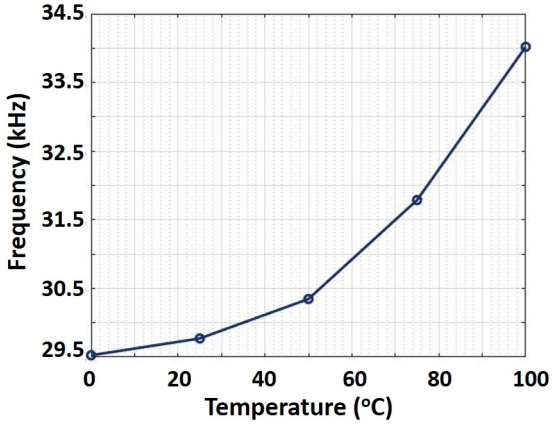


Fig. 11: Simulation showing effect of leakage in switches on oscillation frequency.

The temperature compensation capacitor C_D gets charged by the differential stage current of the comparator as follows

$$\Delta I = C_D \frac{dV_{O1}}{dt} = g_m \Delta V in \tag{16}$$

where Δ Vin = V_{C1} - V_{P1} for phase $\phi 1$ operation. g_m is the transconductance of the differential input pair transistors of the comparator, biased in the sub-threshold region.

V_{C1} itself is charged using a PTAT current source I_1, such that

$$I_1 = C_1 \frac{dV_{C1}}{dt} \tag{17}$$

Once V_{C1} reaches V_{P1}, the comparator trips after delay τ, during which time the capacitor further charges to (V_{P1} + ΔV)

$$\int_{T/2}^{T/2+\tau} I_1 dt = C_1 \int_{V_{P1}}^{V_{P1}+\Delta V} dV_{C1} \tag{18}$$

$$I_1 \tau = C_1 \Delta V_{C1} \tag{19}$$

From Eq. 16 and Eq. 17,

$$\Delta I = g_m \frac{I_1 \tau}{C_1} \tag{20}$$

From Eq. 19 and 20,

$$\frac{g_m I_1 \tau}{C_1} = C_D \frac{dV_{O1}}{dt} \tag{21}$$

Hence, the delay of the comparator is

$$\tau = \sqrt{\frac{2 C_D C_1 V_{O1}(T)}{g_m I_1(T)}} \tag{22}$$

V_{O1} decreases with temperature, as given in Eq. 15, while I_1 rises linearly with temperature. The transconductance of the transistor is constant with temperature as it is biased in the sub-threshold region. Overall, the delay decreases with temperature.

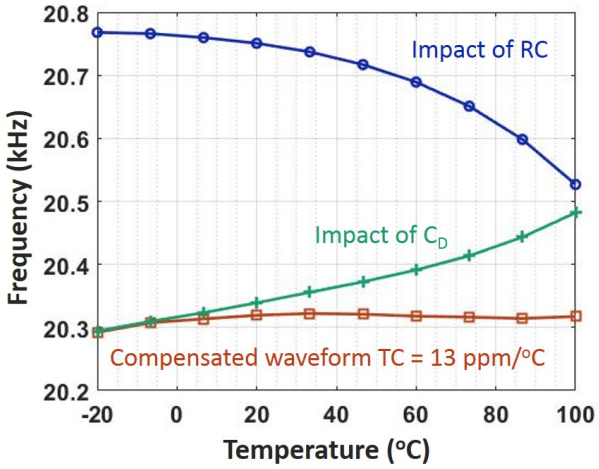


Fig. 12: Simulation showing impact of resistor R and NMOS varactor C_D on oscillation frequency.

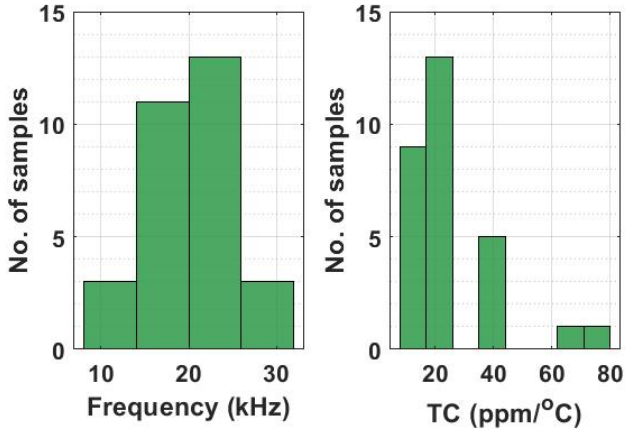


Fig. 13: (a) Simulation showing variation of clock frequency with Monte Carlo global process variation for 30 samples, R = 12.1MΩ. (b) Simulation showing variation of temperature coefficient with Monte Carlo global process variation for 30 points without calibration.

$$\tau = \sqrt{\frac{2C_D C_1 R_{CS}}{g_m V_T ln(K)}} \sqrt{V_{th} + \eta V_T \ln\left(\frac{I_{M1}}{I_S}\right)} \tag{23}$$

The second factor affecting temperature stability is the variation in resistance R and capacitors C_1 and C_2 with temperature. R and $C_{1,2}$ increase with temperature, resulting in CTAT response in oscillation frequency. Since comparator delay and RC variation show opposing temperature coefficients, their effects can be cancelled out with careful design of the comparator. The delay of the comparator is further increased using an additional MOS capacitor C_D at V_{O1} to achieve 2^{nd}-order compensation. The n-MOS capacitor is biased in positive voltage range where capacitance decreases with voltage. With the rise of temperature, PTAT current increases which decreases V_{O1} discussed above, leading to a reduced load at high temperature. While, the additional capacitor increases the delay of the comparator but it introduces a negative temperature component to cancel out the effect of R and $C_{1,2}$. Further, the dependence of delay on V_{O1} as given by eq. 22 requires that the offset of the comparator needs to be corrected. In the presence of offset, V_{O1} will vary randomly which will reduce the effectiveness of the temperature compensation using the comparator delay. Fig. 12 shows the combined effect of delay and RC variation on frequency of oscillation. The opposing effects of RC and n-MOS varactor C_D cancel out, improving temperature stability to 13 ppm/°C in simulation.

Fig. 13-(a) shows the variation in frequency of the oscillator with process Monte Carlo variation, with R = 12.1MΩ. It shows that our mean frequency of oscillation is 20KHz. Fig. 13-(b) shows the variation of temperature coefficient of the TC-RCO with global process variation. The mean temperature stability is 25 ppm/°C. For this simulation calibration is not used which can improve the temperature stability even for worst corners. Fig. 14 shows the simulated result for frequency variation against temperature for different V_{DD}.

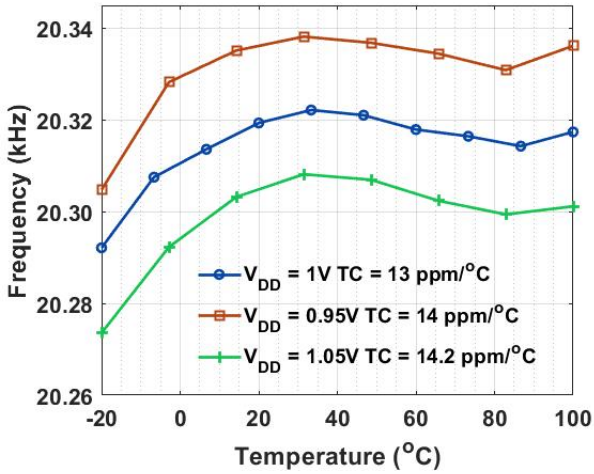


Fig. 14: Simulation results showing variation of frequency against temperature for different V_{DD}.

D. Allan Deviation

Noise sources inherent in the oscillator give rise to Allan variance, or long term frequency instability of the oscillator with respect to time. A method to improve the Allan deviation of the RC oscillator is shown here. As shown in Fig. 2, current I_1 is used to charge capacitors C_1 and C_2. the same current I_1 is also used to generate reference voltage V_{P1}. Hence, the frequency of oscillation is given by $T = 2RC_{1,2}$, which is independent of I_1. However, since $V_{P1} = I_1 R$, the reference voltage level changes with I_1. Period of oscillation is given by

$$T = \frac{CV_{P1}}{I_1} \tag{24}$$

Owing to the noise generated by the circuit, there will be random variation in the time period (ΔT). Referring all the noise generated in the circuit to the reference voltage V_{P1},

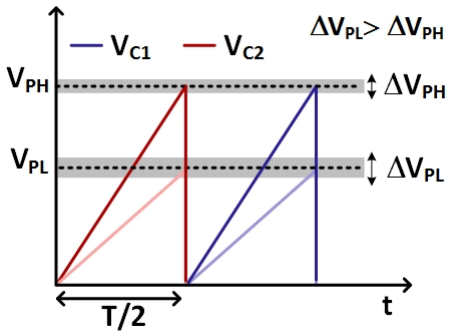


Fig. 15: Clock Period at high power and low power mode with noise.

ΔT is given by

$$\Delta T = \frac{C\Delta V_{P1}}{I_1} \tag{25}$$

where ΔV_{P1} is the noise referred to the reference voltage. Therefore, the error in the time period can be given as

$$\frac{\Delta T}{T} = \frac{\Delta V_{P1}}{V_{P1}} \tag{26}$$

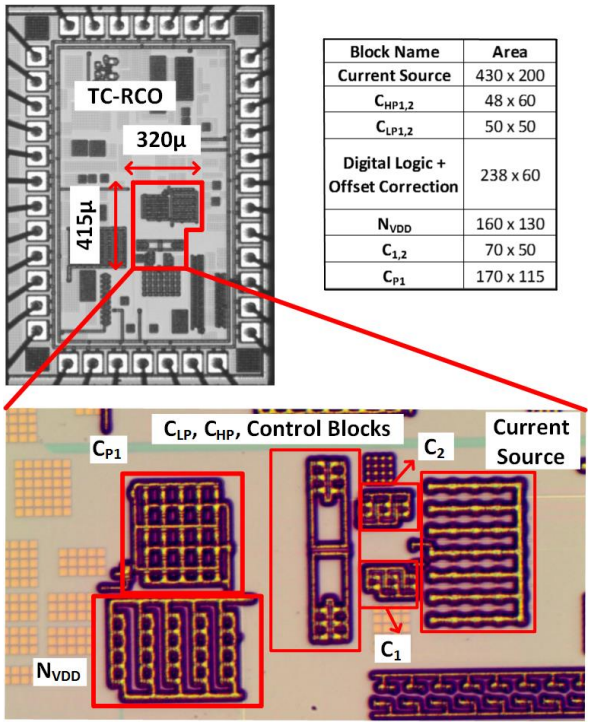
For lower I_1, the circuit produces more noise, which implies $\Delta V_{PL} > \Delta V_{PH}$, where V_{PL} and V_{PH} are the reference voltages for low and high power mode. The low and high power modes differ only in the current value I_1. Comparing the variation in the time period in the low and high power modes,

$$\frac{\Delta T_L}{\Delta T_H} = \frac{\Delta V_{PL}}{\Delta V_{PH}} \times \frac{V_{PH}}{V_{PL}} \tag{27}$$

Hence, the overall randomness around the timing is much lower in the high power mode owing to two factors. First, the higher bias current helps in reducing the input-referred thermal noise of the comparator to reduce overall input noise. Secondly, since the period of oscillation is directly dependent on reference voltage, a higher reference voltage makes noise a lower fraction of the period. These two factors reduce the contribution of noise in the high power mode. This results in a lower Allan deviation in the high power mode. The approach helps in trading off power with long-term instability.

IV. Measurement Results

The TC-RCO was fabricated in 130 nm CMOS process. Fig. 16 shows the die photo, and the area breakdown of the TC-RCO sub-circuits. The total area occupied by the TC-RCO is 415 μm $\times$ 320 μm. The bias current in the high power comparators is also made configurable to effectively cancel out the variation in frequency due to R. The bias current is set only once before the temperature sweep. Fig. 17 shows the variation in frequency with temperature for 4 chips. The four chips achieve temperature stability between 21 ppm/°C and 49 ppm/°C for a temperature range of -20°C to 100°C. Each chip is calibrated only once by configuring the current in the high power comparators to compensate for comparator delay in $C_{HP1,2}$. The same setting is used for the entire temperature sweep.



Block Name	Area
Current Source	430 x 200
$C_{HP1,2}$	48 x 60
$C_{LP1,2}$	50 x 50
Digital Logic + Offset Correction	238 x 60
N_{VDD}	160 x 130
$C_{1,2}$	70 x 50
C_{P1}	170 x 115

Fig. 16: Chip micrograph of TC-RCO.

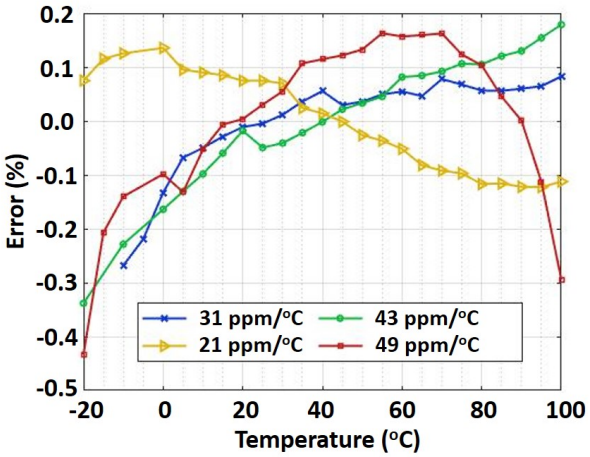


Fig. 17: Variation of frequency with temperature for 4 chips. Each chip is calibrated only once to obtain lowest TC.

The supply sensitivity of the oscillator is shown in Fig. 18-(a). The average variation in frequency for 4 chips is 5.5%/V for a supply variation of 0.9 V to 1.3 V. The TC-RCO frequency can be tuned by calibrating the resistor R. Fig. 18-(b) shows the variation in frequency as R is tuned. With 3-bit calibration, the oscillator can be tuned from 18.7 kHz to 21.7 kHz.

Fig. 19-(a) shows chip-to-chip variation in frequency, at one process corner, with R = 12.1MΩ. It has an average frequency of oscillation of approximately 20KHz which agrees with our simulation results in Fig. 13-a. The TC-RCO was calibrated to be at the lowest power setting, and the 1-σ variation was found to be 325 Hz with no further calibration for 9 different

TABLE II: Performance Summary

	JSSC'16 [9]	JSSC'18 [12]	JSSC'16 [17]	JSSC'19 [18]	LSSC'19 [19]	JSSC'20 [20]	TCSI'19 [21]	TCSI'19 [22]	TCSII'18 [23]	This work
Technology (nm)	65	180	180	65	65	65	180	350	65	**130**
Area (mm^2)	0.032	0.2	0.26	0.005	0.098	0.134	0.058	0.032	0.12	**0.13**
Transistor Type	Nominal V_{th} HVT	Nominal V_{th} DTMOS	Nominal V_{th} HVT	NR	Nominal V_{th} LVT	NR	NR	NR	NR	**Nominal V_{th}**
Frequency (kHz)	18.5	1.22	70.4	1200	1016	560	444.9	1000	1500	**20**
Power (nW)	130	1.14	110	820	45.3	10.5	21300	160×10^3	6000	**254/345***
Temp. Range (^oC)	-40/+90	-20/+70	-40/+80	-25/+125	-20/+60	0/+100	-20/+100	-40/+125	0/100	-20/+100
TC (ppm/^oC)	27 – 84	40 – 153	14.7 – 75	82 – 113	20.3	60 – 150	224	31.5	50–100	21–49##
No. of Chips	4	5	5	7	1	4	100	1	4	**4**
Energy (nW/kHz)	7	0.93	1.56	0.68	0.044	0.018	47.8	160	4	**12.8/17.4**
Voltage Acc. (%/V)	< 5	17.2	0.75	0.7	100	11.01	0.07	$\pm$0.08%	0.15	**5.5**
Allan Floor (ppm)	20	58	<7	10	300	100	1.1	15	NR	**10@**

**Low Power mode/ High Power mode, ## -20-100^oC stability in Low Power mode, @Allan floor in High Power mode*

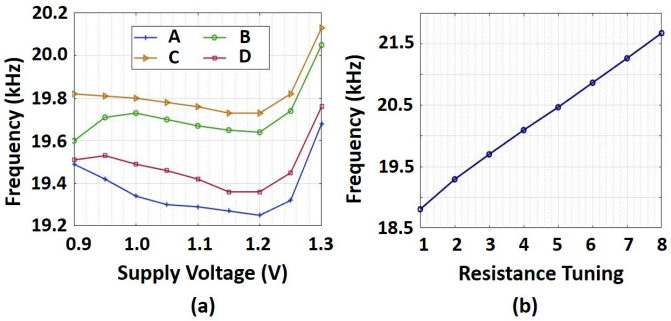


Fig. 18: (a) Supply voltage variation of oscillator frequency for 4 chips. The measurement was taken at the lowest power setting with no further calibration.(b) 3 bit calibration of the resistor R for tuning of the RC oscillator.

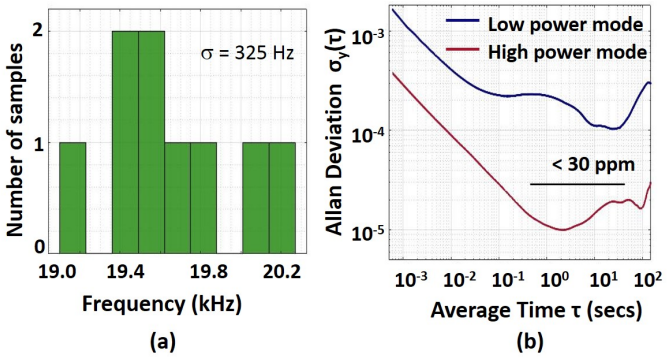


Fig. 19: (a)Measured frequency variation of the oscillator across 9 chips at room temperature, R = 12.1MΩ. The measurement was taken at nominal frequency with no further calibration. (b) Measured Allan Deviation of the TC-RCO.

chips.

Table II shows a comparison of performance metrics of the TC-RCO with previously published oscillators. It achieves a minimum temperature stability of 21 ppm/^{o}C and a maximum temperature stability of 49 ppm/^{o}C across 4-different chip for a temperature range of -20-100^{o}C. Oscillator's minimum temperature stability is one of the lowest for a large temperature range compared to other state-of-the-art oscillators. The TC-RCO also has one of the lowest supply sensitivity a 5%/V variation over a 400 mV range of supply variation. The TC-RCO achieves one of the lowest Allan deviation among oscillators with similar temperature coefficients and temperature range. In this work, we have only used nominal V_{th} transistors in the TC-RCO design. Previously published state-of-the-art oscillators have been designed with a combination of high V_{th} transistors (H_{VT}), and low V_{th} transistors (L_{VT}) to achieve high temperature stability. Overall, the TC-RCO achieves one of the best performance across design parameters. It has one of the lowest TC, supply variation, and Allan Floor with power consumption comparable to other ultra-low power oscillators.

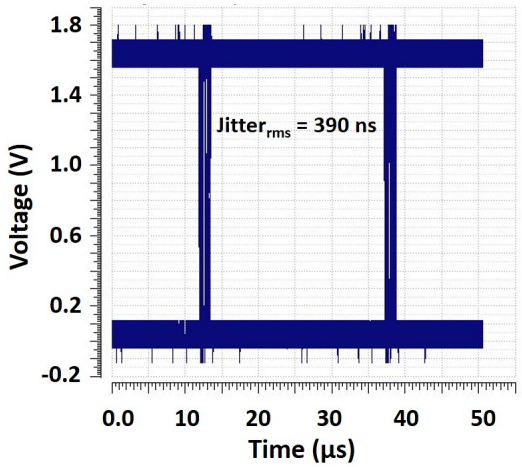


Fig. 20: Measured jitter of the TC-RCO.

The long term stability of the oscillator is measured and shown in Fig. 19-(b). The Allan Deviation is measured at nominal frequency and lowest power settings, and is found to be $<$ 300 ppm after averaging time of 1 s. With increased power from 254 nW to 345 nW, the Allan Deviation floor improves to 10 ppm, showing 30$\times$ improvement. The eye diagram of the TC-RCO output is shown in Fig. 20 which

shows measured RMS jitter of 390ns which approximately 0.8% of the period. The oscillator output is brought out using 1.6V I/O buffers to protect against electrostatic discharge (ESD) related issues.

V. Conclusion

An ultra low power RC oscillator is presented in this work. The TC-RCO achieves high frequency stability by utilizing offset compensation and second order delay compensation in the comparators. The second order compensation is by loading the comparator with an n-MOS capacitor. It achieves a minimum temperature stability of 21 ppm/°C for a temperature range of -20 - 100°C. Additionally, the long term stability of the oscillator is improved with a trade off in power consumption without affecting the oscillator frequency. Long term stability of 10 ppm is achieved after an integration time of 1 sec. The oscillator also achieves low variability with supply voltage, with a voltage accuracy of 5.5%/V. The design is carried out using nominal-V_{TH} transistors and uses a negative supply to control the leakage. It achieves one of the best performance across design parameters for ultra-low power precision clocks.

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