33.9 A Miniature Neural Interface Implant with a 95% Charging Efficiency Optical Stimulator and an 81.9dB SNDR ΔΣM-Based Recording Frontend

Linran Zhao[1], Wei Shi[2], Yan Gong[3], Xiang Liu[3], Wen Li[3], Yaoyao Jia[1]

[1]University of Texas, Austin, TX
[2]Meta, Santa Clara, CA
[3]Michigan State University, East Lansing, MI

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Neural interface implants are revolutionizing neuroscience research, especially in brain-machine interfaces and neuromodulation therapies. Miniaturizing implants can significantly reduce their invasiveness and prevent them from impeding natural behaviors due to size or tethering. However, device miniaturization brings new challenges when the implant needs to support power-intensive applications like optical stimulation. These challenges arise from the power Rx (e.g., a coil) receiving a limited amount of power due to its small size. Hence, the recently demonstrated miniature implants can only support a single neural interface modality, either stimulation or neural recording [1-4]. To bridge this gap, we designed a miniature neural interface implant for simultaneous optical stimulation and neural recording. The ASIC of the implant incorporates a linear charging switched capacitor stimulation (LC-SCS) structure that can deliver peak pulses of 12mA to the LED with 95% charging efficiency while reducing the off-chip components required by the ASIC to one small capacitor. This innovation facilitates both device miniaturization and wireless power transmission. The ASIC also employs an artifact-tolerant frontend design, in which a CT-ΔΣM directly digitizes neural signals with a peak SNDR of 81.9dB and a dynamic range (DR) of 83.7dB. This innovative frontend ensures reliable neural recording, even in the presence of artifacts up to 400mV$_{PP}$.

Figure 33.9.1. shows the conceptual view of the miniature neural interface device implanted on a desired brain surface. In the miniature implant, the ASIC, one off-chip capacitor, LED, electrode, and the Rx coil (L_3) are assembled on a substrate board. A 144MHz 3-coil inductive link with its Tx coil (L_1) and resonator (L_2) placed outside the body can deliver sufficient power in the near-field to the implant at 18% power transfer efficiency (PTE) without surpassing the SAR limit. This inductive link is also used for bidirectional data transmission between the ASIC and the data Rx. In the ASIC, a rectifier converts the AC input (V_{COIL}) to a DC voltage (V_{SUP}), which is further regulated to V_{DD}. The LC-SCS drives LED with current pulses to apply optical stimulation. The pulse pattern can be adjusted based on stimulation parameters decoded from the OOK-modulated V_{COIL} through forward data telemetry. The CT-ΔΣM can simultaneously sample recorded signals in the presence of artifacts. The digitized data produced is routed to the backscatter-based data Tx, which then wirelessly transmits the data to the external data Rx for data recovery and display.

In Fig. 33.9.2, traditional stimulation architectures like constant current simulation (CCS) and switched capacitor stimulation (SCS) have low charging efficiency and require a high supply voltage (V_{SUP}) that is larger than LED's forward voltage [1]. While the voltage-boosted SCS (VB-SCS) mitigates the need for high V_{SUP}, it necessitates multiple large off-chip capacitors, challenging device miniaturization [5]. The LC-SCS incorporates a 3× charge pump (CP), elevating the LED driving voltage (V_{LED}) to 3xV_{SUP}. In the CP, the non-overlapping (NOV) clocks (Φ_1 and Φ_2) converted from CLK_{SW} drive the CP power stage, in which two identical CP cells ($Cell_{0°}$ and $Cell_{180°}$) operate in a time-interleaved manner. Each cell employs serial-parallel topology due to its high efficiency. Moreover, to efficiently drive the switches in the CP cell, a self-gate-driven mechanism is implemented, which is to use the top plate voltage of the flying capacitor (C_{U2}), V_{CU2}, in one CP cell to power the gate driver in the other CP cell. Specifically, when $Cell_{0°}$ is connected in parallel configuration, $V_{CU2,180°} = 3V_{SUP}$ powers the gate driver in $Cell_{0°}$, in contrast, when $Cell_{180°}$ is in parallel connection, $V_{CU2,0°} = 3V_{SUP}$ powers the gate driver in $Cell_{180°}$. Moreover, the LC-SCS employs a linear capacitor charger to regulate the charging current, reducing the loading on inductive link. During the charging phase (Φ_C), the CP continuously charges the off-chip storage capacitor (C_S) with a small constant current through the linear charger. During the stimulation phase (Φ_S), C_S dumps its charges to LED, generating high instantaneous LED current (I_{LED}). LC-SCS achieves high charging efficiency thanks to its current charging mechanism. In addition, since the charging current is under control, this charging mechanism prevents large V_{SUP} drops caused by the loading effect. Hence, the capacitor at the V_{SUP} node can be reduced to the order of nF, allowing for on-chip implementation.

Figure 33.9.3 shows the ΔΣM-based direct digitizing frontend. The CT-ΔΣM realizes a 2nd-order noise shaping (NS) using a linearized Gm-C filter followed by a NSSAR quantizer. To eliminate input DC offsets, the ΔΣM employs an AC-coupled input. The feedback signal, reconstructed by a CDAC, is subtracted from the input signal at the input of the Gm-C integrator. The produced residue signal with a small swing is then integrated by the Gm-C filter. Since the Gm-C serves as the primary integrator, its linearity dominates the DR of the ΔΣM. To improve the Gm-C's linearity, a high-gain folded-cascode amplifier is implemented to boost Gm, enhancing the Gm value to approach a constant value of $1/R_S$. The NSSAR quantizer samples the Gm-C output while performing the 2nd integration. Compared to the SAR quantizer [6], the NSSAR quantizer exhibits higher energy efficiency as its inherent integration function enables the NSSAR to achieve quantization noise suppression similar to that of the SAR quantizer while using smaller quantization bits. Moreover, since the NSSAR is a DT quantizer, it will not introduce extra excess loop delay (ELD), eliminating extra feedback or feedforward circuits for ELD compensation. In addition, the NSSAR features a parasitic-insensitive active integrator, ensuring superior NS performance.

In the optical stimulation measurements (Fig. 33.9.4), even with a low V_{SUP} of 1.25V, C_S can be fully charged, the voltage across C_S, V_C, reaching the CP's output voltage (V_{CHAR}) of 3.6V. When the stimulation starts, the LC-SCS discharges C_S within a short time, delivering current pulses with 2ms pulse width at 0.5Hz to the LED. The current limiter sets the peak I_{LED} to 12mA, resulting in the peak output light intensity of 10.5mW/mm^2, which is well above the optical stimulation threshold. After each stimulation, the charger in the LC-SCS continuously charges C_S with 12μA current until the onset of the next stimulation, resulting in V_C linear increasing during the charging phase. The CP together with the linear charger achieves a high measured peak charging efficiency of 90.1-95% at different charging currents. The charging efficiency is defined as the stored energy in C_S over the input energy of the CP. Smaller charging current results in higher charging efficiency but longer charging time. The peak charging efficiency is measured when charging C_S takes the maximum tolerable charging time. LC-SCS can deliver I_{LED} tunable within 1.5 to 12mA, corresponding to the measured peak light intensity of 1.625 to 10.5mW/mm^2. Figure 33.9.5 shows the measured SNDR and DR of the CT-ΔΣM. With a 400mV$_{PP}$, 2.03kHz sinewave applied to the CT-ΔΣM, the output power spectral density (PSD) indicates a peak 81.9dB SNDR within 10kHz bandwidth. The measured SNDR vs. input amplitude shows 83.7dB DR with a full scale of 1V. The power consumption of the CT-ΔΣM is 9.8μW. These measurements reveal that the CT-ΔΣM can provide 173.8 FoM$_{DR}$ and tolerate artifacts up to 400mV$_{pp}$.

To verify the functionality of the miniature neural interface implant, in vivo experiments were conducted on 2 anesthetized Sprague Dawley rats with AAV-m Cherry virus injected in their primary visual cortex (V1). After cortical neurons expressed light-sensitive channelrhodopsin-2 (ChR2), subjects received unilateral stimulation on the left V1 lobe. The prototype of the miniature implant has a size and weight of 4×4×2.5mm^3 and 18mg (Fig. 33.9.6). The ASIC and the single off-chip capacitor were mounted on the top of the substrate. The substrate also carried one blue LED and one pad for electrode assembly on its backside. L_3 was wound around the ASIC after coating the ASIC and its bonding wires. A power amplifier wirelessly delivered power to the miniature implant through the 144MHz 3-coil inductive link. The miniature implant drove the LED with a 3ms pulse train at 1Hz and 12mA I_{LED} and simultaneously recorded local field potentials (LFPs) from the left V1 lobe at 800μm depth through a penetrating tungsten electrode. Digitalized LFP data, wirelessly received by the data Rx, was recovered for data analysis. Compared to the baseline (LFPs without stimulation), the light-evoked LFPs showed higher amplitude and PSD, indicating the effectiveness of optical stimulation. In addition, the transient LFPs showed that the miniature implant successfully recorded the desired LFPs in the presence of artifacts. Figure 33.9.7 shows the ASIC micrograph in 0.18μm standard CMOS and a benchmarking table.

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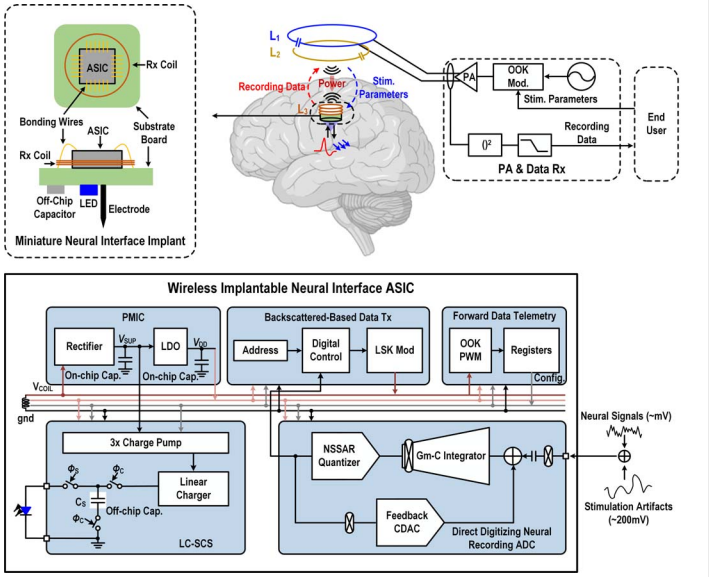


Figure 33.9.1: Conceptual view of the miniature neural interface device and ASIC block diagram.

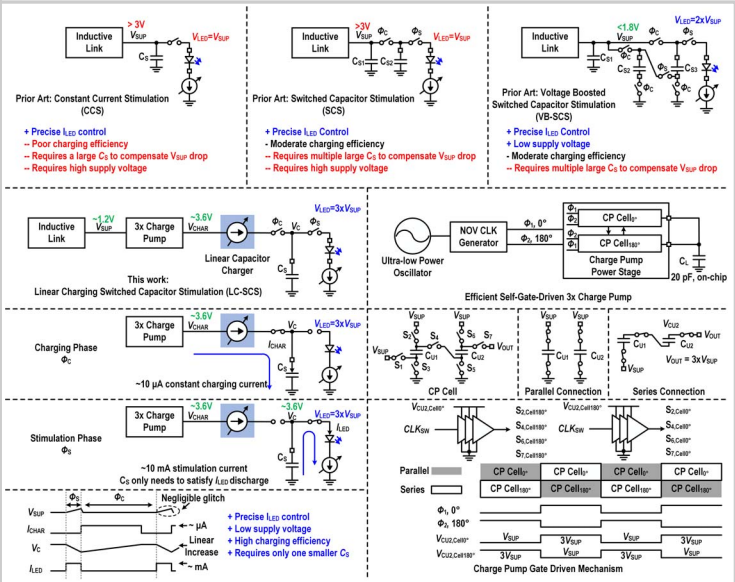


Figure 33.9.2: Comparison between the prior art, such as CCS, SCS, and VB-SCS, and the LC-SCS; schematic of the self-gate-driven charge pump.

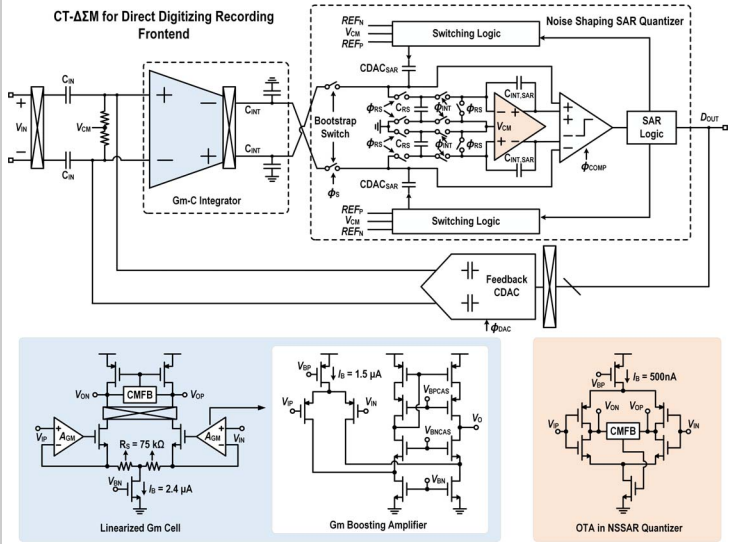


Figure 33.9.3: Schematic of the CT-ΔΣM, Gm cell, Gm-boosting amplifier, and OTA in NSSAR quantizer.

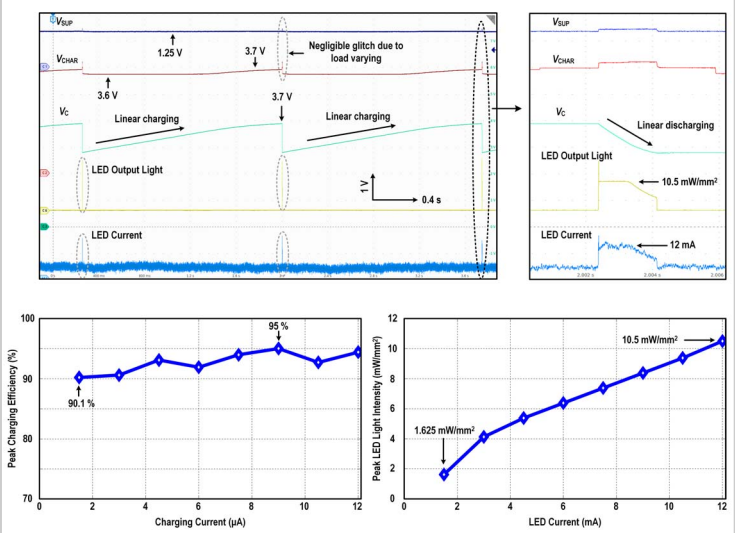


Figure 33.9.4: Measurement results of the transient LC-SCS operation, the peak charging efficiency at different charging currents, and the peak light intensity as a function of the LED current.

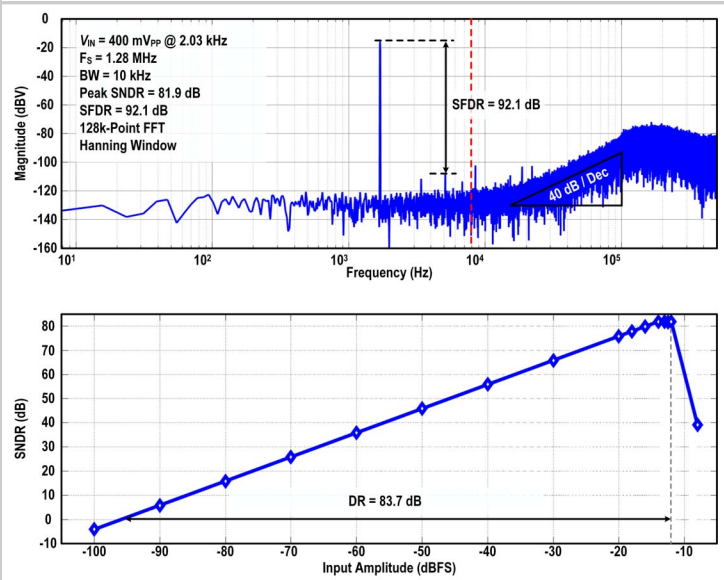


Figure 33.9.5: CT-ΔΣM measurement results: output PSD and SNDR vs. input amplitude.

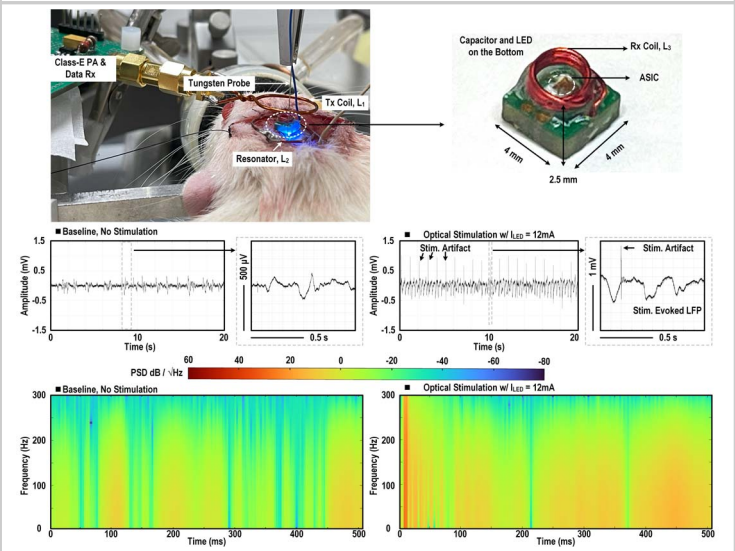
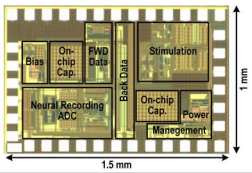


Figure 33.9.6: *In vivo* experiment results from two transfected rats, applying optical stimulation while recording LFPs from the left V1 lobe, to verify the functionality of the miniature neural interface implant prototype.



	Reference	This Work	ISSCC'18 Jia [1]	ISSCC'19 Ghanbari [2]	Nat. Electron.'20 Lee [3]	ISSCC'22 Lee [4]
System	Technology	180 nm	350 nm	65 nm	65 nm	110 nm
	Chip Area (mm²)	1.5	1	0.25	0.25	4
	Supply Voltage (V)	1 / 1.25	5	1	1	1 / 2.3
	Wireless Link	RF, 144 MHz	RF, 60 MHz	US, 1.78 MHz	RF, 915 MHz	Body Link, 32MHz
	Total Power (mW)	0.27[b]	1[b]	0.028[c]	0.030[b]	0.644[c]
	Implants Size & Weight	4 x 4 x 2.5 mm³, 18 mg	2.5 x 2.5 x 1.5 mm³, 15 mg	3.8 x 0.84 x 0.75 mm³, -	0.65 x 0.65 x 0.25 mm³, -	4 x 8 x 1 mm³, -
	Required Off-Chip Components / Channel[a]	1 Coil, 1 Capacitor	1 Coil, 3 Capacitors	1 US Transducer	None	2 Electrodes for Power & Data
	System Modality	Opt. Stim. + Rec.	Opt. Stim.	Rec.	Elec. Sti. / Rec.	Rec.
Stimulation	Stim. Topology	LC-SCS	SCS	-	CCS	-
	Stim. Supply (V) / LED Drive Volt. (V)	1.2 V / 3.6V	5 V / 5 V	-	1 V / -	-
	Max Stim. Current (mA)	12	10	-	0.025	-
	Max η_{CHAR} (%)	95	37	-	-	-
Recording	Topology	CT-ΔΣM	-	LNA	CT-ΔΣM	CT-ΔΣM
	Power (μW) / Channel	9.8	-	4	3.2	8.6
	Area (mm²) / Channel	0.15	-	-	0.01	0.04
	Supply (V)	1	-	1	1	1
	IRN (μV_{RMS})	7	-	5.3	2.2	6.6
	Signal BW (kHz)	10	-	5	0.5	10
	SNDR/DR (dB)	81.9 / 83.7	-	- / -	51 / -	82.3 / 83.3
	Peak Input (mV_{PP})	400	-	20	2	300
	FoM_{SNDR} / FoM_{DR}	172.2 / 173.8	-	- / -	133 / -	173 / 174

[a]Exclude the commonly required off-chip components for neural recording and stimulation. (e.g. electrodes, LEDs) [b]Measured at maximum stimulation current.
[c]No stimulation function

Figure 33.9.7: Neural interface ASIC micrograph, along with a benchmarking table.

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