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A 12-162 GHz Distributed Amplifier in a 45-nm BiCMOS SOI Process Achieving 2.67 THz Gain-Bandwidth Using an Active Bias Termination

Justin J. Kim[1], Wonho Lee[2], James F. Buckwalter[1]
[1] *University of California Santa Barbara, Santa Barbara, CA*
[2] *PRL PCR, Intel Labs, Hillsboro, OR*

***Abstract*—A low power 12-162 GHz distributed amplifier (DA) is demonstrated with an average gain of 25 dB. This circuit is realized with a NMOS/HBT cascode cell using a 45-nm BiCMOS Silicon-on-Insulator (SOI) process. The DA utilizes the high f_{max} CMOS to provide an active bias termination on the input in order to add tunability in the circuit to mitigate the unknowns of a new process. The total power consumption of the DA is 215 mW with a core area of 0.45 mm^2.**

***Index Terms*—SiGe BiCMOS, silicon-on-insulator (SOI), distributed amplifier (DA), millimeter-wave integrated circuit.**

I. Introduction

The distributed amplifier (DA) is a useful circuit technique for broadband applications such as optical and wireless communication, which might use RF, microwave, and millimeter-wave frequency bands. With silicon-based process technologies continuing to improve, state-of-the-art DAs have demonstrated 100 GHz of bandwidth (BW) as designers are now nearing and exceeding 200 GHz of BW [1]-[12]. These ultra-broadband amplifiers have leveraged Silicon Germanium (SiGe) process technologies to improve the gain and BW of the amplifiers as well as take advantage of the NMOS and HBT devices [12]. The NMOS is useful in the distributed amplifier as it presents a largely capacitive load through the gate-source capacitor (C_{gs}) but typically has lower transconductance than the HBT. Oftentimes, to reduce power consumption of the DA, strategies are applied to prevent lost power in gate and drain terminations. These might include blocking the DC current through a 50 Ohm termination or supply scaling [2].

An average gain of 25 dB across 150 GHz of BW is demonstrated by using a NMOS/HBT cascode shown in Fig. 1. This cascode topology has been demonstrated in a DA [12] but is improved upon through the scaled 45-nm NMOS device. We demonstrate four different versions of the DA based on a traditional resistive termination and an active load termination enabled by the highly-scaled CMOS available in this 45-nm BiCMOS SOI process. A 1-stage resistor-terminated (RT) and active-bias-terminated (ABT) DA design is investigated to compare the effectiveness of the topology and performance limits of the new technology. A 3-stage RT and ABT design is then pursued to increase the gain and benchmark this new technology against recent work. Section II describes the technology used in this work. Section III describes the design of the proposed DA. Finally, Section IV introduces the measurements of both the 1-stage and 3-stage RT and ABT DAs.

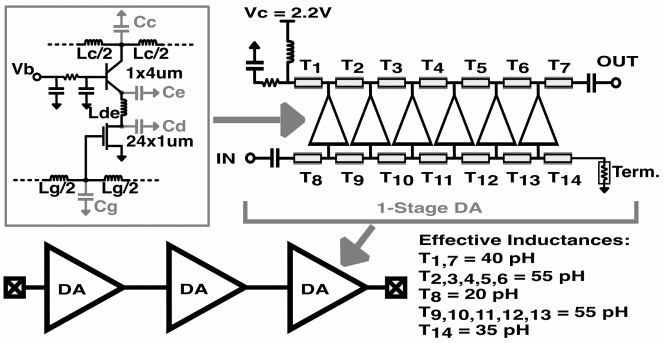

Fig. 1: Schematic of 3-stage cascode distributed amplifier illustrating the NMOS/HBT cascode cell with the effective inductance of each transmission line.

II. Technology

All four DA designs are implemented in Global Foundries 45-nm BiCMOS SOI (45SG01). The process is built upon a high resistivity SOI substrate and offers high-Q passives. The HBTs offer 400 GHz f_T and 600 GHz f_{max}, while the NMOS devices have 350 GHz f_T and 400 GHz f_{max}. The back-end-of-the-line (BEOL) consists of nine copper metal layers and a top aluminum metal layer. All transmission lines are employed as micro-strips on the top copper layer (OB) with the ground plane on the fifth copper layer (BA).

The maximum available gain (MAG) of the NMOS/HBT cascode are plotted for f_{max} in Fig. 2. A (1um x 24) / 40nm NMOS and 1x4um HBT are used with a current density of 0.23 mA/um and 1.38 mA/um, respectively. The PDK NMOS and HBT curves reflect the current used in the cascode and not the optimum bias point for peak f_{max}. While both the NMOS and the HBT have excellent RF performance, the cascode of a common-source NMOS with common-base HBT offers significantly higher gain up to around 200 GHz as plotted in Fig. 2. The MAG curve for the NMOS/HBT cascode includes electromagnetic simulations of the parasitic resistance and capacitance up to the OB layer and can be seen in Fig. 2. The MAG remains above 15 dB to 200 GHz.

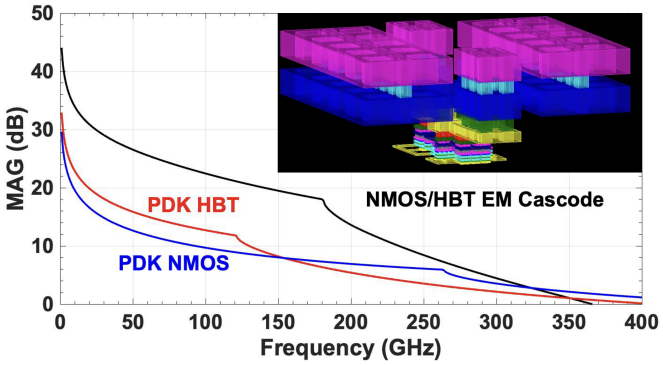

Fig. 2: Simulated MAG for NMOS/HBT cascode including EM simulation of BEOL interconnects compared to foundry model of NMOS and HBT. The NMOS/HBT cascode offers significant gain to 180 GHz. The BEOL interconnects are simulated to the top copper metal as indicated by the inset image.

III. Distributed Amplifier Design

Fig. 1 shows the schematic of a 3-stage cascode DA. Each stage is identical and consists of 6 sections of the NMOS/HBT cascode. This topology was chosen due to the reduced junction capacitance SOI technologies offer at 45-nm when compared to traditional bulk CMOS. A high performance DA was previously demonstrated using a purely CMOS SOI approach [11]. The common-base HBT allows for improved voltage swing and improved output resistance from the active device.

Micro-strip transmission lines are implemented between each section to emulate a series inductance that absorbs the parasitic NMOS and HBT capacitance to create an artificial transmission line with characteristic impedance close to 50 Ω. The characteristic impedance is approximated by the equation $Z_0 = \sqrt{L_g/C_g} = \sqrt{L_c/C_c}$. The effective values of the interstage inductances are included in Fig. 1. The gate capacitance per segment is ∼22fF while the collector capacitance per segment is ∼25fF.

Two different input terminations are explored in this work for the gate transmission line; the schematic for both can be seen in Fig. 3. The transmission line (T_{14}) in Fig. 3 illustrated in the figure refers to the gate transmission line section in Fig. 1. The RT DA follows the traditional approach of terminating the 50-Ω line to an approximately similar resistance, shown as 40-Ω, while providing DC bias through the choke inductor. The disadvantage of this approach is that the low-impedance to ground shifts between the inductor to the voltage supply to the bypass capacitor (1 pF), which must be designed to have a higher self-resonant frequency.

An active termination is created using the high f_T CMOS devices in a shunt-feedback transimpedance stage. The input impedance to M1/M2 is determined by the channel resistance of M3, e.g. $Z_{IN} = \frac{r_{ds3}}{1+(g_{m1}+g_{m2})(r_{ds1}||r_{ds2})}$. To mitigate the matching of this relatively new process, the r_{ds3} can be tuned through a 1.1kΩ resistor.

To match to the nominally 50Ω transmission line, the magnitude of the input impedance is plotted between DC and 200 GHz for the RT and ABT terminations in Fig. 4. The simulated S_{11} is indicated at the input to the single stage DA. The RT indicates degraded matching near 10 GHz as well as worse return loss at 100 GHz and higher frequencies. On the other hand, the ABT approach is plotted for two sample tuning voltages. The V_{tune} of 0.5V indicates a high termination impedance, e.g. large r_{ds3}, and shows poor matching below 100 GHz. For V_{tune} of 2.0V, the input reflection is similar to the RT solution with the advantage that the matching ripple is significantly lower.

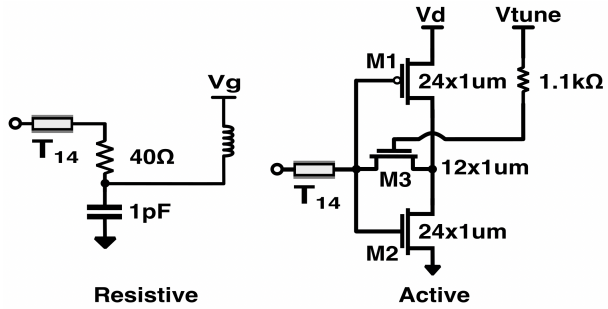

Fig. 3: Schematic of resistive and active-bias terminations.

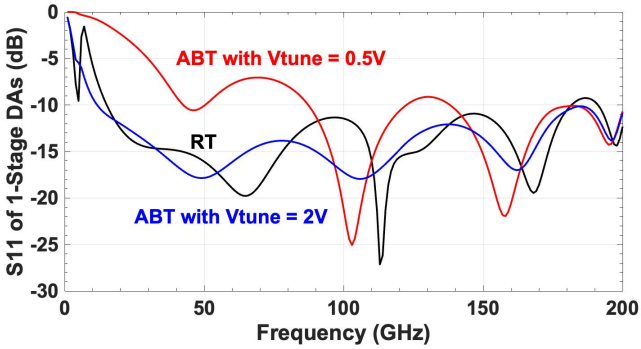

Fig. 4: Simulated S_{11} from DC - 200 GHz for the RT and ABT single stage DA. The higher tuning voltage on the ABT DA offers similar input reflection as the RT DA with the benefit of lower matching ripple.

IV. Measurements

The die photographs for the 1-stage RT DA and the 3-stage ABT DA are shown in Fig. 5. The total area for both the 1-stage ABT (not shown) and the 1-stage RT DA is 0.85 x 0.45 mm^2, with a core area of 0.58 x 0.25 mm^2. The total area for both the 3-stage ABT and the 3-stage RT (not shown) DA is 2.08 x 0.45 mm^2, with a core area of 1.81 x 0.25 mm^2.

S-parameters measurements between 10 MHz and 200 GHz are performed using three different test benches including coaxial measurement up to 67 GHz and waveguide band measurements. All setups use a Keysight PNA-X with Keithley DC power supplies. From 10 MHz - 67 GHz, 1.85 mm connectors are used with the network analyzer and calibrated with a CS-2-100 calibration substrate. At D-Band (110-170 GHz), Virginia Diodes (VDI) WR6 waveguide extenders are used

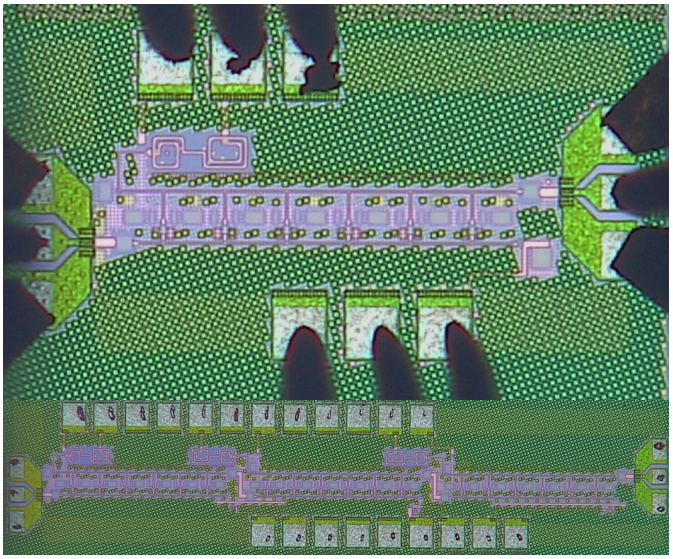

Fig. 5: Chip micrograph of the 1-stage resistive terminated DA (top) and the 3-stage active bias terminated DA (bottom).

and calibrated with on-chip TRL structures. At G-Band (140-220 GHz), OMN V05VNA-T/R WR5 waveguide extenders are used and calibrated with on-chip TRL structures. Due to higher uncertainty in calibration at the end of the frequency extenders, the measurement data for the 1-stage DAs at D-Band are shown from 113-160 GHz and 113-167 GHz for the 3-stage DAs. For the 1-stage DAs, measurement data from 160-200 GHz are taken from the G-Band setup. Measurements were not taken from 67 - 110 GHz due to lack of equipment; however, measurement data below 67 GHz and above 110 GHz show a relatively flat gain response with low return loss on both the input and output and suggests uniform gain within the unmeasured frequency range. Measured S-Parameters for the 1-stage and 3-stage designs are plotted in Figs. 6 and 7, respectively.

The measured S_{21} of the 1-stage ABT DA is 8.8-10.8 dB at 12-67 GHz, 7.1-8.4 dB at 113-160 GHz, and 5.3-7.5dB at 160-180 GHz for an average piecewise linear gain of ∼8.3 dB between 12-180 GHz. The measured S_{21} of the 1-stage RT DA is 8.4-11.0 dB at 12-67 GHz, 6.8-8.5 dB at 113-160 GHz, and 5.3-8.1 dB at 160-180 GHz for an average piece-wise linear gain of ∼8.3 dB between 12-180 GHz. Using the average gain, both versions of the 1-stage DA exhibit a gain-bandwidth product (GBW) of 437 GHz. The reverse isolation is greater than 25dB from DC-200 GHz for both versions of the 1-stage DA.

The measured S_{21} of the 3-stage ABT DA is 25.1-32.5 dB at 12-67 GHz and 21.0-24.3 dB at 113-162 GHz for an average piece-wise linear gain of ∼25 dB between 12-162 GHz. The measured S_{21} of the 3-stage RT DA is 26.0-31.6 dB at 12-67 GHz and 19.0-24.3 dB at 113-162 GHz for an average piece-wise linear gain of ∼25 dB between 12-162 GHz. Using the average gain, both versions of the 3-stage DA exhibit a GBW of 2667 GHz, which is very competitive among other state-of-the-art SiGe DAs. The reverse isolation is greater than 33 dB from DC-200 GHz for both versions of the 3-stage DA.

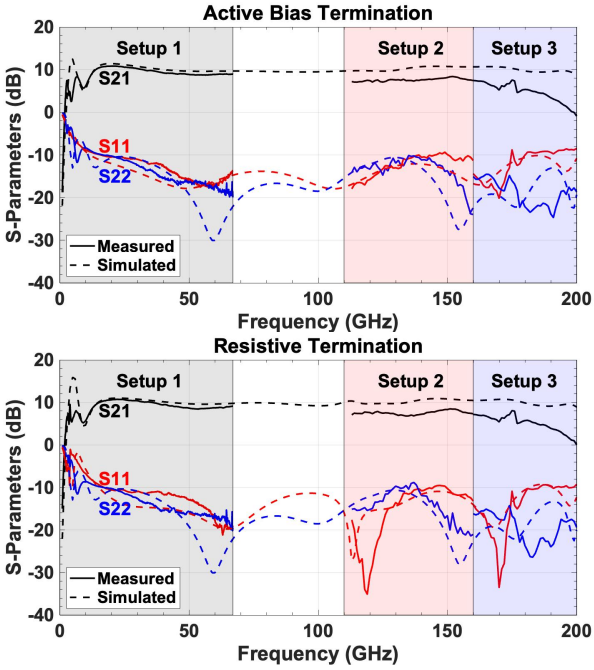

Fig. 6: Simulated and measured S-parameters of the 1-stage resistor- and active-biased- terminated DA.

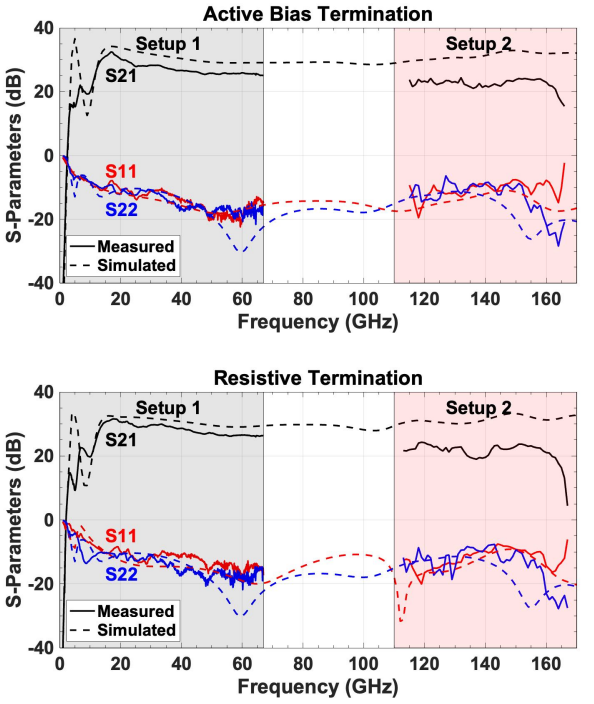

Fig. 7: Simulated and measured S-parameters of the 3-stage resistor- and active-biased- terminated DA.

Despite creating the ABT version of the 1-stage and 3-stage DA to mitigate process unknowns of a new technology and provide tunability to the input, the RT versions performed equally well. The most noticeable measurement result of the ABT was a lower variation in gain at D-Band in the 3-stage design when compared to the RT. This can be seen by comparing the slight drop in gain around 135 GHz in Fig. 7.

The measured data from 10 MHz - 67 GHz shows good agreement with simulation for both 1-stage designs; however, gain is 1-2 dB lower at 110+ GHz for the 1-stage DAs and 7-9 dB lower for the 3-stage DAs. The discrepancy at higher frequencies can be attributed to the poor modeling of the T-junction on the input and output of each transistor cell and the addition of higher metal fill in the middle of the design to meet the aggressive density requirements of the process.

All S-parameter measurements are performed with a collector bias of 2.2 V and a base bias of 1.85 V which generated a current of 31.3 mA per stage. For the RT designs, a gate bias of 0.57 V was applied while the ABT designs had a 1.2 V bias on the source of the PMOS and a tuning voltage set to 2 V which generated a current of 2.3 mA per stage.

Both the 1-stage and 3-stage DA are compared to other state-of-the-art SiGe DAs in Table 1. The 3-stage DA is very competitive in terms of GBW while also providing a low power and small area design.

TABLE I: Comparison to SiGe Distributed Amplifiers with BW near and above 100 GHz.

Ref.	Process	Gain (dB)	BW (GHz)	GBW (GHz)	Power (mW)	Area (mm^2)
This Work 1-Stage	90-nm SiGe$^+$	8.3	168	437	72	0.15
This Work 3-Stage	90-nm SiGe$^+$	25	150	2667	215	0.45
[1]	90-nm SiGe	27	120	2577	-	1.25
[2]	90-nm SiGe	12	91	362	297	1.51*
[3]	130-nm SiGe	10	110	348	357	2.18*
[4]	130-nm SiGe	24	95	1500	247.5	0.41
[5]	130-nm SiGe	10	170	537	108	0.38*
[6]	130-nm SiGe	13	170	759	74	0.23*
[7]	130-nm SiGe	18.7	180	1550	86	0.61*
[8]	130-nm SiGe	19	160	1426	560	0.91*
[9]	130-nm SiGe	19	170**	1515**	350	0.14
[10]	130-nm SiGe	23 25.5	167 248	2359 4671	465 644	0.13 0.091
[12]	90-nm SiGe	15.5	80	477	870	1.05*

*Total Area. **Measurement Limited. $^+$ 90-nm SiGe on 45-nm SOI

V. Conclusions

A low power, compact, 12-162 GHz DA is demonstrated in the new 45SG01 Global Foundries process with an active bias termination. This work utilizes a NMOS/HBT cascode that leverages the scaled 45-nm NMOS. The three-stage DA achieves an average gain of 25 dB with a very competitive gain-bandwidth product of 2667 GHz.

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