

2.4 GHz Ultra-Low Power Direct Digital-to-RF CMOS Transmitter for Biosensing Applications

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Abstract—This paper presents a low-power and low-complexity direct digital-to-RF transmitter architecture, suitable for biosensing applications. The RF front end of the transmitter is based on a ring oscillator, whose output phase is modulated through the charge-to-phase mechanism using a charge injection block. Hence, the phase shift keying (PSK) modulation can be performed directly in the RF domain. Post-layout simulation results show that the transmitter is able to collect, process, and transmit sensed data with the maximum data rate of 20 Mbps and an error vector magnitude (EVM) of smaller than 3.5%, while dissipating the DC power smaller than 0.5 mW. The results demonstrate that the proposed transmitter architecture is effective for wireless biosensing applications.

Index Terms—Biosensing, low-power RF front end, phase shift keying, ring oscillator, direct digital-to-RF transmitter.

I. INTRODUCTION

Biosensors play an important role in various fields, from healthcare to environmental monitoring and food safety [1]–[5]. These innovative devices combine the power of biology with the sensitivity of modern technology to detect and measure vital and biological responses and convert them into quantifiable signals [6]–[13]. This ability to rapidly and accurately detect and analyze these signals has revolutionized the process of early treatment of serious life-endangering conditions by offering real-time monitoring, early disease diagnosis, and enhanced safety measures [14], [15]. The growth of biosensors has been remarkable in recent years, driven by advancements in technology, increasing demand for point-of-care diagnostics, and the need for rapid and accurate detection methods. The global biosensor market has witnessed significant expansion, with projections indicating continued growth in coming years. There are several challenges to grow the projected market size of biosensors [16]. Manufacturing and maintenance costs, sustainability and reliability, and power consumption are a few important factors that could be addressed partially or completely through hardware design.

Although wired sensors offer superior accuracy and resolution in data collection and transmission, they have limited mobility and wearability compared to wireless ones [17]. Typical wireless biosensors are powered by batteries, and replacement or recharging batteries interrupts the sensing operation and is cumbersome. Self-powered biosensors fit better for typical biosensing applications [18]. However, the limited harvested

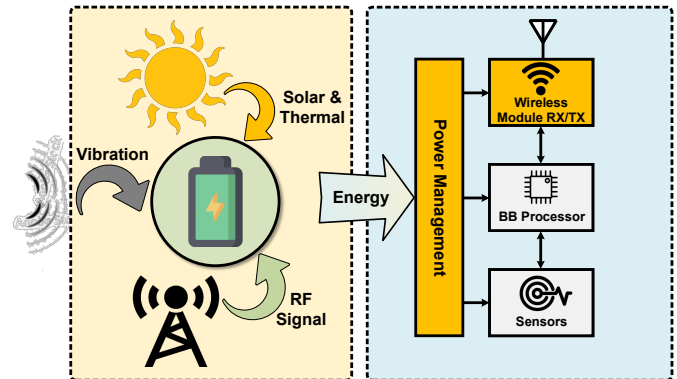


Fig. 1: Block diagram of a typical self-powered sensor.

power can cause an interruption in the sensing process or failure in the data transmission. Low power design of self-powered wireless biosensors is a major design challenge. Fig. 1 shows the block diagram of a typical self-powered wireless sensor equipped with a versatile energy harvester to power the sensor. The RF front end for a typical wireless transmitter dissipates most power [19], and reduction of the power dissipation for the RF front end is of paramount importance.

This paper presents a direct digital to RF transmitter architecture featuring low-power dissipation, compact size, and low complexity, which enables the transmitter to be powered by a simple energy harvester.

This paper is organized as follows. Section II presents design of major building blocks including the charge control block for a ring oscillator. Section III discusses the post-layout simulation results. Finally, Section IV concludes the paper.

II. DESIGN OF A DIRECT RF TRANSMITTER

A. Phase Modulated Oscillator

Oscillators in typical circuits provide clock signals with a fixed phase and are distributed among the building blocks. The phase of an oscillator waveform can be controlled by controlling the charge to the phase translation mechanism [20], [21], and such an oscillator is presented in our earlier paper [22]. Fig. 2 shows a conceptual block diagram of a variable phase oscillator adopted in [22]. The amount of charge drawn from the oscillator output can be controlled by connecting/disconnecting the capacitor C_T with the switch S_1 .

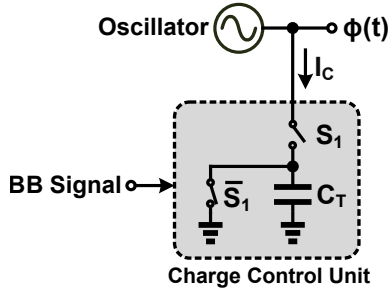


Fig. 2: Conceptual representation of the charge injection mechanism. "BB Signal" is the baseband control signal.

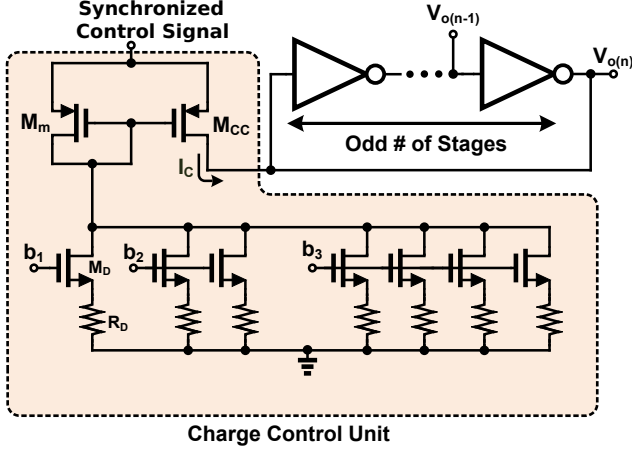


Fig. 3: Schematic of the charge control block with a 3-bit DAC.

When S_1 turns on, it temporarily disturbs the equilibrium state of the oscillator loop, resulting in disruption of the oscillation frequency. When the oscillation settles back to its steady state, the phase of the oscillator waveform is changed. The impact on the phase $\Phi(t)$ can be expressed as follows [21].

$$\Phi(t) = \int_{-\infty}^t h(\tau) i(\tau) d\tau \quad (1)$$

where $h(t)$ is the impulse response of the oscillator to the external injected/extracted charge. The current $i(t)$ is the current flowing into the capacitor C_T . Expression (1) shows that a larger impulse response $h(t)$ increases the phase shift. Therefore, it is desirable to apply the charge current $i(t)$ when $h(t)$ is large, i.e. around the rising/falling edge of the waveform. For details, refer to [21].

The variable phase oscillator in [22] is based on the conceptual circuit in Fig. 2. It has a few drawbacks. First, it requires a large capacitor array to achieve high accuracy and small phase resolution, leading to a large die area. Second, the charge sharing between the parasitic capacitors at the output node of the oscillator and C_T could degrade the accuracy of the phase shifting. Third, a mismatch between the two complementary switching signals, S_1 and $\bar{S}_1$, results in an inaccurate phase shift in the output waveform of the oscillator.

To address the drawbacks, we propose a charge control unit incorporating a digital-to-analog converter (DAC). Fig. 3 shows an example charge control unit along with 3-bit DAC

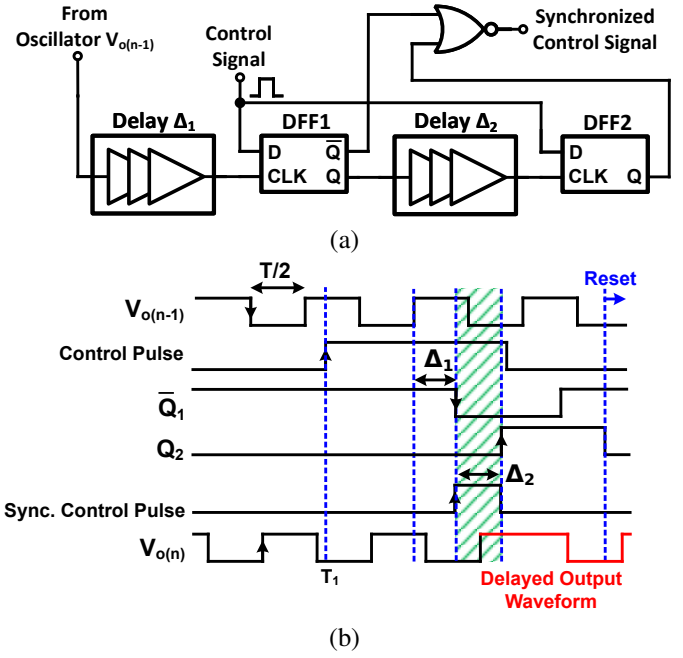


Fig. 4: (a) Block diagram of the synchronization block and, (b) the waveforms.

Clock Rate	1 MHz	5 MHz
Constellation		
Data Rate	4 Mbps	20 Mbps
EVM	3.44 %	3.4 %

Fig. 5: Simulated 16-PSK constellation diagram and its corresponding EVM for different clock frequencies.

and the ring oscillator. The binary-weighted switches b_1 to b_n , where $n=3$ for the example circuit, control the current of M_m , and the current is copied to I_C through the current mirror formed by M_m and M_{cc} . When "Synchronized Control Signal" is active (=high), the current I_C flows into the oscillator to increase the output voltage $V_{o(n)}$, resulting in the delay of the phase. The proposed charge control unit does not require a capacitor to reduce the die area. Also, the adoption of a DAC enables the circuit to control a wide range of current and hence phase shift.

The amount of phase shift of the oscillator depends on the instance of the current I_C applied to the oscillator as well as the magnitude and duration of the current. Therefore, the control pulses must be applied at the same instant of an oscillation cycle [22]. The circuit for the "synchronized control signal" and its waveform are shown in Fig. 4. When the control signal becomes activated or high, the Q_1 output of DFF1 becomes high with the delay Δ_1 after the rising edge of $V_{o(n-1)}$. The Q_2 output of DFF2 becomes high with the delay Δ_2 after the rising edge of the Q_1 output.

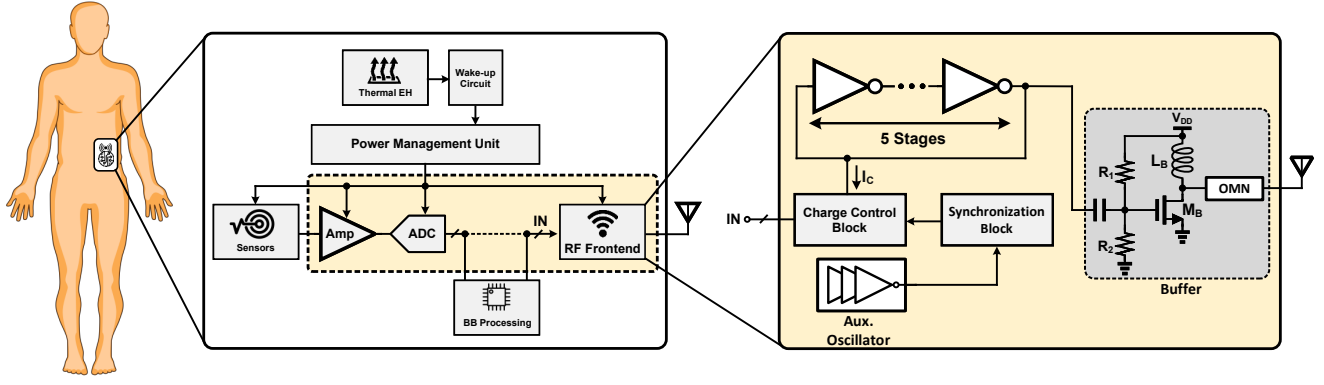


Fig. 6: Block diagrams of the self-powered wireless sensor and the RF front end.

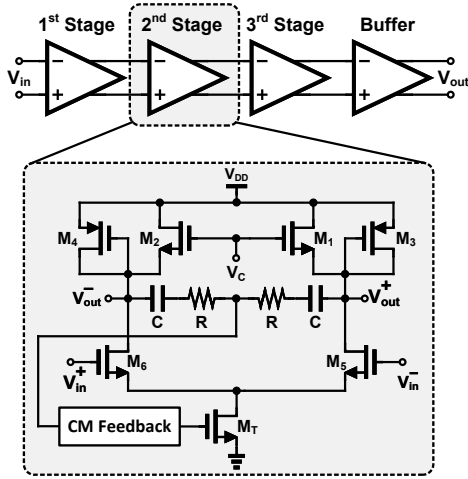


Fig. 7: Schematic of the VGA block.

The delay Δ_1 is set accordingly, so that the center point of the activation period of the "synchronized control signal" is ideally the rising edge of $V_{o(n)}$. The delay Δ_2 decides the activation period of the "synchronized control signal". When the "synchronized control signal" is activated, the DAC and the associated transistors are settled for the proposed design owing to the sufficiently large delay Δ_1 .

The proposed charge control adopts a 4-bit DAC and a 5-stage ring oscillator operating at 2.4 GHz. The simulated error vector magnitude (EVM) of the 16-PSK modulated signals at the output of the proposed transmitter is shown in Fig. 5. The EVMs for two different data rates, 4 Mbps and 20 Mbps, remain virtually the same. This is mainly due to the fact that the amount of phase shift and the application time of the "synchronized control signal" is not affected by disturbances of the application time of the control signal, which is a major advantage of the proposed design. The settling time and frequency drift of the oscillator limits the maximum attainable PSK modulation order. It is noted that the proposed modulation approach can be applied to other oscillator architectures such as negative transconductance (g_m) and Colpitts oscillators.

B. Transmitter

The block diagram of a self-powered wireless sensor is shown in Fig. 6. A thermoelectric energy harvester integrated with a power management unit powers the wireless sensor. The variable gain amplifier (VGA) amplifies the sensed signal, and the analog-to-digital converter (ADC) converts the signal to digital. The converted data, possibly after being processed by a baseband (BB) processor, is applied to the RF front end, which modulates and transmits the data. In this work, we focus on design of the highlighted part of the transmitter including the VGA, the ADC, and the RF front end.

Fig. 7 shows the schematic diagram of the VGA [23]. It is composed of three stages of unit cells followed by a buffer stage. The individual VGA stages can exhibit the exponential-like characteristic using a pair of complementary transistors as the load i.e. $M_{1,3}$ and $M_{2,4}$. Simulation results show that the VGA achieves a voltage gain of 41 dB and approximately 60 MHz of the operation bandwidth while dissipating average power of 44 μ W.

A 6-bit fully differential level-crossing ADC, proposed in [24], is developed for the proposed transmitter. The ADC utilizes a charge redistribution block instead of the conventional n-bit DAC, resulting in a significant reduction of the switching energy and hence power dissipation. The input bandwidth of the ADC is tuned to be greater than 5 kHz with DC power dissipation of 3 μ W under a 0.85 V supply. For details, refer to the original work in [24].

C. RF front end

The phase-modulated oscillator in Fig. 3, along with the charge control unit, is the foundation of the RF front end shown in Fig. 6. An auxiliary ring oscillator is also implemented to provide the clock signal for the synchronization block, in which its oscillation frequency is equal to the sampling rate for the modulated signals. A buffer is also added at the final stage of the transmitter to isolate the main oscillator from the antenna, resulting in prevention of the loading effect on the oscillator. The buffer could be removed if the harvested energy is insufficient.

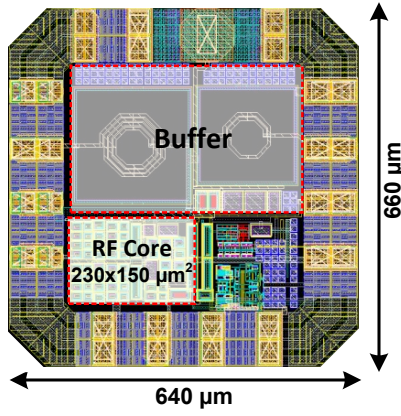


Fig. 8: Complete layout of the transmitter.

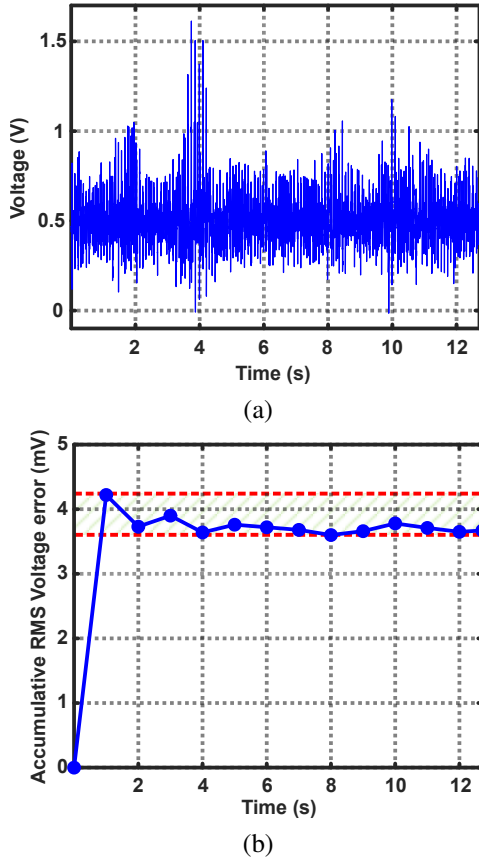


Fig. 9: (a) The sample EMG signal [25], and (b) the corresponding RMS amplitude error at the output.

III. POST-LAYOUT SIMULATION RESULTS

We laid out the transmitter in 180-nm TSMC CMOS process technology, and the layout is shown in Fig. 8. The entire circuit occupies $660 \times 640 \mu\text{m}^2$ of the silicon area, while the RF front end, excluding the output buffer, has a compact size of $150 \times 230 \mu\text{m}^2$. The RF front end, excluding the output buffer, has a DC power consumption of $492 \mu\text{W}$ under supply voltage of 0.85 V.

Fig. 9 (a) shows an analog electromyogram (EMG) signal sampled from a 44-year-old man without a history of neu-

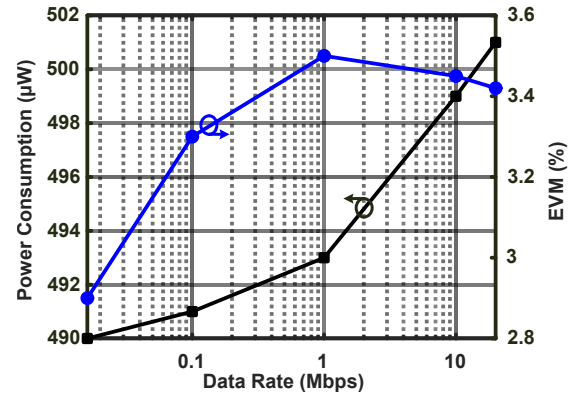


Fig. 10: Average power consumption of the RF front end and EVM of the transmitted signals versus data rate.

romuscular disease [25]. The signal is used to measure the performance of the proposed transmitter. The clock frequency of the RF front end (i.e., the frequency of the auxiliary oscillator) is set to 10 kHz, and the sampling rate of the ADC 5 kHz. The EMG signal is applied to the transmitter, and compared with at the output of the transmitter. Fig. 9 (b) shows the simulation results for the root mean square (RMS) error of the amplitude of the recovered signal. The RMS voltage error of the recovered signal remains in a narrow boundary of around 4 mV.

To further investigate the capabilities of the transmitter, we increased the number of sensors (i.e., EMG signals) and adjusted the oscillation frequency of the auxiliary oscillator accordingly. Fig. 10 shows the simulation results for the data rate ranging from 16 kbps to 20 Mbps. The power dissipation of the RF front end, excluding the output buffer, increases from $490 \mu\text{W}$ to $501 \mu\text{W}$ mainly due to the increased power dissipation of the auxiliary oscillator and dynamic power consumption of the charge control unit. The EVM of the signals at the output of the transmitter initially increases from 2.9% to 3.5% and then decreases to 3.4%. The performance is satisfactory for typical biosensing applications.

IV. CONCLUSION

This paper presents a low-power and compact transmitter architecture suitable for biosensing applications. The transmitter is designed and laid out in 180-nm CMOS process technology. The RF front end has a die size of $150 \times 230 \mu\text{m}^2$. The proposed RF front end reduces power dissipation substantially and hence is suitable for self-powered wireless sensors with limited energy harvesting capability. The number of sensors or the data rate of the transmitter can be increased significantly at the cost of slightly higher DC power dissipation. In conclusion, the simulation results demonstrate that the proposed transmitter architecture is effective for wireless biosensing applications.

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