A Single-Switch 3.1-4.7 GHz 194.52-dB FoM Class-D VCO with 495μW Power Consumption

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***Abstract*—This brief presents an ultra-low-power class-D voltage-controlled oscillator (VCO) designed for GHz applications that mandate decent phase noise performance. A waveform-centric approach of phase noise reduction by controlling the ratio between the floating and single-ended (SE) capacitors in an oscillator tank is proposed. By co-designing an RF choke with the tank inductor to introduce high impedance for the floating capacitors, the optimum capacitance ratio is maintained across the tuning range. The VCO is fabricated in 65nm Bulk CMOS technology and achieves a measured phase noise of -118.36 dBc/Hz and -138.64 dBc/Hz, and figure-of-merit of 192.89 dBc/Hz and 194.52 dBc/Hz at 1 MHz and 10 MHz offset frequencies, respectively. The VCO's lowest measured $1/f^3$ corner is approximately 50kHz, which enables a decent figure-of-merit (FoM) down to a frequency offset of 10 kHz. The VCO features a tuning range of 40% (3.1 GHz - 4.66 GHz) using a one-bit switch to realize two-point modulation in phase-locked loops (PLLs) with milliwatt-level power consumption.**

***Index Terms*—Class-D VCO, GHz, RF choke, one-bit switch, phase noise, ultra-low-power, wide tuning range.**

I. Introduction

With the widespread adoption of CMOS integrated circuits (ICs) for the development of Internet of Things (IoT) and implantable biomedical applications [1], there is a growing demand for ultra-low-power CMOS-based frequency synthesizers. The output signal of these synthesizers is used to generate on-chip clocks for digital systems [2] or provide carrier signals for communication and sensing systems [3]. Recent advancements in digital phase-locked loops (DPLL) [4], all-digital phase-locked loops (ADPLL) [5], and other variants of frequency synthesizers have successfully reduced the system-level power consumption to the order of several milliwatts for enhanced system integration. Consequently, reduction of VCO power consumption to sub-mW level in these applications, while maintaining satisfactory phase noise and frequency tuning range, is desirable.

In light of the low-voltage operation of class-D VCOs, there has been a growing research interest to implement low-power signal sources in the advanced CMOS nodes with scaled power supply. In some of the previous class-D VCO work presented in [6]–[8], a switch-based transistor model was used to derive the steady state waveform and identify the optimal values for the tank floating capacitors (C_F) and single-ended capacitors (C_{SE}) that achieve the lowest phase noise. Despite impressive phase noise and low-power consumption (sub-5 mW), a trade-off between increasing the tuning range and keeping the optimal phase noise performance across the tuning range has been noted in the prior class-D VCO designs. This is mainly because realization of C_F and C_{SE} by switching capacitors and tuning varactors does not allow to consistently enforce the optimum capacitance ratio C_F/C_{SE}.

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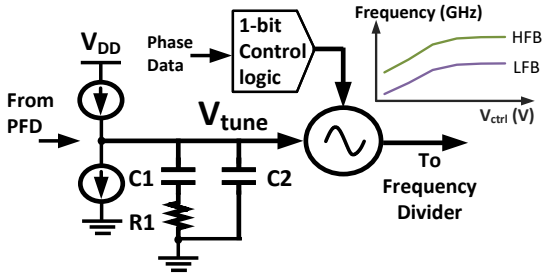

Fig. 1: Block diagram of VCO with one-bit switch in a phase locked loop.

Another design consideration for low-power VCOs is the two-point modulation capability when they are deployed in a PLL [9]. The two-point modulation can result in constant modulation sensitivity regardless of the loop bandwidth. It is widely adopted that using multiple switched capacitor banks together with small varactors increases the tuning range while maintaining a small tuning sensitivity (K_{VCO}) for loop stability consideration. However, multi-bit digital switches incorporated in previous CMOS VCOs to extend the tuning range, demand high-resolution logic circuits (e.g., ADCs) to control the switch states which add to the power consumption [10]. With a one-bit switch, a simple one-bit digital functional block (Bang-bang control logic) can be implemented to support two-point modulation as shown in Fig. 1. The implemented one-bit switch should also maintain low-phase-noise performance across the tuning range along with identical frequency tuning curves (invariant K_{VCO}) at low frequency (LFB) and high frequency (HFB) bands.

To address the aforementioned challenges, this paper presents a one-bit class-D VCO with a new tank architecture deploying varactors and RF chokes that alleviates the C_F/C_{SE} ratio variation by frequency. The presented VCO also achieves almost identical tuning characteristics, i.e., K_{VCO}, for both switching states. The rest of the paper is organized as follows. Section II conducts a comparative analysis of steady-state waveforms and their corresponding phase noise performance to highlight the importance of maintaining a constant C_F/C_{SE} ratio. Section III discusses the realization of the VCO focusing on a novel tank architecture with a constant C_F/C_{SE} ratio. Section IV presents the simulation and measurement results that justify the low-power and low-noise performance of the fabricated VCO. Section V concludes the paper.

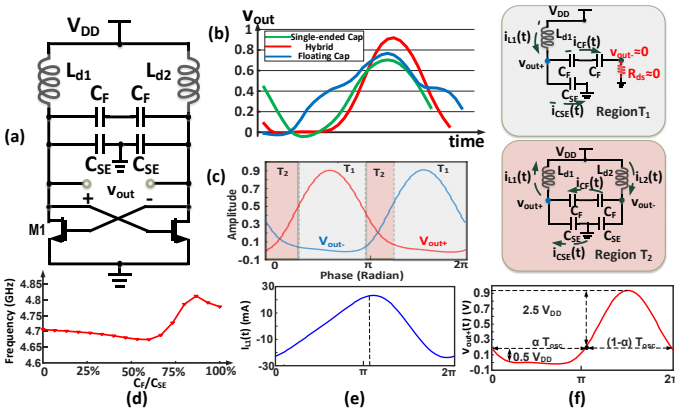

Fig. 2: (a) Block diagram of Class-D VCO with C_F and C_{SE}, (b) steady state waveforms under all three operational scenarios, (c) steady state oscillation waveform of hybrid condition and the corresponding circuit block diagrams, (d) oscillation frequency under under different C_F/C_{SE} ratios, (e) voltage and (f) current waveform under hybrid condition.

II. Optimum C_F/C_{SE} Ratio for Waveform Shaping

The class-D VCO with both C_F and C_{SE} in the oscillation tank is shown in Fig. 2 (a). The transistors are usually biased near threshold voltage so that for half of the period, there is no current in either side of the tank [7]. This low-voltage bias, upon satisfying the oscillator start-up condition, reduces power consumption and at the same time reduces the thermal noise contribution to the phase noise. Three operational scenarios of only C_{SE}, only C_F, and both C_F and C_{SE} present in the tank while the total capacitance is constant, can be perceived in Fig. 2(a). Consequently, three different steady state oscillation waveforms can be achieved as shown in Fig. 2 (b). It is observed that only under the hybrid condition with both C_F and C_{SE} in the tank at a certain C_F/C_{SE} ratio, the oscillation waveform can be boosted to close to $3V_{DD}$. Therefore, we focus on the high-swing waveform of hybrid condition and separate the waveform into two regions, T_1 and T_2, as shown in Fig. 2(c). The equivalent circuit for each region is shown with the same color on the side of Fig. 2(c). During region T_1, the transistor is pushed into triode region and is modeled as a small "ON" resistor on one side, whereas during region T_2 both transistors are in saturation region, which can be treated as open circuit. Therefore, two corresponding tank frequencies, i.e., $\omega_{\text{tank1}} = 1/\sqrt{L_d(C_{SE}+\frac{C_F}{2})}$ and $\omega_{\text{tank2}} = 1/\sqrt{L_d(C_{SE}+C_F)}$ exist during one oscillation period. As shown in Fig. 2(d), the simulated oscillation frequency remains relatively unchanged with respect to different C_F/C_{SE} ratios for an invariant $(C_F + C_{SE})$, therefore we can approximate:

$$\omega_{\text{osc}} \simeq \omega_{\text{tank2}}. \tag{1}$$

To find the optimum C_F/C_{SE}, the ratio between ω_{tank1} and ω_{tank2} should be calculated. Based on Fig. 2 (e,f), when $v_{\text{out+}}(t) = 0$ (region T_1), the inductor current i_{L1} is calculated as:

$$i_{L1}(t) = -I_0 + \frac{1}{L_{d1}} V_{DD} t, \quad 0 \le t \tag{2}$$

$$I_0 = \frac{1}{2}\frac{1}{L_d} V_{DD} \cdot \alpha \cdot T_{osc}, \tag{3}$$

$$T_{osc} = \frac{2\pi}{\omega_{\text{osc}}} = \frac{2\pi}{\omega_{\text{tank2}}}, \tag{4}$$

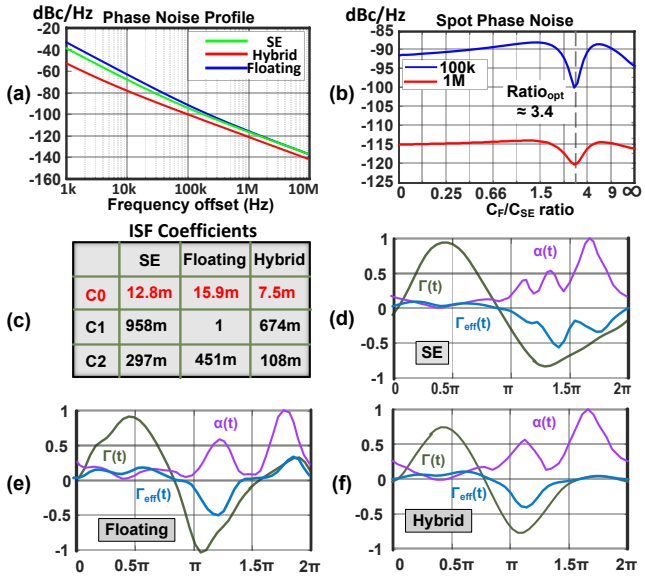

Fig. 3: (a) Phase noise profile under all three scenarios, (b) phase noise at 100kHz and 1MHz offset for various C_F/C_{SE} ratios in hybrid scenario, (c) table of coefficients of simulated ISF function. $\Gamma(t)$, $\alpha(t)$ and $\Gamma_{\text{eff}}(t)$ of (d) SE (e) floating, and (f) optimum ratio hybrid scenaios.

$$\frac{\omega_{\text{tank1}}}{\omega_{\text{tank2}}} = \frac{1}{2(1-\alpha)}. \tag{5}$$

In (5), α is the ratio of the duration of the region with linear current to oscillation period (T_{osc}) as illustrated in Fig. 2 (e). Thus, the current when $v_{\text{out+}}(t)) \neq 0$ can be approximated as:

$$i_{L1}(t) = I_0 \cos[\omega_{tank1}(t - \alpha T_{osc})], \quad \alpha T_{osc} \le t \le T_{osc}, \tag{6}$$

The voltage v_{out+} can be calculated by integrating the current flowing through the capacitor when $v_{\text{out+}}(t)) \neq 0$, which gives:

$$v_{out+}(t) = \frac{1}{(C_{SE}+\frac{C_F}{2})}\frac{I_0}{\omega_{tank1}}\sin[\omega_{tank1}(t-\alpha T_{osc})] + 0.5V_{DD}, \quad \alpha T_{osc} \le t \le T_{osc}, \tag{7}$$

According to Fig. 2(f) we approximate $0.5V_{DD}$ as the transition point between linear current region and sinusoidal current region. Therefore, the maximum V_{out+} can be expressed as:

$$V_{out+} = \pi V_{DD}\alpha\frac{\omega_{tank1}}{\omega_{tank2}} = \pi V_{DD}\frac{\alpha}{2(1-\alpha)}. \tag{8}$$

To boost the maximum swing to $3V_{DD}$, V_{out+} should be approximately $2.5V_{DD}$, for which α is 0.61, hence:

$$\frac{\omega_{\text{tank1}}}{\omega_{\text{tank2}}} = 1.28, \tag{9}$$

and the corresponding optimum C_F/C_{SE} ratio that leads to $3V_{DD}$ swing in the hybrid scenario is 3.5. Under this optimal ratio, the voltage swing is maximized.This optimum ratio is different than that reported in [11], [12] where an ideal sinusoidal signal and a tank including the coupling coefficient k between the inductors were considered, respectively.

Simulation results of phase noise profile for the three operational scenarios and spot phase noise for various C_F/C_{SE} ratios are depicted in Fig. 3(a) and (b), respectively. To evaluate the phase noise, we deploy the linear time-invariant model presented in [13]. Accordingly, the simulated impulse sensitivity function (ISF), $\Gamma(t)$, for the transistor noise is

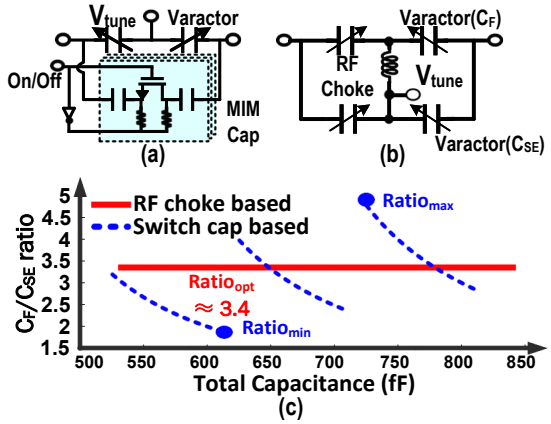

Fig. 4: Comparison of C_F/C_{SE} ratio with RF choke and switched capacitor

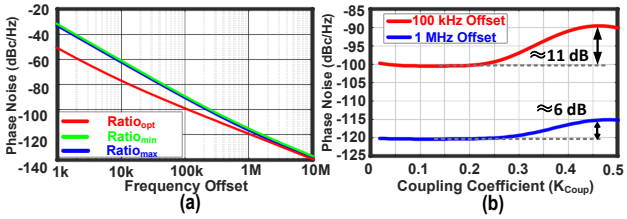

Fig. 5: (a) Phase noise profile for maximum, minimum and optimum ratio in Fig. 4 (c), (b) simulated spot phase noise at 100 kHz and 1 MHz offset vs coupling coefficient K_{coup}.

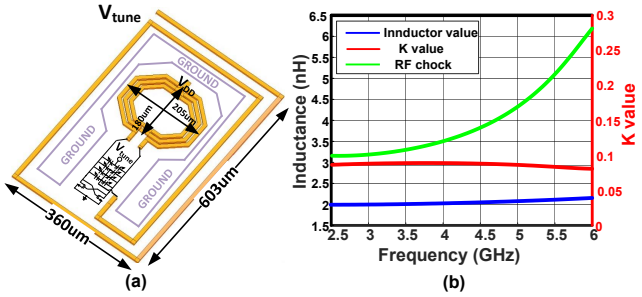

Fig. 6: (a) HFSS view of RF choke and L_d, (b) simulated inductance of RF choke and tank inductor and coupling coefficient K_{coup}.

extracted. The ISF Fourier coefficients, ISF time-domain function, noise modulating function (NMF) denoted by $\alpha(t)$, and resulted effective ISF for the SE, floating, and hybrid scenario under optimum capacitance ratio are depicted in Fig. 3 (c)-(f), respectively. The effective ISF (Γ_{eff}) is calculated as $\Gamma_{eff}(t) = \Gamma(t) \cdot \alpha(t)$ [13]. According to Fig. 3 (c), the optimum C_F/C_{SE} ratio in the hybrid scenario achieves the smallest Fourier coefficients of $\Gamma_{eff}(t)$, specially the DC term (C_0). This is because under maximized oscillation swing for a low-voltage bias, the amplitude of $\alpha(t)$ diminishes due to a decrease in the conduction angle, yielding smaller C_0 and thus 1/f noise up-conversion. As mentioned in [13], C_0 will directly impact the corner frequency of flicker noise. Therefore, the proposed optimum ratio not only impacts the suppression of thermal noise, but also helps to reduce the up conversion of flicker noise into PN.

III. Circuit Implementation

A. RF choke based floating capacitor

The conventional method for implementing SE and floating capacitors in VCO leverages continuous tuning varactors and

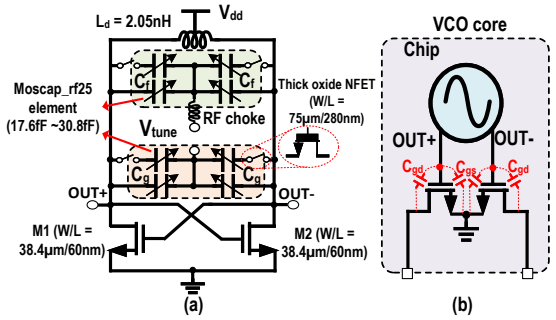

Fig. 7: Circuit of (a) implemented VCO and (b) open-drain buffer.

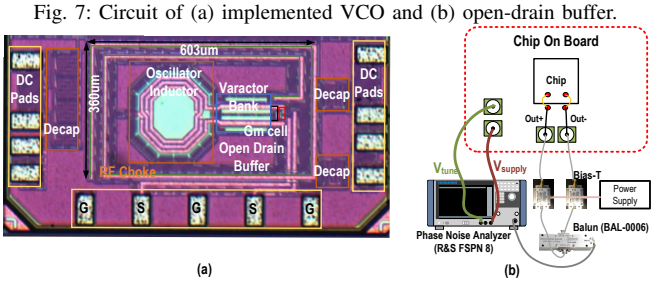

Fig. 8: (a) Chip photograph of implemented VCO and open-drain buffer, (b) measurement setup.

discrete switching capacitors, as illustrated in Fig. 4 (a). The continuous tuning varactors are regarded as SE capacitors, given that V_{tune} is considered as AC ground, whereas the discrete switching capacitors can be treated as floating capacitors because of the switching transistor's low turn-on resistance.The proposed realization using varactors for both floating and SE paths is shown in Fig. 4 (b). An RF choke is incorporated for the floating path and for the varactor implementation, a standard element varying from 17.6 fF to 30.8 fF is used with an array of 9 elements implemented for the SE bank and 31 elements for the floating bank, which enables precise control of the C_F/C_{SE} ratio. The simulated C_F/C_{SE} ratio for both designs is shown in Fig. 4(c) highlighting the advantage of proposed design in Fig. 4(b) over the conventional design in maintaining a constant optimum C_F/C_{SE} ratio.

The total Q factor of the VCO in Fig. 2(a) when the C_{SE} and C_F are designed based on Fig. 4(a) is calculated by:

$$\frac{1}{Q_{tot}} = \frac{1}{Q_L} + \frac{C_{\text{var}}}{C_{tot}}\frac{1}{Q_{\text{var}}} + \frac{nC_u}{C_{tot}}\frac{1}{Q_{\text{bank}}}, \qquad (10)$$

where Q_{tot}, Q_L, Q_{var}, and Q_{bank} are the quality factor of the tank, inductor, varactors, and switching capacitor bank and C_{tot}, C_{var}, C_u, and n are the total capacitance, varactor capacitance, switching capacitor bank, and the number of switches, respectively. In the proposed capacitive network design in Fig. 4(b), the total Q factor is determined by $1/Q_{tot} = 1/Q_L + 1/Q_{\text{var}}$ where the Q of the RF choke does not impact the differential fundamental oscillation. Although the Q factor of switching capacitor bank and varactor may vary by the deployed CMOS technology, the total Q is predominantly influenced by the Q factor of the inductor at frequencies below 10 GHz [14] ($Q_{tot} \approx Q_L$), hence a noticeable Q variation between Fig. 4(a) and Fig. 4(b) is not foreseen. In Fig. 5 (a), the simulated phase noise of $ratio_{min}$, $ratio_{max}$ and $ratio_{opt}$ in Fig. 4 (c) are plotted and compared.

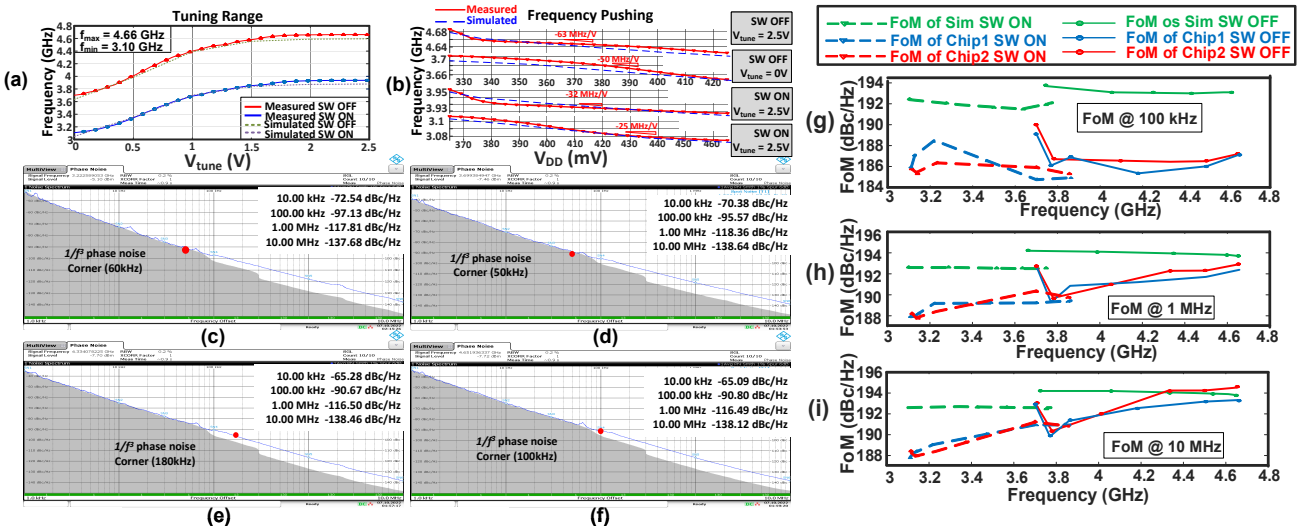

Fig. 9: Simulated and measured (a) tuning range for both SW on and off, (b) frequency pushing for both SW on and off at V_{tune} = 0 and 2.5V. Measured PN at (c) 3.22 GHz, (d) 3.70 GHz, (e) 4.33 GHz, (f) 4.65 GHz. Simulated and measured FoM of two chips at (g) 100 kHz, (h) 1 MHz, (i) 10 MHz offset.

TABLE I: Performance Summary and Comparison with State-of-the-Art

	Topology	Tech.	V_{DD} (V)	Frequency (GHz)	Tuning range (FTR) (%)	Power (mW)	PN @ (dBc/Hz)			FoM# @ (dBc/Hz)			FoM$_T$## @10MHz dBc/Hz	$1/f^3$ Corner (kHz)	Core area (mm^2)
							100kHz	1MHz	10MHz	100kHz	1MHz	10MHz			
This work	Class-D	65nm	0.33 / 0.36	3.10-4.66	**40.2**	**0.495**	-95.57	-118.36	-138.64	**187.20**	192.89	**194.52**	**206.6**	**50**	0.21
[7]	Class-D	65nm	0.4 / 0.5	3.0-4.8	46	4.0 / 6.8	-102†	-128†	-143.5	183.2	189.2	192*	205.26	800	0.15
[6]	Class-D	65nm	0.35	3.67-4.44	18.7	4.95 - 4.2	-104.4	-129.1	-150.5	188.7	193.5	194.9	200.34	230	0.12
[8]	Class-D	28nm	0.225	2.4	NA	0.171	-90.2	-115.9	-136†	185.5	191.1	191.0*	NA	800**	0.18
[15]	Class-C DCO	28nm	0.3	2.02-2.87	35	0.75	-93.98	-118.19	-133.98	184.4	188.1	184.4	199	60	0.14
[16]	Switching I_{DC}	40nm	0.5	4.0-5.0	22.2	0.58	-89	-113.99	-134.54	183.4	188.4	188.9*	195.83	250	0.14
[17]	Triple Coil VCO	180nm	1	4.2-4.6	9	7.4	-97**	-126.3	-149.3	181.11**	190.5	193.2	192.37	600**	0.52
[18]	Series Res VCO	55nm BiCMOS	1.2	9.96-10.9	9	600	-117	-138	-150**	189	190	182**	181.08	NA	0.54
[19]	Dual Core-VCO	22nm FinFet	1.1	7.1-16.8	80.6	13.5	NA	-116.1	-137.9	NA	186.1	187.6	205.7	1100	0.05
[20]	Class-E	180nm	0.7	4-4.45	10.6	4.9	-102.5	-129.5	-152.75	187.6	194.6	197.9	198.07	1100	0.23

$\text{FoM} = -\text{PN} + 20\log_{10}(f_0/\Delta f) - 10\log_{10}(P_{\text{DC}}/1\text{ mW})$

$\text{FoM}_{\text{T}} = \text{FoM} + 20\log_{10}(FTR/10)$

* FoM not mentioned for a particular frequency offset ** Estimated from measured PN plot

The phase noise of $ratio_{min}$ and $ratio_{max}$ are 10dB and 5dB higher than that of optimum ratio at 100 kHz and 1 MHz offset frequencies, respectively. Therefore it is evident that the inability of the conventional design in Fig. 4(a) to maintain the optimum ratio, adversely impacts the phase noise in a wideband VCO.

Although for the design in Fig. 4(b), the phase noise variation across the whole tuning range is substantially reduced, the coupling between the RF choke and the tank inductor should be meticulously evaluated. Fig. 5(b) illustrates that when the coupling coefficient between the two inductors, K_{coup}, exceeds 0.4, there is a noticeable deterioration in phase noise: an increase of 11 dB at 100 kHz offset and 6 dB at 1 MHz offset. Therefore, the layout of RF choke is characterized in the HFSS EM solver to identify the routing losses and mutual couplings. Since the purpose of RF choke is only to provide a floating point, the performance of VCO is not sensitive to its precise inductance value. Furthermore, to ensure a reliable floating condition for the varactors, a minimum inductance of 3 nH across the tuning range is considered and since the self-resonance frequency (SRF) of the RF choke is close to 10 GHz, on the higher end of the tuning, the inductance rises further to 6.5 nH which creates a higher impedance open circuit. By incorporating minimum 20-μm-thick distributed ground walls between the tank inductor and the choke, the RF choke is winded around the VCO core to achieve reduced K_{coup} and maintaining a compact area, Fig. 6(a). The tank inductance value of VCO core and RF choke, as well as coupling coefficient, K_{coup}, were simulated in HFSS EM solver and the simulation results are shown in Fig. 6(b). The tank inductor value stays invariant in the presence of RF choke and K_{coup} remains around 0.1 for the entire tuning range which does not degrade the phase noise according to Fig. 5(b).

B. One-bit switch to enhance tuning range

The completed schematic of this VCO is shown in Fig. 7(a). To boost the tuning range, a one-bit switch is incorporated for both SE and floating varactor pairs. The deployed switches are implemented by thick oxide transistors (W/L=75μm/280nm) to achieve a small "ON" resistance. The varactor pairs in the switching and non-switching branches are sized such that the C_F/C_{SE} ratio does not vary between "ON" and "OFF" states.

For reliable measurability, a differential open-drain buffer is also designed as shown in Fig. 7(b), which introduces extra capacitors to the LC tank. The parasitic C_{gs} =24 fF and C_{gd} =27 fF of the buffer can be treated as SE capacitor using the Miller effect.

IV. Measurement Results

This VCO is fabricated in 65nm bulk CMOS technology and the chip photograph is shown in Fig. 8(a) with a core area of $0.21mm^2$. Fig. 8(b) shows the measurement setup. Two bias-Ts are utilized to supply power to the open-drain buffer which is followed by a differential to single-ended balun that is fed into the R&S phase noise analyzer FSPN8. The tuning voltage is directly provided by the phase noise analyzer that

is further low pass filtered by on-board decoupling capacitors. The VCO draws 1.5mA from 330mV V_{DD} when Switch is off and 2.1mA from 360mV V_{DD} when Switch is on. Due to the loss associated with switching transistors, a higher V_{DD} is required when switch is on to ensure the oscillation startup.

As shown in Fig. 9 (a), when SW is ON, the tuning range is from 3.10 GHz to 3.93 GHz, and when SW is off, the tuning range is from 3.70 GHz to 4.66 GHz. The combined tuning range from 3.1 GHz to 4.66 GHz corresponds to 40.2% continuous frequency tuning. The tuning curves at lower and higher frequency bands are similar, leading to almost identical K_{VCO} for the same V_{tune} in either of the SW states which is critical for low-power PLL design according to Fig. 1. The frequency pushing for four different conditions of SW states and V_{tune} are measured and shown in Fig. 9 (b) which confirm relative robustness against power supply variations.

The phase noise profile is measured averaging 10 iterations for each frequency across the whole band as shown in Fig. 9 (c)-(f). The variation of PN in the $1/f^2$ region (due to thermal noise) across the tuning range is less than 2 dB at 1 MHz offset and less than 1 dB at 10 MHz offset, which confirms the effectiveness of the proposed design to maintain the optimum C_F/C_{SE} ratio. The simulated and measured FoM of two chip samples at various frequency spots are depicted in Fig. 9(g)-(i). Both chip samples attain similar values for PN and FoM, confirming the robustness against process variations. The FoM when SW is on is slightly lower than when SW is off due to a higher power consumption. The measured VCO exhibits a very low power consumption of only 0.495 mW, while achieving phase noise performances of -118.36 dBc/Hz and -138.64 dBc/Hz at 1 MHz and 10 MHz offsets, respectively. This results in best FoM of 192.89 and 194.52 dBc/Hz at 1 MHz and 10 MHz offsets respectively. The performance comparison with state-of-the-art is summarized in Table I. According to Table I, this VCO exhibits an state-of-the-art performance in terms of frequency tuning range, power consumption, and phase noise, while attaining high FoM at 10 kHz - 10 MHz offset frequencies and a very low $1/f^3$ corner frequency.

V. Conclusion

This paper introduced a single-switch class-D VCO capable of improving the power efficiency and maintaining the phase noise performance. It was shown that the largest voltage swing from a class-D VCO is only achievable when the oscillator tank encapsulates both single-ended (SE) and floating capacitors at a certain ratio. Moreover, a novel hybrid varactor bank technique, comprising both floating and single-ended varactors was introduced which was capable of shaping waveforms to achieve higher amplitudes. The novel implementation of floating varactors using an on-chip RF choke was demonstrated, highlighting the practicality of the proposed approach. The method's effectiveness was confirmed through simulations and multiple chip measurements. Given the presented attributes, this VCO is deemed suitable for low-power applications.

Acknowledgments

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