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Low-voltage short-channel MoS_2 memtransistors with high gate-tunability

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Neuromorphic hardware promises to revolutionize information technology with brain-inspired parallel processing, in-memory computing, and energy-efficient implementation of artificial intelligence and machine learning. In particular, two-dimensional (2D) memtransistors enable gate-tunable non-volatile memory, bio-realistic synaptic phenomena, and atomically thin scaling. However, previously reported 2D memtransistors have not achieved low operating voltages without compromising gate-tunability. Here, we overcome this limitation by demonstrating MoS_2 memtransistors with short channel lengths < 400 nm, low operating voltages < 1 V, and high field-effect switching ratios > 10^4 while concurrently achieving strong memristive responses. This functionality is realized by fabricating back-gated memtransistors using highly polycrystalline monolayer MoS_2 channels on high-κ Al_2O_3 dielectric layers. Finite-element simulations confirm enhanced electrostatic modulation near the channel contacts, which reduces operating voltages without compromising memristive or field-effect switching. Overall, this work demonstrates a pathway for reducing the size and power consumption of 2D memtransistors as is required for ultrahigh-density integration.

Introduction

The rapid ascent of artificial intelligence (AI) and machine learning (ML) has imposed unprecedented energy demands on existing digital electronic hardware. As a stopgap measure, graphics processing units (GPUs) have provided incremental computational efficiencies to support the training and development of AI/ML based on deep neural networks (DNNs) [1, 2]. However, GPUs continue to rely on silicon complementary metal–oxide–semiconductor (CMOS) integrated circuits and von Neumann computing architectures, which require nearly constant transfer of data between the memory and processing units [3]. In the limit of large data that underly the training of DNNs, the von Neumann bottleneck limits computing performance and requires unsustainable energy consumption [4, 5]. Therefore, neuromorphic hardware that takes inspiration from the human brain has attracted significant attention due to its potential for co-locating memory and processing functionality in a manner that promises to dramatically reduce power consumption, particularly for AI/ML applications [6, 7].

Emerging neuromorphic devices include memristors, phase change memory, ferroelectric switches, and synaptic transistors. Among these options, memristors are particularly prominent due to their effectiveness in implementing the matrix multiplications that underlie many AI/ML algorithms. Memristors are two-terminal devices that impart non-volatile memory characteristics through diverse mechanisms including conductive filament formation and rupture, charge trapping, phase changes, and defect migration [8–14]. Although memristors enable dense integration into compact crossbar arrays, their two-terminal structure fails to achieve the highly interconnected, multi-terminal nature of biological neurons, which each typically has hundreds to thousands of synaptic connections. In contrast, the synaptic transistor gains some bio-realism compared to memristors with a three-terminal structure where the drain

and gate electrodes serve as pre-synaptic modulatory terminals [15–17]. However, synaptic transistors rely on charge-trapping mechanisms that require complex time control over the pulsing of the drain and gate terminals, ultimately limiting adaptive learning and high-density integration. On the other hand, the memtransistor concurrently possesses volatile and non-volatile responses in manner that provides synaptic tunability in addition to multi-terminal architectures that more faithfully mimics the interconnectivity of the brain [7, 8]. In particular, memtransistors provide gate-tunable non-volatile memory and learning behavior that combines the device characteristics of a memristor and a field-effect transistor [18–20].

The gate-tunable synaptic phenomena in memtransistors are enabled by the strong electrostatic modulation that is inherent to two-dimensional (2D) materials due to weak screening and reduced density of states that also underlie other superlative electronic, optical, and chemical properties [21–26]. While the memtransistor device concept has been generalized to a wide range of 2D materials and van der Waals heterojunctions, most of these prototypes show large operating voltages [7, 15, 18–20, 27–30], which is often attributed to the fact that stochastic processes in inhomogeneous media generally do not follow linear scaling behavior with decreasing channel dimensions [33]. The scaling behavior of memtransistors involving polycrystalline MoS_2 is further complicated by incomplete understanding of the role of defect migration and charge trapping near and within grain boundaries, resulting in spatially inhomogeneous field effects from the gate voltage [34].

Here, we explore back-gated memtransistors in the scaling limit where the channel length is shorter than the grain size in monolayer polycrystalline MoS_2 grown by chemical vapor deposition (CVD). The use of the back-gate architecture, high-κ gate dielectric layer, and small channel length (L < 400 nm) results in strong memristive responses at low operating voltages < 1 V while maintaining high transistor ON/OFF ratios exceeding 10^4. The critical requirement is that the channel width (W) be larger than the MoS_2 grain size such that at least one of the grain boundaries intersects with the contact metal edges. Furthermore, the degree of field-effect conductance modulation depends on electrostatic coupling of the gate potential to the metal–semiconductor contacts. In this regard, back-gating is critical to circumvent the screening experienced with top-gating by the metal contacts, which is an effect that is exacerbated in the short-channel limit. This advantage of back-gating for short-channel memtransistors is elucidated through finite-element simulations, which confirm significant control over the electrostatic potential in the depletion region formed near the Schottky barrier at the source electrode. Overall, this work provides insights into the switching mechanisms in scaled memtransistors that can guide future efforts aimed at achieving high-density, low-power neuromorphic hardware architectures.

Results and discussion

Back-gated memtransistor devices were fabricated by transferring CVD-grown polycrystalline monolayer MoS_2 onto the pre-patterned gate terminal and gate dielectric layer. The gate electrodes were fabricated using electron-beam lithography (EBL) and metal evaporation (2-nm-thick Ti adhesion layer, 20-nm-thick Au, 2-nm-thick Al seeding layer) on p-doped Si substrates (with 300-nm-thick thermal oxide) followed by atomic layer deposition (ALD) to grow the 20-nm-thick Al_2O_3 gate dielectric layer. Note that the 2-nm-thick Al layer on top of the Au electrode oxidizes upon removal from the evaporator chamber, which facilitates its use as a seeding layer for ALD. The gate width (5 μm) is designed to be larger than the channel length to ensure that the gate overlaps with the source and drain contact edges, as shown in Fig. 1(a). MoS_2 films were grown using a previously reported CVD method [20] and then transferred from the sapphire growth substrate onto the pre-patterned chip (see Methods section). The source and drain Ti/Au (2/60 nm) electrodes were subsequently patterned by EBL, and the MoS_2 channel width was defined with reactive ion etching (RIE) (see Methods section).

Various characterization methods were employed to assess the structure and properties of the polycrystalline monolayer MoS_2 films. High crystallinity and monolayer thickness were verified with Raman spectroscopy, as noted by the gap spacing of 19 cm^{-1} between the characteristic E^1_{2g} and A_{1g} vibrational modes [Fig. 1(b)]. Photoluminescence spectroscopy likewise confirmed a high-quality monolayer MoS_2 film with a peak intensity at 1.86 eV (Fig. S1). To quantify grain size distribution, lateral force microscopy (LFM) was employed, which measures the lateral deflection of an atomic force microscopy (AFM) tip and provides visual contrast of grain boundaries in polycrystalline MoS_2 films resulting from differences in frictional coefficients on the atomically flat basal planes compared to the surrounding grain boundaries [Figs. 1(c, S2)]. In this manner, LFM imaging revealed the grain size distribution with a mean grain size of 1.2 ± 0.4 μm [Fig. 1(d)].

Electrical characterization of the back-gated MoS_2 memtransistors is summarized in Fig. 2. First, the family of output curves in Figs. 2(a), S3, and S4 exhibits field-effect tuning of the current by a factor of 10^3–10^5 (see Fig. S7 for the transistor ON/OFF ratio). The excellent gate control over the channel conductance can be attributed to the back-gated architecture in combination with the weak screening in monolayer MoS_2. Second, the output curves exhibit characteristic bipolar resistive switching, which manifests itself as pinched hysteresis loops when sweeping the drain voltage bias (V_D) at various gate voltage biases (V_G) for devices with an L and W of 370 nm and 20 μm, respectively. In the forward-bias regime, the device initially starts in a low-resistance state (LRS) and

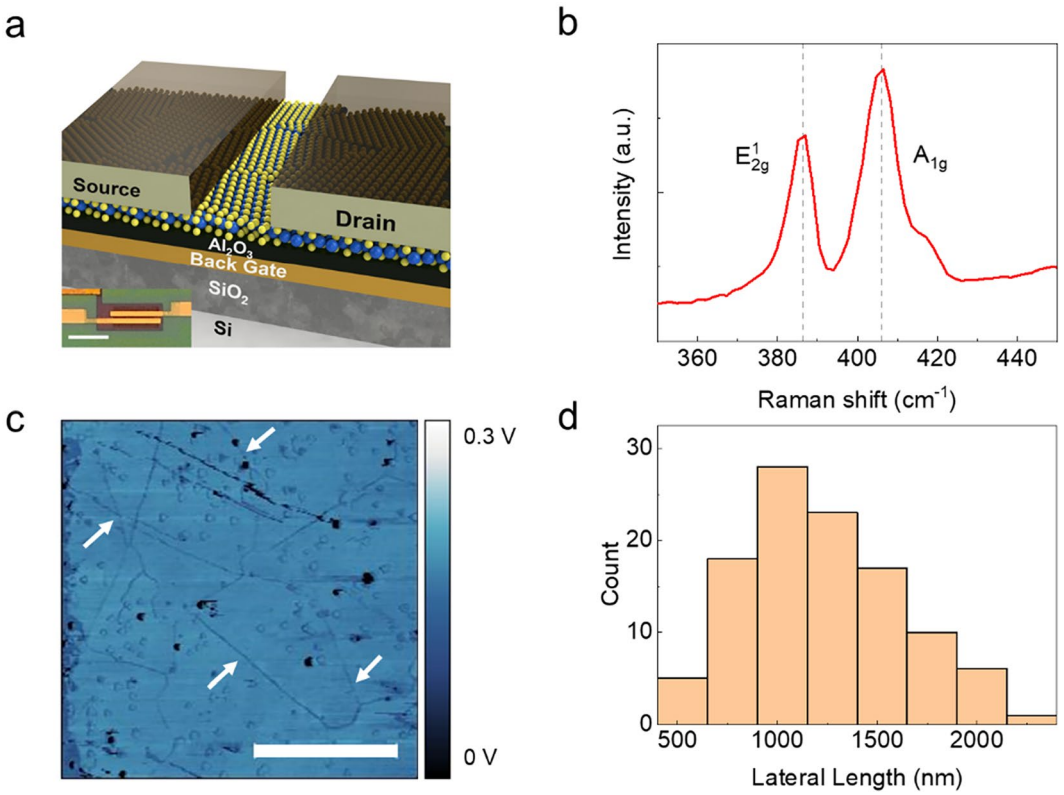

Figure 1: (a) Device schematic of a back-gated, short-channel MoS_2 memtransistor. Inset: An optical micrograph of a representative device. Scale bar is 10 µm. (b) Raman spectrum for the MoS_2 monolayer film. A peak gap spacing of ≈19 cm^{-1} indicates monolayer MoS_2 of high crystalline quality. (c) Lateral force microscopy of the MoS_2 monolayer polycrystalline film. White arrows are indicating the darkened grain boundaries. Scale bar is 2 µm. (d) Histogram of the grain size distribution for 108 measured grains. These statistics reflect a mean grain size of 1.2 ± 0.4 µm.

then switches to a high-resistance state (HRS) as the drain voltage is returned to zero, producing a clockwise loop. In the reverse-bias regime, the device maintains the HRS from previous programming and similarly switches in a clockwise fashion back to LRS as the negative bias is attenuated. This clockwise directionality in both the forward-biased and reverse-biased regimes is consistent with previous work on dual-gated short-channel MoS_2 memtransistors with Al_2O_3 as one of the gate dielectric layers [19]. The memristive switching ratio (I_{LRS}/I_{HRS}) at V_D = 0.1 V increases with decreasing V_G in the range of 10–300 (Fig. 2(a), S6) [15, 18]. The overall shape of the memristive loop is further elucidated by plotting the evolution of the memristive switching ratio (I_{LRS}/I_{HRS}) at all values of V_D (Figs. S3, S4). Smaller devices with L = 100 nm that are biased at low operating voltages (V_D < 0.5 V) also show high I_{LRS}/I_{HRS}, suggesting that the reduction in channel length does not adversely impact the memristive behavior, highlighting a non-linear scaling behavior in memtransistors based on polycrystalline monolayer MoS_2 (Figs. S3, S4). Lastly, the output characteristics in Fig. 2(a) show a similar asymmetry observed in previously reported MoS_2 memtransistors [19]. Specifically, the drain current in the forward-bias mode is greater than in reverse-bias, suggesting a similar charge transport mechanism to that of dual-gated memtransistors [19], as will be discussed later.

The low-voltage memtransistor device also shows robust endurance and retention behavior. Figure 2(c) displays the endurance behavior with minimal cycle-to-cycle deviations for 80 cycles. The corresponding LRS and HRS states extracted at V_D = 0.1 V maintain a steady switching ratio > 10. The two programmable states also show stable retention [Fig. 2(d)]. In particular, the device was programmed in the LRS and HRS states, and the readout current was collected at V_D = 0.1 V every 30 s for an 8 h measurement duration. Extrapolation suggests non-volatile memory retention for greater than 1 year (Fig. S5) [44].

Pulse measurements further reveal the tunable synaptic learning behavior of the low-voltage memtransistors. A V_D pulse train consisting of 100 write pulses, each with a 70 ms duration, was applied to the drain terminal, while the change in conductance was measured by interleaved read voltage pulses (V_D = 0.2 V, duration = 70 ms). The source was grounded, and the gate voltage was held constant for all measurements. Consistent with the clockwise memristive loop and asymmetry of the hysteresis curves in Fig. 2(a), negative

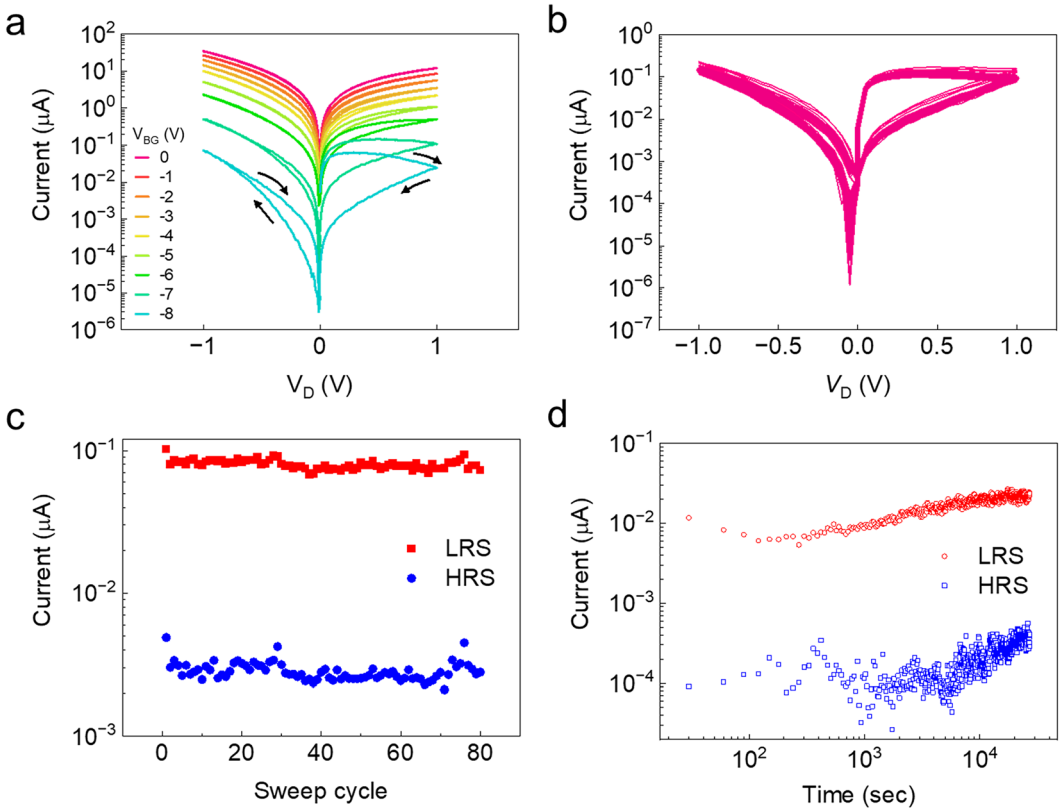

Figure 2: (a) Output characteristics for a MoS_2 memtransistor with $L = 370$ nm, showing a memristive switching ratio ranging from 10–100. (b) Memtransistor endurance testing at $V_G = -8$ V for 80 cycles. (c) Extracted LRS and HRS values (at $V_D = 0.1$ V) from the endurance cycling in (c). (d) Retention behavior for LRS and HRS at a read voltage of $V_D = 0.1$ V.

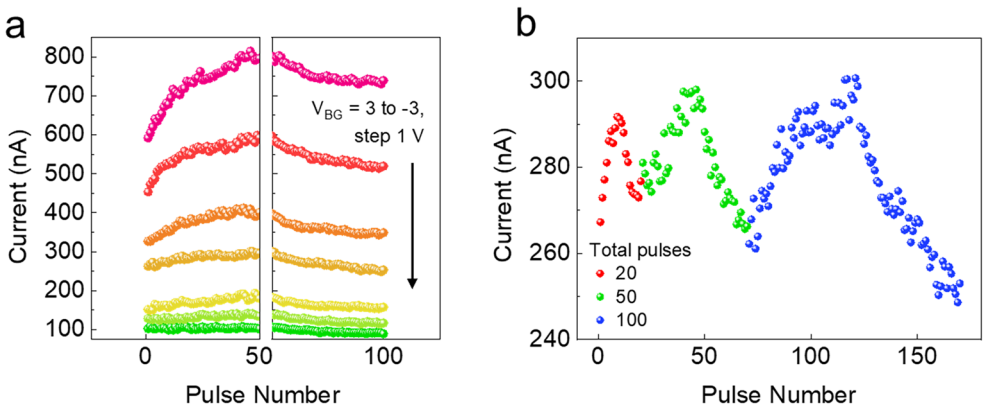

Figure 3: (a) Synaptic learning curves generated from a pulsing scheme of 70 ms pulse width, $V_D = -5$ V pulse amplitude for LTP, and $V_D = 2$ V pulse amplitude for LTD. Varying V_G during pulsing enables changes in the initial learning rate. (b) Learning curve behavior as a function of pulse number. Increasing number of LTP/LTD pulses increases the dynamic range achieved.

write pulses ($V_D = -5$ V) achieved long-term potentiation (LTP), and positive write pulses ($V_D = 2$ V) achieved long-term depression (LTD). The resulting learning curves illustrated in Fig. 3(a) highlight the effects of the gate electrode on learning behavior. First, V_G modulates the post-synaptic current with dynamic tunability over an order of magnitude ($I_D \approx 88$–815 nA). The ability to tune the range of accessible resistive states by the gate voltage terminal without changing amplitude and duration of the programming pulses holds practical use for dynamic neural network applications [31]. Second, the qualitative change in the learning curve shape (i.e., degree of non-linearity) with V_G can be exploited for AI/

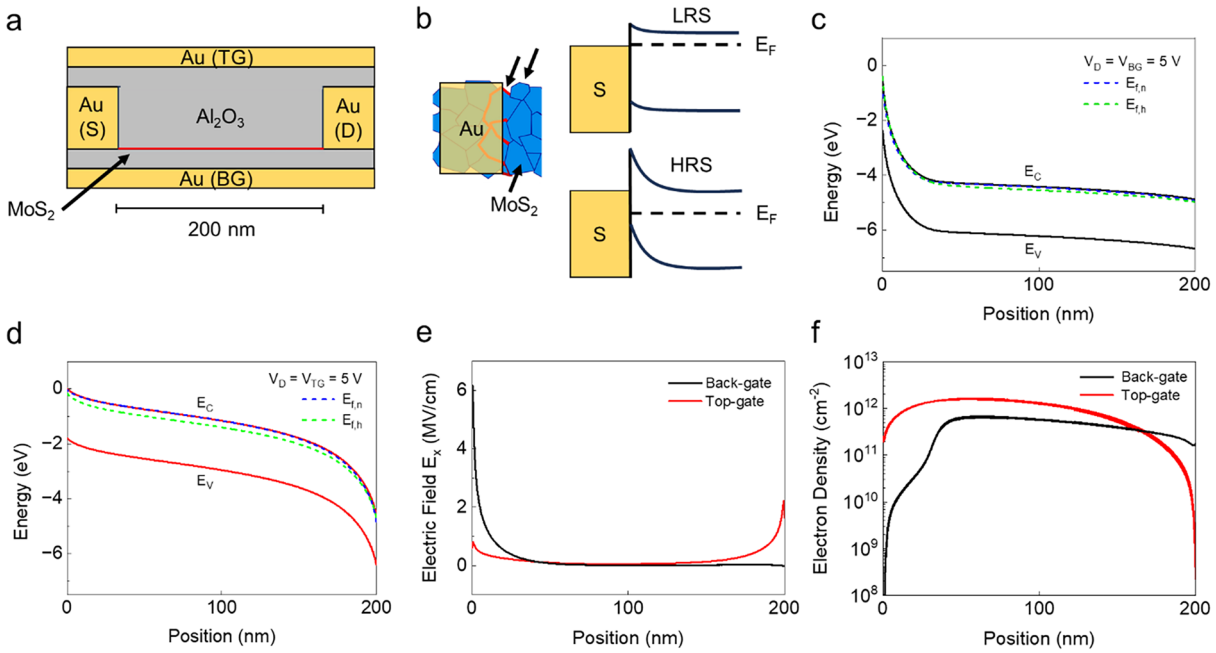

Figure 4: (a) Simulated device structure with channel length $L = 200$ nm. (b) Schematic illustrating switching between LRS and HRS at the source contact, specifically at the multiple contact-grain boundary interfaces near the channel. The yellow region is the contact, and the blue region is the MoS_2 channel. The top arrows indicate grain boundaries, where the red grain boundaries participate in resistive switching. (c) Band diagram along the channel for the back-gated design at $V_D = V_{BG} = 5$ V. A pronounced pinch-off region exists, which suggests that the dominant switching occurs at the depleted source contact. (d) Band diagram along the channel for the top-gated design at $V_D = V_{TG} = 5$ V. No pronounced pinch-off region is apparent. (e) Lateral electric field along thee MoS_2 channel for the back-gated and top-gated cases. (f) Electron density concentration along the channel for the back-gated and top-gated cases. Compared to the top-gated design, the back-gated design experiences a prominent depletion region with lower carrier concentration near the source contact.

ML accelerator applications where a tunable learning rate is desirable in the context of continuous learning [20, 41].

The dynamic range of states (calculated by dividing the highest read current by the lowest read current) during the learning process can also be tuned by modifying the number of applied write pulses. Earlier top-gated, short-channel memtransistors were programmed with 200, 400, and 1000 total write pulses, resulting in a fourfold, sevenfold, and 12-fold change in the analog ON/OFF ratio, respectively [32]. However, two outstanding challenges remained. First, the increase in dynamic range was at the expense of increasing the number of write pulses by fivefold. Such excessive electrical stress can cause degradation in 2D devices that impact endurance and overall reliability [35–38]. Second, normalization of the dynamic range with the number of write pulses yields a pulse efficiency of 2.0%, 1.8%, and 1.2% with increased number of pulses. In contrast, Fig. 3(b), shows a series of learning curves generated under the same voltage pulse conditions described above with the gate grounded where the number of total write pulses is varied among 20, 50, and 100, equally divided between LTP and LTD processes. While the absolute dynamic ranges are only modulated by a factor of 1.09, 1.12, and 1.21, respectively, the total number of pulses applied are an order of magnitude smaller than the top-gated incumbent design. Thus, the pulse efficiencies in this work are calculated to be 5.4%, 2.2%, and 1.2%, which surpass those of the top-gated memtransistors [32]. This improved synaptic behavior can be attributed to enhanced electrostatic coupling under the contact region from the back-gate, as discussed below.

Finite-element simulations were performed through COMSOL to elucidate the physical mechanisms that underlie the high performance of scaled back-gated memtransistors. Figure 4(a) illustrates a dual-gated memtransistor geometry for a direct comparison of the effects of the two gates. The top-gate and back-gate are 20-nm-thick Au, the source and drain contacts are 60-nm-thick Au, and the thickness of back-gate and top-gate Al_2O_3 dielectric are 20 nm and 80 nm, respectively. Additional materials parameters are delineated in Table S1. For simplicity, the top-gate oxide was specified to be thicker than the back-gate dielectric thickness due to the height of the source and drain contacts. Below we analyze the electrostatic potential variation near the intersection of the metal contact and the semiconductor channel (within the Debye length) due to its importance in modulating carrier injection across the Schottky junction.

The calculated conduction and valence band energies, lateral electric field, and electron density for the back-gated and top-gated configurations are provided in Fig. 4(c–f) at the biasing condition of $V_D = V_G = 5$ V. A noticeably stronger depletion region is formed near the source in the back-gated

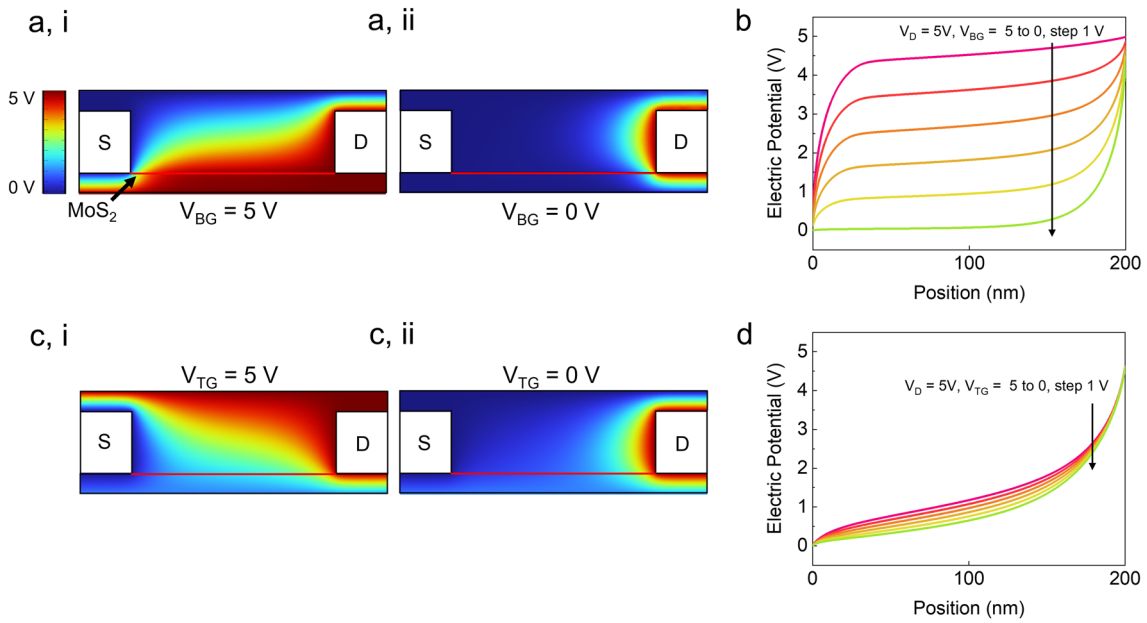

Figure 5: (a) i. 2D map (excluding metal contacts and gates) of the electrostatic potential in the back-gated device at $V_D = 5$ V and $V_G = 5$ V. ii. 2D map of the electrostatic potential in the back-gated device at $V_D = 5$ V and $V_G = 0$ V. (b) One-dimensional electrostatic potential profile along the MoS_2 channel of the back-gated device at $V_D = 5$ and varying V_G. (c) i. 2D map (excluding metal contacts and gates) of the electrostatic potential in the top-gated device at $V_D = 5$ V and $V_G = 5$ V. ii. 2D map of the electrostatic potential in the top-gated device at $V_D = 5$ V and $V_G = 0$ V. (d) One-dimensional electrostatic potential profile along the MoS_2 channel of the top-gated device at $V_D = 5$ and varying V_G.

device compared to the top-gated case, which leads to a larger lateral electric field (E_x) near the source edge in the back-gated case compared to the top-gated case. Moreover, the electron density (n) shows a sharp decline near the source in the back-gated case. Consequently, the reverse-biased source is more resistive than the drain for $V_D > 0$ V, and the larger electric field assists in memristive switching near the source. These results suggest that the source contact is where the dominant switching occurs and serves as the bottleneck for charge injection at $V_D > 0$ as illustrated in Fig. 4(b).

Previous reports have suggested a defect-migration-mediated resistive switching mechanism facilitated by grain boundaries in polycrystalline monolayer MoS_2 memtransistors [18–20, 34]. To achieve that condition, the channel is only required to be wider than the grain size, which allows the channel length to be smaller than the grain size. Since our devices meet this condition, dynamic tuning of the Schottky barrier height results in memristive switching at the channel-contact interface [39]. In addition, our Al_2O_3 gate dielectric was grown at a low temperature 100 °C, which broadens the trap state distribution in the alumina bandgap, and in turn dopes the MoS_2 under high electric fields [40]. Smaller channel dimensions and higher electric fields at the source contact thus increase the Schottky barrier height when the Schottky diode at source is reverse-biased ($V_D > 0$ V), leading to a clockwise switching direction in contrast to the counter-clockwise switching direction in memtransistors with larger $L > 5$ μm [18].

Additional COMSOL simulations reveal enhanced gate-tunability across the entire channel including the source contact for the back-gated case compared to the top-gated case. Figure 5(a) and (c) provide 2D electrostatic potential maps of the back-gated versus top-gated cross-sectional device structures at $V_G = 5$ V (left side) and $V_G = 0$ (right side) with constant $V_D = 5$ V. The 2D maps exclude the contacts for clarity. The critical differences between the back-gate and top-gate cases become apparent by looking at the potential along the MoS_2 channel [Fig. 5(b) and (d)]. As shown in the 1D profiles, the gate voltage has a much larger control of the channel potential in the back-gated case compared to the top-gated case, which experiences greater screening from the source contact. Because the variation in potential at the source contact is more pronounced in the back-gated case, it favors effective gating of the memristive Schottky barrier at the source edge, ultimately leading to a large memristive loop with high gate-tunability [42, 43].

Previously reported memtransistors have shown a tradeoff between operating voltage, switching ratio (memristor ON/OFF), and field-effect gating (transistor ON/OFF). In particular, Fig. 6 plots the transistor gate-tunability versus the memristive switching ratio where both metrics are normalized by their operating voltages for previously reported memtransistors (operating voltages are presented in Table S2). Some of the previous memtransistors based on CVD polycrystalline monolayer

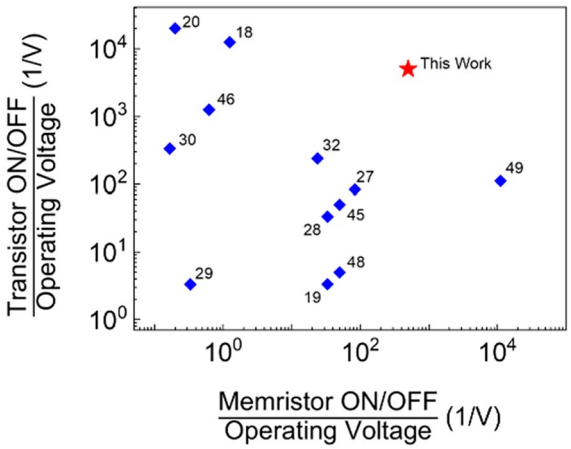

Figure 6: Comparison of operating-voltage-normalized transistor gate-tunability versus memristive switching ratio for the memtransistor device in this work compared to literature precedent (the reference numbers are indicated next to each point on the plot).

MoS_2 also reported large memristive switching ratios and high gate-tunability, but with high operating voltages of 30–80 V due to larger *L* and thicker gate dielectrics [15, 18–20, 29]. Few-layer or bulk nanosheets have also shown memtransistor behavior. However, thicker channels limit the gate-tunability [45–49]. Similarly, bulk oxides and one-dimensional carbon nanotubes have also been explored for memtransistors, but have not achieved concurrently high memristive and transistor switching ratios at low operating voltages [30, 50]. Lastly, efforts to reduce operating voltages through smaller device dimensions have only employed top gates, which leads to screening of the gate field near the contacts that compromises gate-tunability [27, 32]. In contrast, our devices that combine a local back-gate architecture with a channel length shorter than and a channel width greater than the grain size simultaneously achieve high memristive switching ratios, high gate-tunability, and low operating voltages that outperform incumbent devices [27, 32]. The integration of thin high-κ dielectrics also represent a design improvement compared to previously reported back-gated MoS_2 memtransistors [18–20]. Future efforts can likely further improve memtransistor performance metrics by minimizing grain size and achieving thinner and more crystalline gate dielectrics through the use of more advanced ALD seeding layers [34, 51, 52].

Conclusions

In this study, we have demonstrated low-voltage short-channel MoS_2 memtransistors with concurrently high memristive switching and transistor gate-tunability compared to incumbent memtransistor designs. In particular, we implement a channel geometry where the channel width is larger than the MoS_2 grain size to ensure grain boundary intersections with the metal contact edges even when the channel length is reduced below the grain size. Utilizing a back-gated design with thin high-κ dielectrics minimizes screening to enable strong electrostatic coupling between the gate and the metal–semiconductor junction to facilitate Schottky barrier modulation for enhanced memristive switching and gate-tunability. Simulations elucidate the differences in electrostatic, band energy, and charge carrier profiles between back-gated and top-gated designs to pinpoint the enhanced device performance obtained with the back-gated design. Overall, this work provides insight into the key parameters that control memtransistor scaling, thus informing efforts aimed at achieving high-density neuromorphic circuits and systems.

Methods

MoS_2 chemical vapor deposition

Continuous polycrystalline films of monolayer MoS_2 were synthesized by chemical vapor deposition (CVD) using sulfur powder (Millipore-Sigma, 99.98%) and molybdenum trioxide powder (MoO3, 99.98% trace metal, Sigma-Aldrich) following a previously reported method [20]. MoS_2 growth was performed on c-plane sapphire substrates cleaned by ultrasonication with acetone and isopropyl alcohol.

Fabrication of MoS_2 memtransistors

MoS_2 films were transferred to pre-patterned gate electrodes on Si substrates through a previously reported wet transfer process [20]. Memtransistor devices were subsequently patterned by electron-beam lithography (Raith Voyager 100) using a PMMA mask followed by metal evaporation (Denton Vacuum Explorer 14) and liftoff in acetone. Dry etching (Samco RIE-10NR) was used to de-scum and etch MoS_2 to define the channel regions [15, 18]. Atomic layer deposition (ALD) of the Al_2O_3 gate dielectric was performed at 100 °C using H_2O and trimethylaluminum precursors (Cambridge Nanotech ALD S100).

Material characterization

CVD films were screened for coverage and monolayer growth quality using optical microscopy, Raman spectroscopy, and photoluminescence spectroscopy (XploRA PLUS). Raman and photoluminescence measurements used a 532 nm laser with 1800 gr/mm and a 100X objective. Lateral force microscopy (LFM) measurements were performed under contact-mode atomic force microscopy (Asylum Cypher AFM) to characterize the film quality and quantify grain size distribution. Soft and thin LFM tips (NanoAndMore PPP-LFMR) were used with dimensions of 48 μm × 225 μm, ≈ 0.2 N/m force constant, and ≈ 23 kHz resonant frequency. Grain size statistics were determined

by measuring the flake lateral size using Gwyddion and plotted in Origin.

Electrical measurements

Electrical measurements were conducted in a vacuum probe station (pressure $\approx 5 \times 10^{-5}$ Torr) at room temperature using a LakeShore CRX 4 K probe station. Voltage sweep, endurance, retention, and pulse tests were measured using a Keithley 4200A-SCS Parameter Analyzer and homebuilt LabVIEW programs.

COMSOL finite-element simulations

Finite-element simulations were employed to quantify the relationship between charge distribution and potential by solving the Poisson equation, $\nabla^2\Phi = -\rho/\varepsilon$, which calculates the potential spatial distribution within the device. Φ signifies the potential, ρ represents the charge density, and ε is the dielectric constant. In contrast to other software packages, COMSOL Multiphysics® software streamlines the modeling workflow by automatically computing the Schottky barrier height after defining the work function and metal contact-related boundary conditions specified in Table S1. The Schottky barrier height Φ_B, is calculated as $\Phi_B = \Phi_M - \chi$, where Φ_M is the metal contact work function (Au) and χ is the semiconductor electron affinity (MoS_2). Subsequent calculations assumed that the device adheres to a drift–diffusion model without quantum effects, thus allowing classical charge carrier transport under the contacts and inside the channel.

Author contributions

S.E.L. and T.T.Z. contributed equally to this work. S.E.L., V.K.S., and M.C.H. conceived the idea and designed the experiments. S.E.L. and T.T.Z. synthesized and characterized the materials, fabricated the devices, and performed the measurements and analysis. R.W. performed the electrostatic potential simulations. All authors discussed the results and wrote the manuscript.

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Data availability

Data will be made available on reasonable request.

Declarations

Conflict of interest The authors declare that they have no conflict of interest.

Supplementary Information

The online version contains supplementary material available at https://doi.org/10.1557/s43578-024-01343-3.

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