A Triple-Band, High DC-to-RF Efficiency, Multicore VCO With a Dual-Path Inductor and Mode-Switching Capacitor

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***Abstract*— This article introduces an innovative four-port dual-path inductor designed to deliver two distinct inductance values to the resonator of a voltage-controlled oscillator (VCO). The switching between the inductor's two excitation modes, even and odd, is determined by the differential excitation's input polarity, eliminating the need for a series switch. Thus, the inductor has a high-quality factor (Q) in both modes. The inductances in these modes can be independently set based on desired frequencies. This inductance change achieves coarse frequency tuning, while fine-tuning is realized by a conventional 2-bit capacitor bank with a small-size varactor. This inductor is well suited for designing multiband VCOs aimed at widely spaced operation frequency bands. Apart from the inductance change, a particular case of mode-switching capacitor is employed to extend to another frequency band in between the low and middle bands, achieving triple-band oscillation. As a result, this article presents two VCOs designed using the proposed inductor: one in class-D biasing in a 65-nm CMOS process and another with class-B biasing in a 180-nm BiCMOS process. Both VCOs successfully oscillate across three distinct frequency bands, centered at 19, 28, and 36 GHz, while maintaining outstanding phase noise and minimal power consumption. Measurement results show good match with simulation, resulting in a peak figure of merit (FoM) of 185.7 dBc/Hz at 18.5 GHz, and occupy 0.088-mm^2 (250 × 350 μm) area in both processes.**

***Index Terms*— 5G, class-B, class-D, efficient, low-phase noise, multiband, SATCOM, voltage-controlled oscillator (VCO).**

I. Introduction

FREQUENCY bands over 24 GHz have an abundance of spectrum, allowing for high capacity, high throughput, and low latency. The rise of 5G is driving demand for multiband transceivers that can support multiple standards on the same chip [2]. Different regions in the world have diverse frequency allocations, such as the 28-, 39-, and 47-GHz bands in North America; the 26- and 28-GHz bands in Europe; and the 24.25–29.5-GHz and 37–43.5-GHz bands in Asia. These allocations underscore the adaptability, extended coverage, and efficient spectrum use, which are essential for the global deployment of 5G bands [3], [4]. There has been significant interest in the design and implementation of mm-wave 5G circuits, especially in voltage-controlled oscillators (VCOs) due to their crucial role in signal generation for multiband applications. Typically, multiband oscillators show superior performance compared with wideband oscillators, especially in the K- and Ka-bands [5], [6].

To achieve frequency tunable resonant mode VCOs, the traditional method is to use either a switched-capacitor array or a varactor, or a combination of both techniques [7]. Capacitor banks and varactors are commonly used for frequency tuning by changing their capacitance, which, in turn, alters the oscillation frequency. In the mm-wave 5G frequency range, using capacitors only to achieve wide tuning range becomes a challenging task. To achieve a wide tuning range, the sizes of the capacitor bank and their associated switches become large. As larger capacitors with switches are used, they tend to show a reduced quality factor (Q), as the frequency goes higher than 20 GHz. Moreover, at mm-wave frequencies, parasitic elements in varactors and capacitor banks lead to losses, reducing the achievable quality factor (Q) and limiting the overall tuning range. Other methods have been suggested to achieve high tunability, such as inductor tuning by varying magnetic flux [8], [9], [10] and switched inductors [11]. The previous studies employed series switches to adjust the inductance of the resonator tank using conventional capacitive tuning. However, these oscillators have lower Q of the inductors due to the series switches.

Recently, several authors have presented a dual-path inductor, which presents discretely tunable inductances without using any switch in the signal path. Based on this concept, digitally controlled oscillator [6], quadrature VCO [12], quad-core VCO [13], [14], and quad-mode transformer-based [15] VCO have been demonstrated. In [13], the inductance values in the two modes are similar, as the authors did not intend to achieve multiband operation. In [6] and [12], the ratio of inductor values in the two modes is limited to 1.8:1 and 1.6:1, respectively, because of the geometry of the inductor. In [15], a mode-switching transformer is introduced, which has four modes of operation. Although this VCO presents an octave frequency tuning range, the inductance in the high band

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suffers from Q degradation due to the magnetic coupling of the transformer.

In [1], a novel inductor is introduced that offers the inductance value changing ratio to 4:1, enabling multiband oscillation in a one-octave frequency range. Since there is no switch in series with the inductor, high inductor Q is ensured across the one-octave frequency range. Furthermore, with the inclusion of a mode-switching capacitor [16], triple-band oscillation is achieved at 19, 28, and 36 GHz. In this work, we achieved multiband oscillation spanning an octave range by introducing a novel dual-path inductor and mode-switching capacitor, instead of using large switched-capacitor banks, which degrade quality factor. Since the capacitors in the cap bank are smaller (to cover smaller frequency bands instead of very wide tuning range), they are designed with smaller capacitors, which does not degrade the overall Q as much large capacitor in the bank, thus improving the dc-to-RF efficiency. In addition, a class-B VCO is implemented in a 180-nm BiCMOS process using the dual-path inductor. The performance of the two VCOs demonstrates that the proposed inductor can generate oscillation across three bands, regardless of the active core topology. Each frequency band covers about 3-GHz tuning range to cover the mm-wave 5G bands. The VCOs attain good phase noise and low-power consumption in all three bands due to the high-quality factor of the inductor and the use of a smaller capacitor bank and varactor. To summarize the contributions of this work, this article provides the following:

1) mathematical analysis and a compact model of the dual-path inductor highlighting the advantages of this structure;
2) the design considerations for the mode selecting switches and their impact on the stability of oscillation;
3) detailed experimental results and characterization of the triple-band VCO;
4) implementation in two different technologies highlighting the design considerations and showing the utility of the inductor structure, regardless of the process technology.

This article is organized as follows. Section II provides a brief theoretical background of mode-switching VCOs, followed by a detailed analysis of the proposed inductor. Section III presents the detailed design procedure of the class-D VCO, and Section IV describes the design of the class-B VCO. Section V describes the details of the measurement results, along with a comparison with recent mode-switching VCOs in CMOS technologies. Section VI concludes this article.

II. Multicore VCO Analysis

Fig. 1 shows the conceptual diagram of the dual-path inductor along with the mode-switching capacitor. The working principle of the inductor will be described later. The transconductance network and the LC resonator constitute the two parts of the proposed oscillator, which form a feedback loop. We will study the basic working principle of the oscillator in this section.

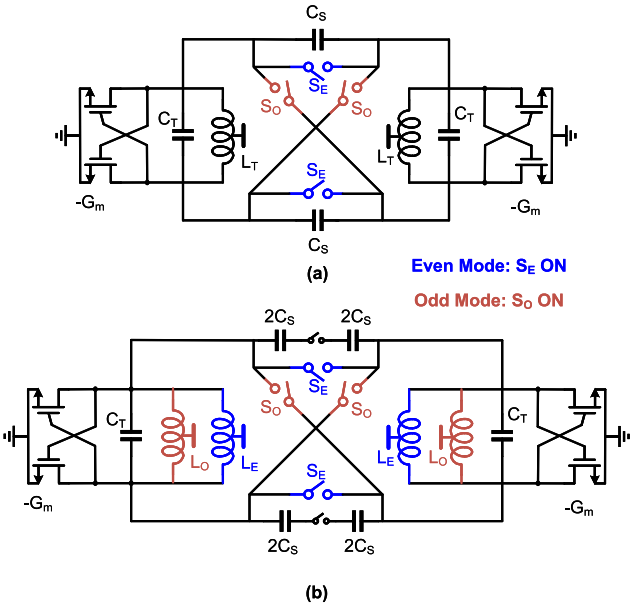


Fig. 1. Conceptual diagram of the dual-core multiband VCO. (a) Conventional design with separate inductors and phase-switched capacitor. (b) Proposed triple-band VCO with dual-mode inductors and tunable phase-switched capacitor.

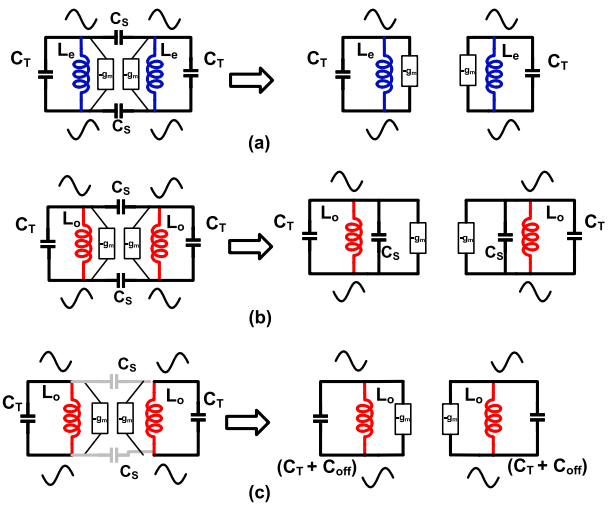


Fig. 2. Conceptual diagram of the VCO. (a) Operation in even-mode inductance, where C_S has no effect on the tank. (b) Odd-mode inductance with the C_S ON. (c) Odd-mode inductance with C_S OFF in parallel with parasitic capacitance C_{off} from the switch.

A. Mode of Operations

We have used our custom dual-path inductor and cross-coupled differential transistor pairs as an active core; as shown in Fig. 1, the oscillator always works with differential excitation. The sign of the voltages at each inductor's two terminals is opposite. Hence, we are only considering the differential modes of the resonator. Its analysis reveals that it has an odd mode and an even mode for resonance. Here, we try to describe the operation of the two modes intuitively.

1) First, we consider the even mode, where the two LC tanks are excited with in-phase signals. As illustrated in Fig. 2, the capacitors C_S do not see any voltage difference across its terminals, hence carrying no current. Thus, the resonator can be reduced to two LC tanks,

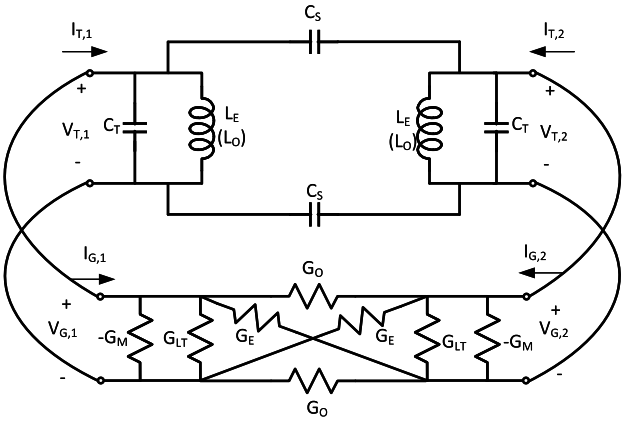


Fig. 3. Dual-mode (even and odd) LC oscillator physical model as two-port network shown as an LC resonator in parallel with transconductance network.

consisting of a tank capacitor C_T and an equivalent tank inductor in this more L_e. Thus, we determine the lowest resonant frequency as follows:

$$\omega_l = \frac{1}{2\pi\sqrt{L_e C_T}}. \tag{1}$$

2) The two LC tanks are in opposite phase when excited in the odd mode. As shown in Fig. 2, the capacitors C_S experience out-of-phase voltage across its terminals. Therefore, the equivalent circuit on the right-hand side of Fig. 2 is obtained, which consists of two LC tanks with equivalent tank inductor of L_O and capacitor (C_S+C_T). Thus, the medium resonant frequency can be expressed as follows:

$$\omega_m = \frac{1}{2\pi\sqrt{L_o(C_T + C_S)}}. \tag{2}$$

3) The third resonant frequency is achieved in odd mode when the C_S capacitor is switched off. An equivalent off-stage capacitance C_{off} is added to the tank capacitance C_T. This achieves the highest resonant frequency given by

$$\omega_m = \frac{1}{2\pi\sqrt{L_o(C_T + C_{\text{off}})}}. \tag{3}$$

The method of achieving two different inductance values is discussed in Section II-B. The resonator can be fully described by modeling it as a two-port network, as depicted in Fig. 3, and utilizing its impedance matrix (Z matrix) [17]

$$\begin{bmatrix} V_{Z,1}(S) \\ V_{Z,2}(S) \end{bmatrix} = Z(S).\begin{bmatrix} I_{Z,1}(S) \\ I_{Z,2}(S) \end{bmatrix}. \tag{4}$$

The expression of the matrix $Z(s)$ is provided later as (5), shown at the bottom of the page 6. When even mode is selected, the two resonance frequencies are at ω_l and ω_h, regardless of the mode-switching capacitor C_S. Only in the odd mode, depending on the capacitor C_S, the two resonance frequencies are ω_m and ω_h. Each matrix element's two terms display the two resonance frequencies. The input impedance of port1 (when port2 remains open) (Z_{11}) has three peaks at ω_l, ω_m, and ω_h. Such a resonator is designed in a 65-nm CMOS process with the inductances in the two modes being 80 and 320 pH. The tank capacitance C_T is varied around 200 fF. The band-switching capacitors C_S are 180 and 40 fF in ON and OFF modes, respectively. Fig. 4 shows the input impedance of port1, with variations in the capacitors. By tuning C_T, we can observe that the resonance frequency changes in all three bands. However, the variation of the mode-switching capacitor C_S does not impact the resonance frequency in the low band. The three bands can be chosen independently by selecting different component values of the inductance in the two modes and the mode-switching capacitor. For demonstration purposes, one-octave frequency separation is chosen between the low and high bands. In this experiment, the tuning range in the three bands is 20%, 18%, and 15%, respectively. Ideally, the mid-band could be chosen anywhere in between the two bands, but parasitic capacitance from the switch limits the tunability that could be achieved with this mode of operation. The mid-band is chosen halfway between the low and high bands for this implementation.

B. New Dual-Path Inductor

Using the top metal layer, a custom inductor is generated in a standard 65-nm CMOS process. Prior works based on phase-switched inductors [6], [12], [13] are limited by the change in the inductance value because of their physical characteristic. This work proposes a new inductor that goes beyond this limitation. A simplified layout of the inductor in two different modes is shown in Fig. 5. A pair of differential signals are fed into the four-port inductor, and the signal travels through two different paths based on the input polarity of the differential signals. When excited in the odd mode, the differential signal travels through a path with a smaller loop radius, which leads to a lower inductance value. This is illustrated in Fig. 5(b). When excited in the even mode, the signal travels through a larger loop, which results in a higher inductance value, as illustrated in Fig. 5(a). The inner and outer radii of the inductors in both modes can be chosen based on the intended applications. This adaptability makes the proposed inductor suitable for multiband applications.

To determine the inductance and Q of the inductor, the structure is simulated by the electromagnetic (EM) tool in Keysight's advanced design system (ADS). Fig. 6 illustrates the inductance and quality factor of the proposed inductor in both modes in the CMOS implementation. The BiCMOS implementation of the inductor shows similar inductance and Q from EM simulation. We observe a 4× variation in inductance change without significant quality factor degradation in the desired frequency bands. As per the authors' knowledge, this is the most considerable inductance variation achieved in a switch-mode inductor without introducing lossy series switches or magnetic coupling that degrades the quality factor in either of the modes [8].

C. Inductor Model

A simplified model of the dual-path inductor is presented previously in [6], which is shown in Fig. 7. The equivalent circuit models of the proposed inductor under

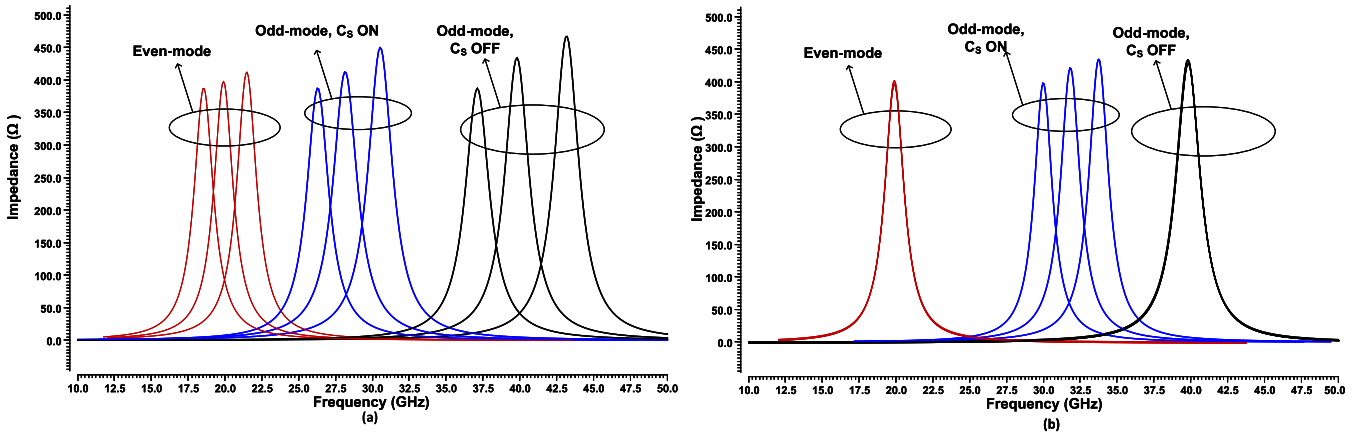


Fig. 4. Impedances looking into the input port of the resonator. (a) Tank capacitor C_T is varied to 170, 200, and 230 fF, while mode-switching capacitor C_S is turned on (180 fF) for the mid-band and off (40 fF) for the high band. (b) C_T is fixed, while C_S is varied to three different values. Note that the low-band and high-band resonance frequencies have not changed.

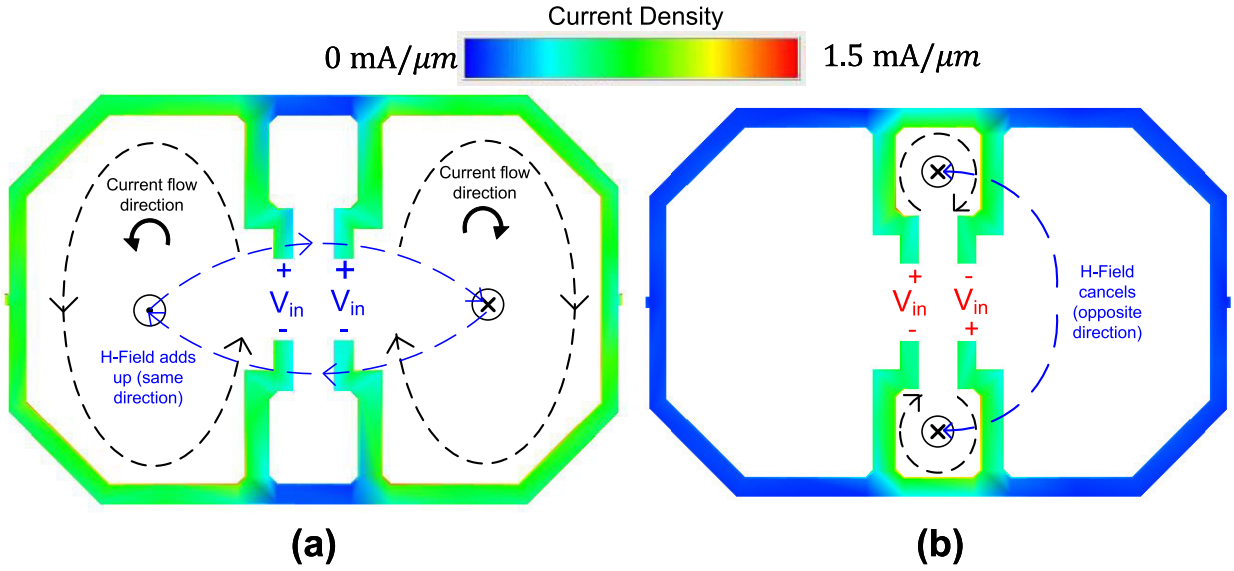


Fig. 5. Electric- and magnetic-field distributions in the two modes of the dual-path inductor. (a) Even-mode excitation. (b) Odd-mode excitation.

even- and odd-mode excitations are shown in Fig. 7(a) and (b), respectively. When the inductor is excited in odd mode, the lowest impedance signal path crosses between the two excitation signals, giving an effective odd-mode inductance of $L_{\text{eq,odd}} = 2\ .\ L_1$, where L_1 refers to the equivalent self-inductance from an input port to the point of symmetry in the odd mode. In the odd mode, there exists a horizontal symmetry, as shown in Fig. 5, which forms a virtual ac ground. The outer loops do not contribute to the inductance seen from the input port, as the current distribution in the outer loop is minimized in this mode [as shown in Fig. 5(b)].

In even-mode excitation, symmetry is maintained only between the left- and right-hand sides, shifting the primary axis of symmetry to a line separating the excitation signal's positive and negative terminals.

The corresponding signal path now extends through the outer loops. The resulting equivalent even-mode inductance is $L_{\text{eq,even}} = 2\ .\ L_1 + L_2$, where L_2 refers to the equivalent self-inductance, as shown in Fig. 5(a).

The mutual coupling varies between the two modes, achieving a larger change in inductance, as described in [6]. The equivalent flux linkage shown in Fig. 5(b) is in the opposite direction, resulting in the cancellation of mutual coupling between the inductor pairs in odd mode. Hence, the equivalent inductance considering mutual coupling does not change. However, in the even mode, the mutual flux linkage adds constructively, as shown in Fig. 5(a), resulting in increased inductance observed in the even mode.

Assuming coupling factor k_{odd} for the loops in odd mode (which is small), the resulting total inductance in odd mode can be derived as follows:

$$L_o = 2\ .\ L_1\ .\ (1 - k_{\text{odd}}) \approx 2\ .\ L_1. \tag{6}$$

Similarly, the resulting inductance in even mode can be derived as follows [6]:

$$L_e = 2.L_1.\left(1 + k_{\text{even},1}\right) + L_2 + 4.k_{\text{even},2}.\sqrt{\frac{L_1.L_2}{2}}. \tag{7}$$

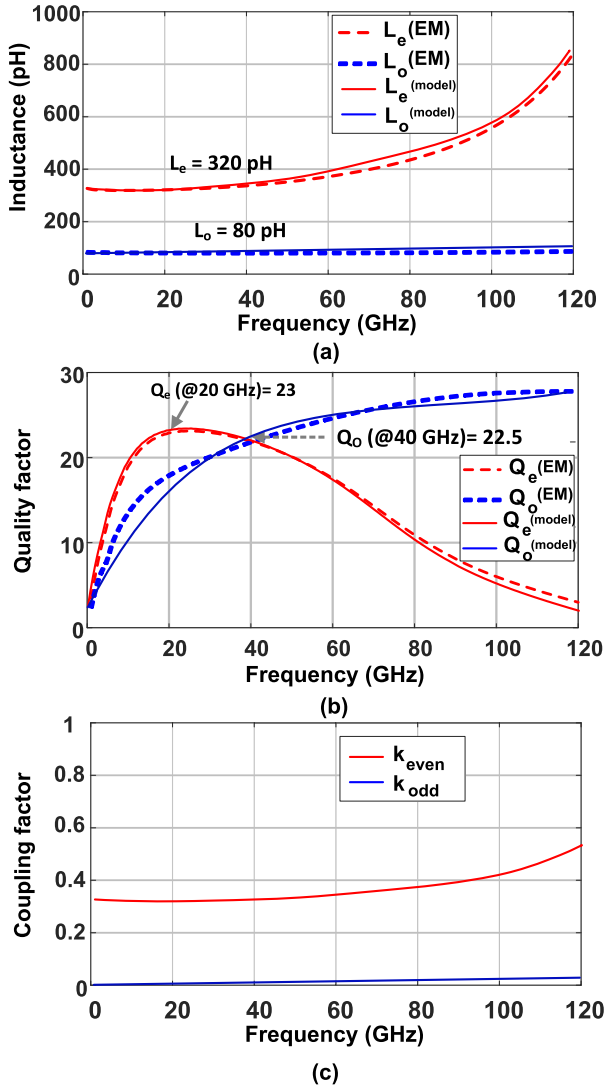


Fig. 6. (a) Inductance, (b) quality factor, and (c) coupling factor in two modes obtained from EM simulation. The dashed lines represent EM simulated results, whereas the solid lines represent results from the equivalent circuit model. The coupling factor is only determined from EM simulation.

Here, $k_{\text{even},1}$ refers to the coupling factor emerging from the mutual coupling between the L_1 segments and $k_{\text{even},2}$ refers to the coupling factor emerging from the mutual coupling between L_1 and L_2. Due to the positive k values in this mode, the total inductance is significantly increased in the even mode. The simulated k values in different modes are shown in Fig. 6(c) versus frequency.

A scalable and compact model is required for dual-path inductors for validation and design. For this purpose, a more comprehensive model is developed in this work, which is shown in Fig. 8. The model predicts equivalent inductance when either of the modes is active, since even- and odd-mode inductances are correlated. The input ports are depicted as P and N as the differential ports looking into the inductor. The capacitor C_c represents the coupling between the two ports, which is small. The inductor $L_{S,PN}$ represents parasitic inductance arising from coupling from the substrate, and the loss is modeled with the series resistor $R_{S,PN}$. The majority of the inductances from the current carrying loops are modeled

TABLE I
SUMMARY OF MODEL PARAMETERS

Model parameters	Odd-mode value(s)	Even-mode value(s)
$L_{S,PN}$	218 pH	375 pH
$R_{S,PN}$	0.93 Ω	0.85 Ω
C_C	8×10^{-5} fF	10^{-4} fF
$L_{S,PP} = L_{S,NN}$	53.53 pH	159.63 pH
$R_{S,PP} = R_{S,NN}$	0.092 Ω	0.26 Ω
$C_P = C_N$	5.3 fF	15 fF
C_X	25 fF	47 fF
$C_{XP} = C_{XN}$	10 aF	10 aF
$R_{XP} = R_{XN}$	71 $K\Omega$	80 $K\Omega$
C_{PN}	1.23 fF	3.25 fF
R_{PN}	600 $K\Omega$	1 $M\Omega$
$C_{P,sub} = C_{N,sub}$	3.8 fF	15 fF
$R_{P,sub} = R_{N,sub}$	3 $K\Omega$	1 $K\Omega$
$C_{X,sub}$	8.7 fF	22 fF
$R_{X,sub}$	1.5 $K\Omega$	700Ω
$K_{m,1} = K_{m,2}$	0.34	0.66
K_{PN}	0.01	0.01

by $L_{S,PP}$ and $L_{S,NN}$, whereas the losses are modeled by the resistors $R_{S,PP}$. In different modes, these inductors account for the contributions of L_1 and L_2 as mentioned before. The mutual coupling between the two inductors is represented by K_{PN}. The point of symmetry between the ports is denoted by the node X, and the distributed capacitances from the input ports and node X to the corresponding substrate nodes are denoted as C_P, C_N, and C_X. The substrate losses and parasitic capacitance from the associated substrate nodes are depicted by the three blue-colored RC parallel branches. The other three parallel RC branches represent the coupling capacitance and substrate losses from the corresponding substrate nodes to the ideal ac ground in the layout.

The model parameters are determined to closely match the inductor's characteristics across a broad frequency range. The simulated results from the model are plotted alongside the EM simulated results shown in Fig. 6. The model parameters are obtained from an optimizer tool in Keysight ADS to match the EM-simulated parameters. The parameter values for both modes are shown in Table I. Due to the symmetry of the layout, some of the model parameters have the same value, as shown in the table. Fig. 6 shows a good match between the equivalent circuit model and the EM simulated results, and the model accurately represents the inductor's behavior in both modes. The parameters listed in Table I give some insights about the inductor behavior in high frequency. The substrate parasitic capacitances in the even mode are higher than those in the odd mode, resulting in a much higher self-resonance frequency (SRF) in the odd mode. This is expected, since the current carrying loop in the odd mode is much smaller. Hence, the substrate-coupled parasitic capacitances are smaller.

D. Effect of the Mode-Changing Switches

The mode of the inductor is chosen by the switches shown in Fig. 1. The switches S_E and S_O ensure even- and odd-mode operations, respectively. The foregoing analysis of the inductance assumes ideal switches with zero impedance when turned on and infinite impedance when turned off. In reality, these switches are implemented by MOS transistors, which

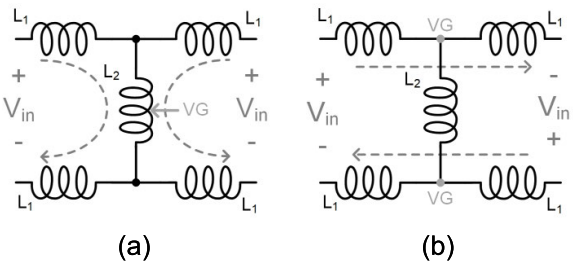


Fig. 7. Simplified equivalent circuit model of the dual-path inductor under (a) even- and (b) odd-mode excitations. Altering the relative phase of the input signals modifies the signal path and VG locations, thereby changing the effective inductance [6].

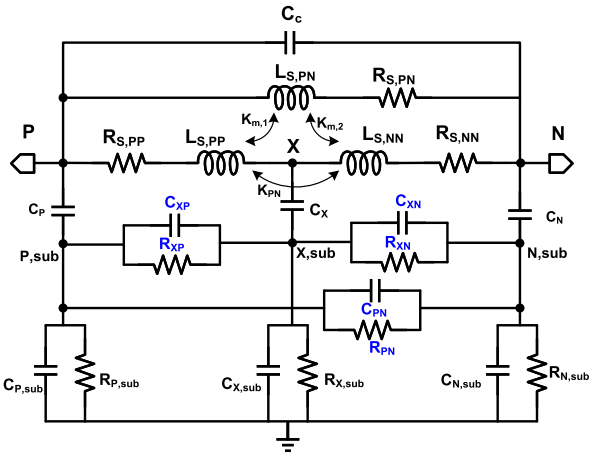


Fig. 8. More complete model of the dual-path inductor showing parasitic capacitance and resistance with coupling factors.

pose finite impedances. Hence, some deviation from the ideal behavior is expected. Because of the finite impedance of the switches, the loaded quality factor is reduced, resulting in degraded phase noise. Moreover, the MOS switch implementation comes with parasitic capacitance, which affects the achievable tuning range. Because of these detrimental effects, the switch should be chosen carefully.

The resonator tank consists of a parallel combination of inductor and capacitor. The mode-switching transistors appear as another parallel resistor to the tank. The resonator quality factor (Q) of this parallel RLC circuit is given by

$$Q = R_{\text{tank}}\sqrt{\frac{C_{\text{tank}}}{L_{\text{tank}}}} = \frac{R}{\omega_o L_{\text{tank}}} = \omega_o R_{\text{tank}} C_{\text{tank}}. \tag{8}$$

Here, R_{tank} is the parallel combination of tank equivalent resistance emerging from the loss of inductor and capacitor, and the switch turn-on resistance (i.e., $R_{\text{tank}} = R_P||R_{\text{on}}$). To maximize the quality factor, the turn-on resistance of the switch should be made as large as possible, so that its

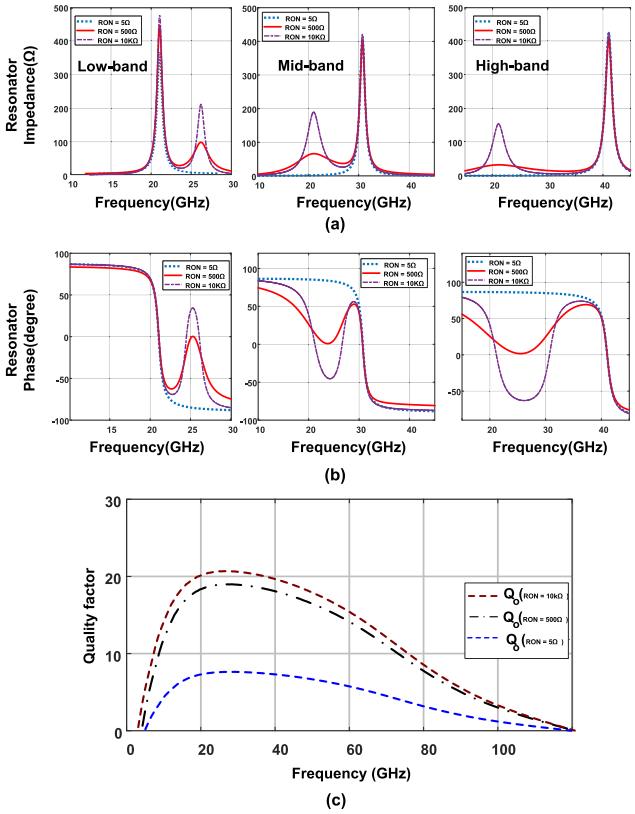


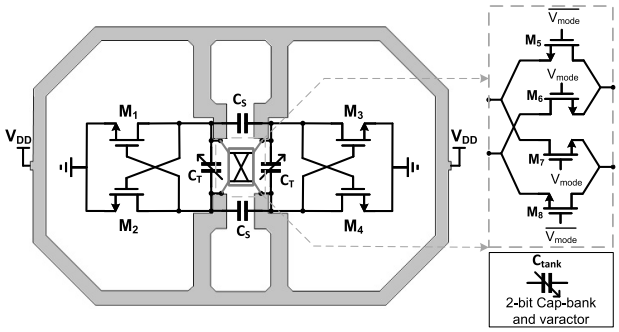
Fig. 9. Simulation results for different turn-on resistances of the switches. (a) Resonator impedances. (b) Resonator phases. (c) Resonator Q in odd mode.

effect is negligible compared with R_P. In reality, there is a problem in increasing R_{on} beyond a certain value, which is empirically determined [13]. If an arbitrarily large value for R_{on} is chosen, stability issues arise, as shown in Fig. 9. Notably, very low R_{on} reduces the tank impedance, as it impacts the equivalent parallel tank impedance. If R_{on} is increased too high, we observe multiple zero crossings in the phase plot, which means oscillation could occur at undesired frequencies. The switch turn-on resistance is kept at 500 Ω to reduce this mode ambiguity.

III. Class-D Triple-Band CMOS VCO

A triple-band VCO is fabricated in a standard 65-nm CMOS process utilizing the proposed dual-path inductor and tunable mode-switching capacitors. Fig. 10 shows the schematic and device sizes of the VCO. A class-D biasing for the oscillator cores is chosen for its low-phase noise, low-supply voltage, and high efficiency, with relatively simple architecture [18]. Class-D operation maximizes the oscillation amplitude, which

$$Z(S) = \begin{cases} \frac{1}{2}\left[\frac{\frac{s}{C_T(s^2+\omega_l^2)} + \frac{s}{C_T(s^2+\omega_h^2)}}{\frac{s}{C_T(s^2+\omega_l^2)} - \frac{s}{C_T(s^2+\omega_h^2)}} \quad \frac{\frac{s}{C_T(s^2+\omega_l^2)} - \frac{s}{C_T(s^2+\omega_h^2)}}{\frac{s}{C_T(s^2+\omega_l^2)} + \frac{s}{C_T(s^2+\omega_h^2)}}\right]; & \text{when } C_S \text{ is switched off} \\ \frac{1}{2}\left[\frac{\frac{s}{C_T(s^2+\omega_h^2)} + \frac{s}{(C_T+C_S)(s^2+\omega_m^2)}}{\frac{s}{C_T(s^2+\omega_h^2)} - \frac{s}{(C_T+C_S)(s^2+\omega_m^2)}} \quad \frac{\frac{s}{C_T(s^2+\omega_h^2)} - \frac{s}{(C_T+C_S)(s^2+\omega_m^2)}}{\frac{s}{C_T(s^2+\omega_l^2)} + \frac{s}{(C_T+C_S)(s^2+\omega_m^2)}}\right]; & \text{when } C_S \text{ is switched on} \end{cases} \tag{5}$$



Component	Purpose	Value
M_{1-4}	Core transistors	56µm/60nm
M_{5-8}	Mode-switching transistors	16µm/60nm
$C_{varactor}$	Accumulation mode varactor	20fF/40fF
C_{b0}/C_{b1}	Capacitor bank	30fF/60fF
C_{band}	Tunable mode switching Capacitor	150fF

Fig. 10. Schematic of the triple-band class-D VCO. The key component values are listed in the table.

has a direct impact on reducing phase noise [19], [20]

$$\mathcal{L}(\Delta\omega) = \frac{4FkTR}{V_o^2}\left(\frac{\omega_o}{2Q\Delta\omega}\right)^2. \quad (9)$$

Here, $\mathcal{L}(\Delta\omega)$ is the phase noise at $\Delta\omega$ offset from frequency ω_o, F is the noise factor of the oscillator, k is Boltzmann's constant, T is the absolute temperature, Q is the loaded quality factor, and V_o is the amplitude of oscillation. According to (9), maximizing the output swing and oscillator-loaded quality factor is necessary to reduce phase noise.

The oscillator cores consist of four nMOS switches (M1–4). The proposed dual-path inductor is used for coarse frequency band switching. Four additional switches (M5–8) control the input polarity of the differential signal that enters the dual-path inductor to select even and odd modes. The inputs to these switches, (V_{mode} and $\overline{V_{\text{mode}}}$), are used to switch between the even and odd modes. The tunable mode-switching capacitor splits the higher frequency band into two bands. Alternatively, the lower frequency band could be split by placing C_S across the inductor terminals. However, this makes the layout more complicated. This is why C_S is placed parallel to the inductor terminals in the odd mode to split the higher frequency band into two, allowing the proposed VCO to operate in three bands. For in-band frequency tuning, a combination of a 2-bit binary-weighted capacitor bank ($C_{b,0-1}$) and a small accumulation mode varactor (C_{varactor}) is used. These form the tank capacitance C_T. In order to minimize the supply voltage and lower power consumption, low-threshold devices are utilized in the VCO's active core. Due to their superior quality factor over metal–insulator–metal (MIM) capacitors, metal–oxide–metal (MOM) capacitors have been employed for switching capacitors.

The VCO settles quickly during mode changing. A simulated transient behavior of the VCO during mode switching is shown in Fig. 11. The transition time for changing from low band to high band and from high band to low band is 650 pS.

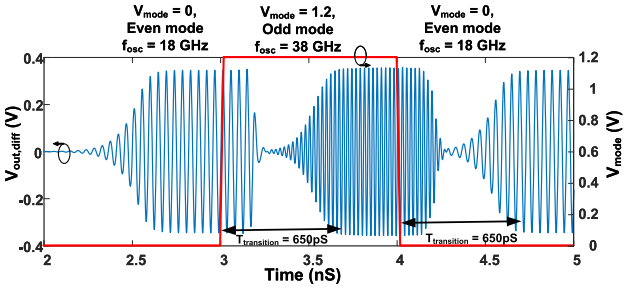
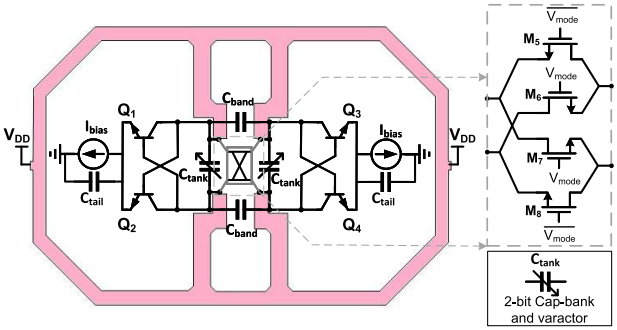


Fig. 11. Transient simulation results of the VCO during mode switching.



Component	Purpose	Value
Q_{1-4}	Core transistors	40µm/55nm
M_{5-8}	Mode-switching transistors	48µm/180nm
$C_{varactor}$	Accumulation mode varactor	25fF/50fF
C_{b0}/C_{b1}	Capacitor bank	30fF/60fF
C_{band}	Tunable mode switching Capacitor	140fF

Fig. 12. Schematic of the triple-band class-B VCO.

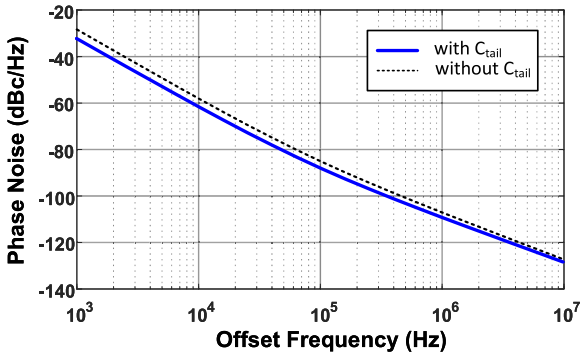


Fig. 13. Simulated phase noise for the low band (19 GHz) showing the variation when the tail capacitor is included and excluded.

The VCO has a quick transition time, making it well suited for frequency hopping applications [21].

IV. Class-B Triple-Band BiCMOS VCO

The modified version of the VCO is fabricated using the TowerJazz 180-nm BiCMOS process. This VCO has a similar inductor structure and switching mechanism as the previous CMOS VCO. However, the oscillator core is biased in class-B, with a tail current source. The schematic of the class-B VCO is shown in Fig. 12. Class-B VCOs are known for their superior robustness with respect to supply variation [22], [23], [24]. By fabricating class-B VCO, we want to demonstrate the feasibility of the proposed inductor and mode-switching

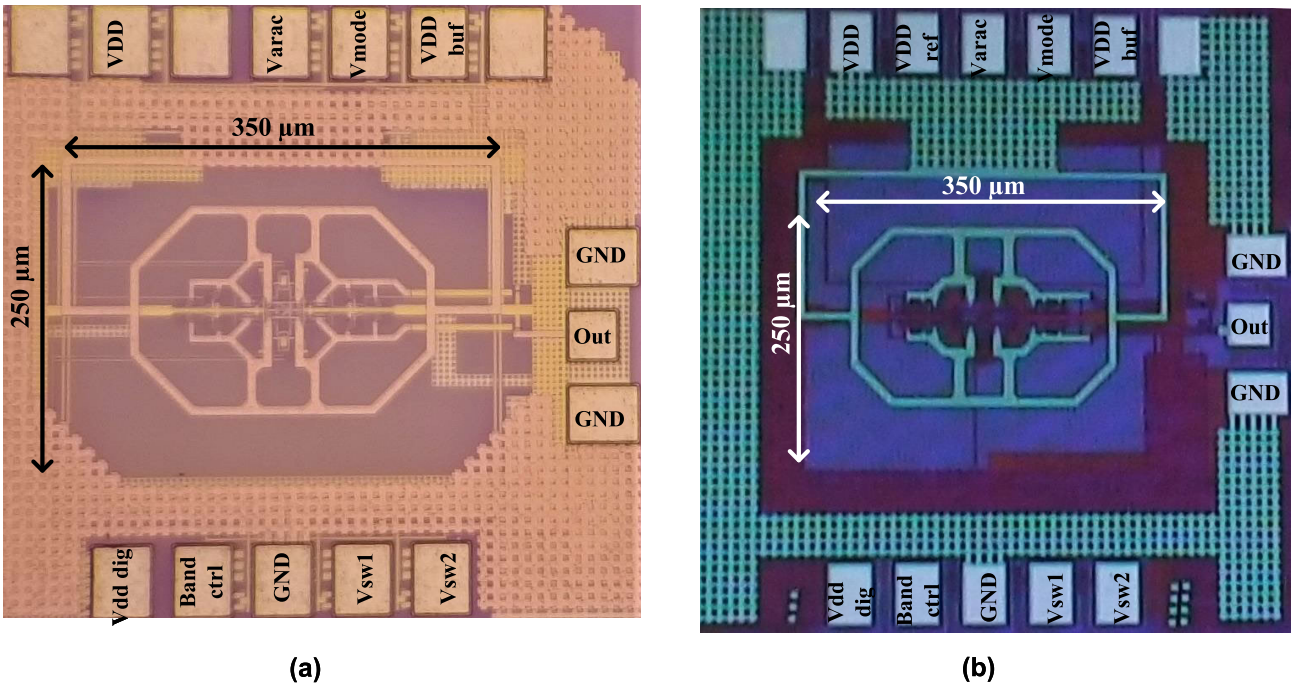


Fig. 14. Chip photographs of the fabricated VCOs in (a) 65-nm CMOS technology and (b) 180-nm BiCMOS technology. The oscillator occupies 350 × 250 μm area in both processes.

operation across both classes. The negative gm cores are formed by cross-coupled heterojunction bipolar transistors (HBTs), as shown in Fig. 12. The tail current source and switching devices are implemented by CMOS devices. The tail current source is particularly notorious for injecting both thermal noise and flicker noise, which affects the phase noise [25].

In class-B oscillators, there is a tail current source, which causes flicker noise upconversion, degrading the overall phase noise. A common technique to reduce this flicker noise is to use an inductor that resonates with the capacitance at the common node at twice the oscillation frequency [26]. However, this technique may not be suitable for multiband oscillators, as the $2f_o$ frequency moves with the change in oscillation frequency (f_o being the fundamental oscillation frequency). Instead, a large capacitor at the common node helps reduce phase noise as follows: 1) the capacitor provides an alternative path for the tail current and 2) it reduces the duty cycle of the drain current, which helps reduce the drain current noise [22]. For these reasons, a tail current capacitor C_{tail} is added at the common node of both oscillator cores. The value of the capacitor is 2 pF. A simulated phase noise plot with and without the tail current source is shown in Fig. 13. Note that the capacitor is placed under the inductor structure, so there is no additional area penalty.

V. Experimental Results

The proposed VCOs are fabricated in a 65-nm CMOS process with a nominal voltage of 1.2 V and a 180-nm BiCMOS process with a nominal voltage of 1.8 V. A micrograph of the fabricated chips is shown in Fig. 14. All active components of the oscillator were placed inside the inductor resulting in a compact active area of 0.088 mm^2 (250 × 350 μm).

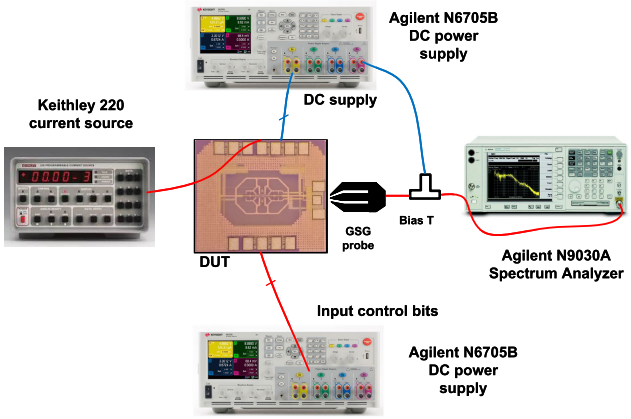


Fig. 15. Measurement test bench with power supplies and a spectrum analyzer to measure output power and phase noise of the triple-band VCOs.

The VCO's output is fed to an open drain buffer, which is terminated by a Keysight PXA N9030A signal analyzer. For balancing the load, the other output is terminated with an on-chip 50-Ω load. Fig. 15 shows the test setup used to characterize the implemented VCOs.

The class-D VCO consumes 6–7 mA in the lowest frequency band and 10–12 mA in both the middle and highest frequency bands from a 0.4-V supply. It provides an average output power of −3 dBm to a 50-Ω load over the tuning range, translating to an RF-to-dc efficiency of 3%–4%. Because of the low-loss high-quality factor dual-path inductor and smaller capacitor bank, the oscillator core can be utilized by only 0.4-V supply in class-D mode. Thus, we can achieve high dc-to-RF efficiency while covering widely separated frequency bands. Because of the tail current source and larger drop across the base–emitter junction, the class-B VCO operates

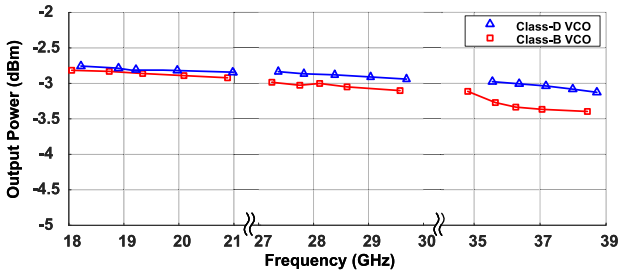


Fig. 16. Output power obtained from the VCO. The presented values are obtained after de-embedding the power loss from the buffer.

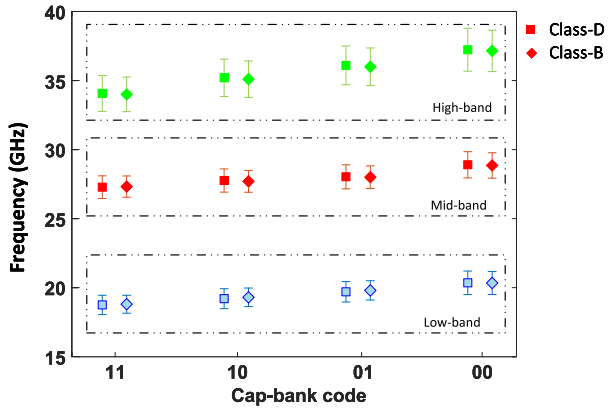


Fig. 17. Frequency tuning range in three bands of operation for both VCOs. The X-axis shows the capacitor bank code in the 2-bit capacitor array.

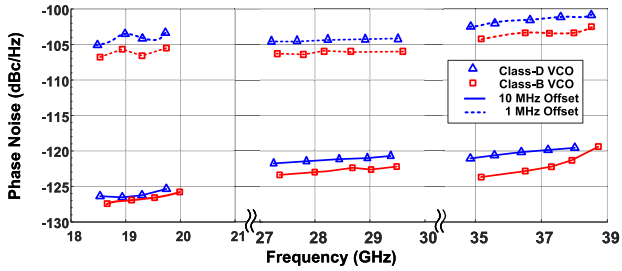


Fig. 18. Measured phase noise at 1- and 10-MHz offset frequencies for class-B and class-D VCOs.

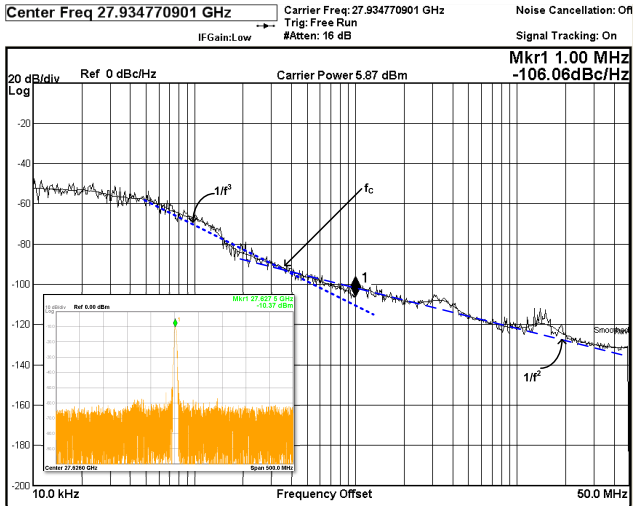


Fig. 19. Measured phase noise spectra in the middle band for the class-B VCO. The picture in the inset shows a spectrum view of the oscillation with a carrier power of −10.37 dBm (including cable loss).

with a 1-V supply. The class-B implementation is less efficient, as it consumes more power than the class-D VCO. The output power at different frequencies is shown in Fig. 16.

Fig. 17 shows the frequency tuning range for both VCOs in three bands. The frequency tuning is achieved by the mode-selecting switches described before. A 2-bit capacitor array is chosen to tune the frequency within a band. A small accumulation mode varactor is employed to achieve continuous tuning alongside the cap array. Although the varactor has lower Q in the K- and Ka-bands (ranging from 10 to 15), since there are other fixed capacitances present in the tank, the overall Q is not severely degraded [27]. This scheme is applied to both VCOs, and they show similar tuning behavior, as shown in Fig. 17. The mode-switching capacitor C_{band} is turned on/off by a voltage $\text{Band}_{\text{ctrl}}$. The lowest frequency band has a tuning range of 18.5–20.8 GHz. To operate the VCO in the middle frequency band, both V_{mode} and $\text{Band}_{\text{ctrl}}$ inputs are on, keeping the inductor in odd mode. In this case, the tuning range is 27.1–29.5 GHz. As $\text{Band}_{\text{ctrl}}$ is set to off and V_{mode} is set to on, oscillation in the highest band is accomplished. The tuning range in the scenario is 33.7–38.2 GHz. In each of the three bands, the fractional tuning ratio (FTR) is 12.15%, 9%, and 12.5%, correspondingly.

Fig. 18 illustrates the phase noise at 1- and 10-MHz offset frequencies across the tuning range for both VCOs. At 10-MHz offset, the phase noise ranges from −127.5 to −120.58 dBc/Hz for the class-D VCO. We observe similar phase noise performance from the class-B VCO, which is also shown in Fig. 18. The purpose of this research work is to achieve wide multiband frequency tunability in mm-wave VCOs. The results show promising phase noise performance even though no existing phase noise reduction techniques have been employed. The phase noise spectrum obtained from the signal analyzer at the mid-band of the class-B VCO is shown in Fig. 19, whereas the phase noise of the class-D VCO in all three bands is shown in Fig. 20. Note that the measurement was taken in open-loop configuration using the signal analyzer. Hence, the phase noise at offset frequencies under 100 kHz may compromise accuracy. From our understanding of the available equipment, phase noise at offset frequencies beyond 100 kHz is fairly accurate. From these assumptions, the noise corner frequency is near 200–300 kHz for the class-B VCO and 500–700 kHz for the class-D VCO.

A comparison with a number of recent multiband and wideband VCOs in the K- and Ka-bands is shown in Table II. Our proposed VCOs, both Class-D and Class-B, demonstrate performance that is either comparable to or surpasses previous multiband VCOs operating in similar frequency bands. Note that some of the wideband VCOs (such as [14] and [28]) reach an octave frequency tuning range with the expense of higher power consumption or degraded dc-to-RF efficiencies despite using more advanced technologies. Our proposed approach demonstrates good phase noise with a relatively simple oscillator core without using any phase noise reduction technique.

TABLE II
PERFORMANCE COMPARISON OF STATE-OF-THE-ART VCOS IN THE K- AND Ka-BANDS

References	**This work**		[6] TMTT'19	[12] ISSCC'19	[29] TCAS-II'18	[11] MWCL'14	[30] TMTT'23	[28] JSSC'21	[14] ISSCC'20	[13] JSSC'18
Technology	**65 nm CMOS**	**180 nm BiCMOS**	65 nm CMOS	65 nm CMOS	180 nm CMOS	65 nm CMOS	28 nm CMOS	22 nm FDSOI	40 nm CMOS	65 nm CMOS
Mode of operation	**Class-D**	**Class-B**	Class-D DCO	Class-D QVCO	CMOS Class-D	Class-B	Class-D	Folded Class-D	Class-B	Class-D
Freq. (GHz)	**19/ 28/ 36**	**18.5/ 27/ 35**	16.7/23.7	25/38	16.1/17	21.5-33.4	18.5/ 24/ 35	8-17	18.6-40.1	42.9-50.6
Type	**Triple-band**		Dual-band	Dual-band	Dual-band	Single band	Triple-band	Three bands merged	Quad-band merged	Single band
VCO supply	**0.4/ 0.5/ 0.5**	**0.9/ 1/ 1.1**	0.45	0.65	1.8	1.2	1.2	0.45	1.1	0.9
PDC (mW)	**2.4/4.7**	**10.1/13.1**	4.8/5.6	17.5/21.6	5.4/7.2	4.8/7.2	11.6/15/11.6	17-33	9-15	17.5-21.6
DC-RF effi. (%)	**5.3/ 4.7/ 3.8**	**3.1/ 2.8/ 2.1**	N/A	N/A	1.85*/ 1.39*	5.2*/ 0.82*	0.57*/0.6*	N/A	0.45*/0.05*	N/A
FTR (%)	**12.1/ 9/12.5**	**13/ 10/12**	23.3/ 24.4	41.2	7.5/4.7	43.3	17.5/ 16.5/ 17.9	72	73.2	16.5
PN 10MHz (dBc/Hz)	**-127.5/ -122.5/ -120.6**	**-129.5/ -125.1/ -124.5**	-130.4/ -122.5	-126/ -119	-127/ -125	-117/ -109	-127.5/ -125/ -122	-143.1/ -135*	-122.7/ -130.3	-122*/ -121*
FoM (dBc/Hz)	**187.5/ 184.5/ 186.1**	**185.6/ 184.3/ 184.9**	187.6/ 184.3	187/ 181	185/ 182	179.63/ 170.1#	184.1/ 184/ 182.8	191.65/ 180.65	183/ 186.3	180.5/ 182
FoMT (dBc/Hz)	**194.8**	**193.7**	195.1	190.8	182	191.9/ 182.1	189/ 188.3/ 187.8	208.8/ 197.8	200.3	184.9/ 186.4
Area (mm2)	**0.088**	**0.09**	0.046	0.08	0.064	0.084	0.043	0.39	0.08	0.04

$FoM = |PN| + 20log_{10}(f_o/\Delta f) - 10log_{10}P_{DC}(mW)$, $FoM_T = FoM + 20log_{10}(FTR[\%]/10)$ *Estimated from plots, #Estimated from FoM_T

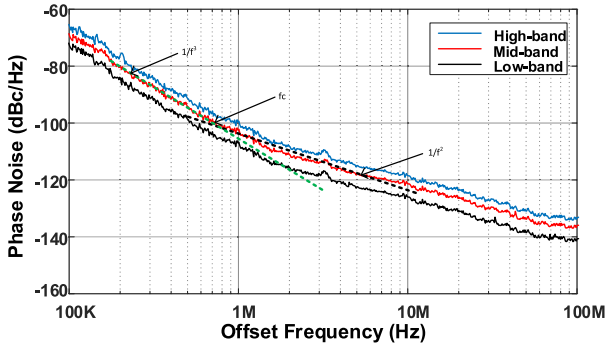


Fig. 20. Measured phase noise spectra for the three bands for the class-D VCO. The flicker noise corner frequency is shown for the mid-band.

VI. CONCLUSION

This article introduces a compact, low-loss dual-path inductor integrated into the resonator of two triple-band, low-phase noise, low-power K/Ka VCOs with an octave frequency tuning range. The innovative dual-path inductor structure changes the inductance value by a factor of 4, maintaining a high-quality factor in both operation modes. The oscillation frequencies can be tailored to meet multiband operations with wide frequency separation, such as 5G or SATCOM. In class-D mode, the triple-band VCO consumes only 2.4–4.7 mW of dc power, and in class-C mode, its consumption ranges from 10.1 to 13.1 mW, demonstrating excellent dc-to-RF efficiency. The observed phase noise is comparable with the state-of-the-art multiband VCOs in the K- and Ka-bands. The fact that the inductor structure works with two different VCO implementations demonstrates that it is appropriate for almost all LC differential VCO topologies. Employing more advanced technology can further enhance this VCO structure's phase noise and FoM.

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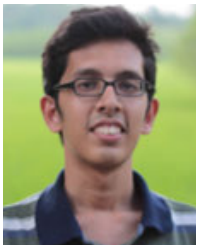

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