A Dual-Path Transformer-Based Multiband Power Amplifier for mm-Wave 5G Applications

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***Abstract*— This article presents a dual-band power amplifier for 28 and 39 GHz frequency bands based on a new dual-path transformer (DPT). This DPT can provide two optimum inductive values at two different frequency bands to optimally design the matching networks for each band without using any switch circuitries. It operates as the output and input matching networks in a parallel power combiner and divider, respectively. DPT-based PA breaks the trade-off between bandwidth and performance in conventional wideband PAs by separating one whole wideband into two narrow bands providing optimum input and output matchings for each band. The DPT-based PA has two input and two output ports. One set of input and output ports is dedicated to a lower frequency band and the other set of input and outport ports can be used for a higher frequency band. Each output port can drive a separate antenna in a phased array for each frequency band. The proposed PA prototype is fabricated in a 65 nm CMOS process achieving 15.3 and 14.0 dBm of saturated output power in 28 and 39 GHz. The peak efficiency of the PA is 34.1% and 30.2% at 28 and 39 GHz frequency bands. The PA has a measured EVM with 64-QAM modulated signal in both frequency bands showing −25.03 and −25.10 dB in the low and higher frequency bands, respectively.**

***Index Terms*— 5G mobile communication, bandwidth, impedance, inductors, linearity, MIMO, modulation, power amplifiers, power combiners, radio frequency, transformers.**

I. Introduction

THE rising demand for and availability of higher-capacity cellular networks have created the need for further advancements in wireless communications. Globally, the changeover to mm-wave 5G networks is rapidly occurring, and mm-wave 5G plays a pivotal role in this changeover. The frequency range of mm-wave 5G communication consists of multiple frequency bands which are N257-261 (FR2). Fig. 1 shows the allocation of those frequency bands with respect to other bands in FR2. As shown in this figure, N257, N258, and N261 are spread between 24.25 and 29.5 GHz (lower bands of FR2), and N260 and N258 are assigned between 37 and 40 GHz (higher bands of FR2). Each cellular carrier may use one or two of these bands. For example, some carriers in the US only support 28 GHz and others provide their services on both lower and higher frequency bands. Thus, user equipment (UE) such as cell phones must support both frequency bands to allow users to conveniently choose their services. However, it is pretty challenging to implement the transceivers covering such wide frequency ranges, e.g., from 27.5 (lower end of N261) to 40 GHz (higher end of N260). In this wideband operation case, the overall bandwidth is 12.5 GHz, where the aggregated bandwidth of N260 and N261 is 3.85 GHz. Thus, the unused 8.65 GHz band needs to be covered unnecessarily. In this case, radio frequency integrated circuit (RFIC) and antenna designers have to trade off the performance of their designs with the wideband operation. The other approach is to design two sets of transceivers and antennas for each frequency band, which occupies double chip areas and increases the whole transceiver's footprint.

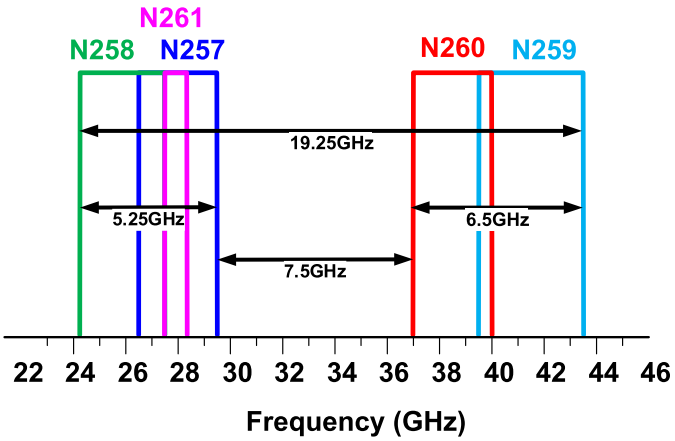

Fig. 1. 5G mm-wave frequency bands (FR2).

In addition, due to high path loss at mm-wave frequencies, phased-array architectures are commonly used [1], [2], [3], [4], [5], [6], [7], [8]. In general, the UEs include 4–16 elements in each array [9], leading to a 12–24 dB increase in EIRP compared to the single transceiver with an antenna. A slight improvement in a transceiver's power consumption, area, and output power could be multiplied by the number of elements in the array. This improvement is more significant in the arrays used for the base station, where the array's number of elements is higher than UEs. Fig. 2(a) shows a conceptual design where a wideband PA in a wideband transceiver employs a wideband matching circuit and antenna. A wideband antenna also has a trade-off between bandwidth and performance. The advantage of the wideband design is that it may need one set of TX–RX to cover the required bands at the expense of more

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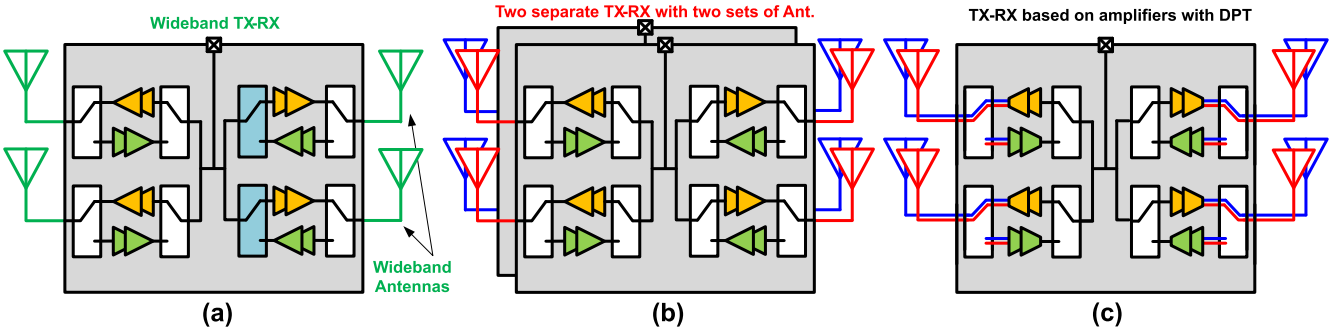

Fig. 2. Conceptual design of mm-wave phased array chips (a) wideband array and antennas, (b) multiple narrow-band array and antennas, and (c) dual-band TX–RX based on DPT structure.

passive losses at different stages. Fig. 2(b) shows two separate transceivers with two sets of antenna ports tuned at different frequency bands, such as lower bands (N257-8, N261) and higher bands of mm-wave 5G (N259, N260). The problem of lower performance in wideband design can be solved at the expense larger footprint for the entire TX–RX.

Fig. 2(c) shows a TX–RX transceiver that uses dual or multiband instead of wideband circuit blocks, and each band has a separate set of antennas. For example, the higher band is shown in red, and the lower band is in blue. The benefit of such a design is that only one TX–RX chip is needed similar to the case with wideband antennas and circuit blocks. However, it can have higher performance similar to the case with two separate TX–RX chips. In this design, the key elements are the passive circuits that provide dual or multiband operation.

Various multiband circuit topologies introduce passive circuits with multiresonances [10] or high-order matching networks [11]. These approaches are attractive in technologies with very low-loss passives, where the transmission lines are low-loss [12] or integrated CMOS processes with multiple ultra-thick metal layers are available. However, while considering bulk CMOS technologies with a low-quality factor of integrated passives, wideband passive circuits do not provide optimal performance. In [13], a dual-band PA supporting lower and higher frequency bands of mm-wave 5G, based on switched inductors in a 28 nm CMOS process is proposed. The design of switches at the output matching circuits of mm-wave PAs with reliable operation is challenging since those switches have to operate safely under high currents. Recently, based on coupled inductors, multiband mm-wave voltage-controlled oscillators are introduced [14]. The dual-path inductor (DPI) and four-port coupled inductor [15] occupy less area than multiple separate inductors providing higher performance compared to their wideband counterparts [14], [15], [16]. For example, dual-band [14], [15] and triple-band [16] oscillators are designed using DPIs. DPI consists of two inductors coupled together and provides two sets of inductive values based on the relative phases of excitation signals. The inductance with a higher value is used for the lower frequency band and the lower one for the higher band. In this way, optimal inductances for bands of interest can be implemented. The concept of the DPI is reusing all, or part of the inductor trace used for one frequency band to implement an inductive value for the other frequency band achieving two specific inductor values for each band, instead of designing two separate inductor traces decreasing the quality factor of inductors for wideband performance. The benefit of this approach provides similar or close performance to multiple narrow-band designs while occupying less area.

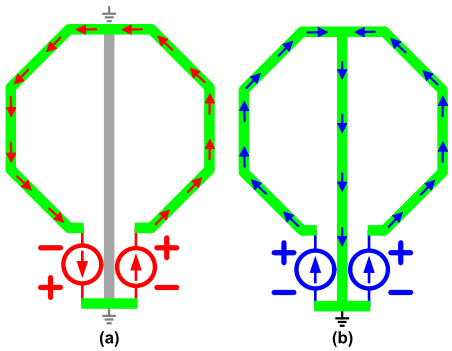

Fig. 3. (a) odd and (b) even mode excitations of a single turn differential inductor.

This article proposes a dual-band PA for mm-wave 5G transceivers that leverages a dual-path transformer (DPT). The DPT acts as a matching circuit and parallel power combiner/divider tuned at two independent frequency bands. Each frequency band is activated based on the polarity of excitation signals. This article is organized as follows, Section II presents the basic principles of the DPI and DPT. Section III describes the design of dual-band PA based on the DPT. Section IV also presents the implementation and measurement results of the dual-band DPT-based mm-wave 5G PA.

II. Developing DPT From DPI

DPI which is a basis for the DPT is described in the following section. Then, the concept of the DPT is introduced.

A. Dual-Path-Inductor

Fig. 3 shows a single-turn differential inductor with an extended center tap. This structure is excited in odd [Fig. 3(a)] and even modes [Fig. 3(b)]. In odd mode excitation, the current flow in the direction of arrows is shown, it does not flow into the centerline since the centerline is an ac ground while in the even mode excitation, the current passes through the centerline and returns to the sources [Fig. 3(b)]. In each mode of excitation, the sources see different inductive values. The inductive component of the even mode is larger than the odd

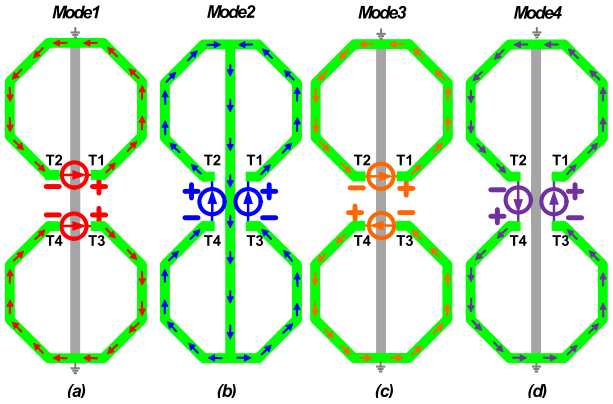

Fig. 4. DPI and four possible excitation modes. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4.

mode since the current loop is larger. Although the structures shown in Fig. 3 implement two specific inductive values in different modes of operation, they may not be used directly in multiband circuit implementation. Note that to excite the structure in even mode, current sources do not constitute a differential pair, which may not be desirable in applications where differential signaling is needed. By taking the inductor of Fig. 3, making a copy of this structure, and connecting their centerlines, it is possible to make coupled inductors, as shown in Fig. 4. The structure is called DPI [14] since based on the relative phases of exciting signals, the current path could be different resulting in two or more inductive values.

With this structure, we can implement four different combinations of exciting signals shown in Fig. 4(a)–(d). Fig. 4(a) and (b) shows the current distribution in odd and even modes described earlier in Fig. 3 which in this case current sources can be implemented with differential pairs. Excitation modes shown in Fig. 4(c) and (d) and their corresponding current distributions are new to the developed structure due to added extra inductor compared to Fig. 3. Although Fig. 4(c) and (d) has different excitation signals they both result in the same current distribution. Therefore, their inductive component is also the same. In [14], excitation modes of Fig. 4(b) and (c) are used to design a dual-band VCO, and other modes shown in Fig. 4(a) and (d) were not known. In Section II-B, it is explained that the first and second excitation modes [Fig. 4(a) and (b)] can be used to generate a transformer based on the DPI.

B. Dual-Path-Transformer

The principle of the DPI is discussed in Section II-A and it is useful for designing multiband VCOs or other low-power blocks. However, it is not possible to apply the DPI directly to a PA design. Since in each mode of operation, the terminals of DPI may have different polarities, if we take the signals at DPI's terminals and connect them, they may be constructively combined in one mode but destructively combined in the other mode.

For example, if we take mode 1 in Fig. 4(a) and connect T1, T3 together and T2, T4 together to make a differential output, it works in this mode only. If the operation is changed, let's

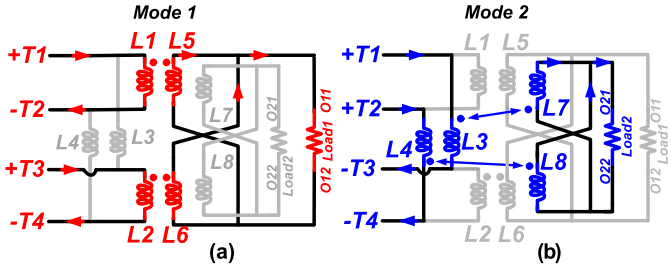

Fig. 5. Simplified schematic of DPT in (a) mode 1 and (b) mode 2.

say mode 2, T1 and T3 have opposite polarities. When they are connected, they cancel each other. In the case of VCO design, since the output power and power efficiency are not as important as in PA, one of the terminals of DPI is connected to the load and other terminals are terminated to dummy loads. Such a design for a PA leads to 6 dB power loss and dramatic degradation in power efficiency. To fix this problem, the very first solution is adding switching circuits. However, designing switches at the output of PA is challenging because of large voltage swings and high currents causing reliability issues.

Combining the currents or voltages of all DPI terminals is essential for PA design. To have a constructive signal combining in each mode of operation, we introduce a secondary coil and create a transformer that does not need switching circuitries and all signal combining happens inside the transformer. Thus, in each mode of operation, signals are combined at a specific load dedicated to the corresponding mode of operation, not leaking into the other load specified to the other mode.

A simplified schematic of the desired transformer is shown in Fig. 5. In this figure, L1–L4 model the primary inductances, and L5–L8 represent the secondary inductances. In Fig. 5(a), T1–T2 and T3–T4 constitute two differential pairs, therefore L1 and L2 are excited and L3 and L4 remain unexcited (no current can pass through them due to the same polarity of excitations). L1 has magnetic coupling with L5. Similarly, L2 has magnetic coupling with L6. The coupled currents into L5 and L6 are summed at Load 1. In the second mode shown in Fig. 5(b), T1–T3 and T2–T4 constitute two differential pairs, therefore, L3 and L4 are excited. They have magnetic coupling with L7 and L8, respectively. The coupled currents into the secondaries (L7 and L8) are combined at Load 2. In this way, we developed a transformer with two modes of operation chosen based on the relative phases of excitation signals at the primary terminals.

One important point about the structure shown in Fig. 5 is that when it is excited in mode 1 (mode 2), only the load associated with the excited mode receives power. Therefore, the impedance connected to the other load does not change the operation of mode 1 (mode 2) and vice versa. This point is explained later in this section too. Also, note that the L1–L4 model of the DPI is presented earlier section.

To explain the proposed DPT in detail, the DPI of Fig. 4(a) and (b) are redrawn in Fig. 6. It shows the primary coils and the secondary coils separately with the current distributions in modes 1 and 2 of operation, respectively. Compared to Fig. 4(a) and (b), the secondary coil (shown in

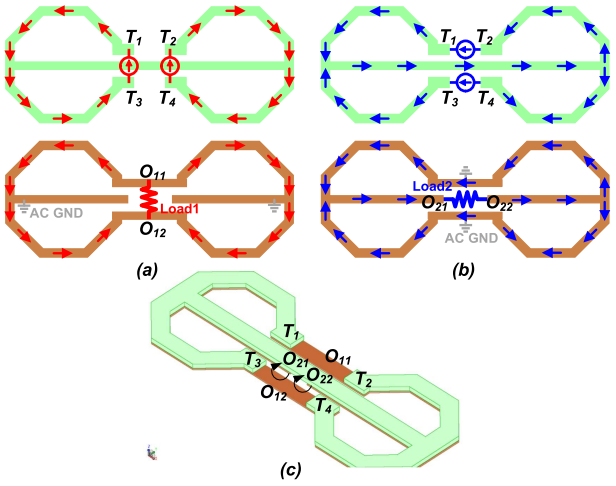

Fig. 6. Primary and secondary of DPT (a) in mode 1, (b) in mode 2 with current excitation signals and dedicated loads, and (c) 3-D view of developed DPT layout.

orange) is introduced, and two other modes [Fig. 4(c) and (d)] are set aside. This point will be discussed in the later section. The current sources are connected to primary coils and specific differential loads are linked to the output ports (O11–O12 and O21–O22). The current sources and the loads corresponding to the first and second modes are shown in red and blue, respectively.

In Fig. 6(a), two current sources inject currents into the T_1 and T_2 terminals of the primary coil. These injected currents pass the short path (not through the centerline of the primary inductor) and reach T_3 and T_4. In the other mode of operation, Fig. 6(b), the current sources are placed between T_1–T_2 and T_3–T_4. The injected currents into T_1 and T_3 flow into the centerline and then back to T_2 and T_4. By looking into the secondary coils, it is evident that the induced currents in the secondaries are combined at the specific loads in both modes of operation

When the DPT is operating in mode 1, the Load 2 (blue) connected between O_{22} and O_{21} (not shown in Fig. 6(a) for simplicity) receives no current since the O_{21} and O_{22} terminals are ac grounds. On the other hand, when the DPT is in mode 2 of operation the load connected between O11 and O12 (not shown in Fig. 6(b) for simplicity) does not receive any currents since once again the terminals of O_{11} and O_{12} are ac grounds. Note that the green (primary) and orange (secondary) coils are stacked and make a two-way parallel-connected differential transformer similar to the one shown in Fig. 6(c). Thus, the developed dual-mode two-way transformer is called DPT. This figure shows the 3-D view of DPT and all input and output terminals are shown.

To build the proposed DPT, we picked the excitation modes shown in Fig. 4(a) and (b) and set aside (c) and (d). If the DPT is excited, similar to Fig. 4(c) or (d), none of the specific loads connected to the secondaries of the DPT receive any power. In fact, the induced current at the secondary circulates in the secondary coil and does not flow into the loads. Next, an analysis of DPT based on a coupled line model is presented, providing more insight into DPT.

C. Coupled Line Analysis of DPT

A coupled line model proposed for transformers in board-level designs [17], [18] and later adapted for transformers in silicon technology has proven valuable in analyzing monolithic transformers [19], [20]. In this section, we employ the coupled line model to analyze DPT. To do that, we solve the coupled line equations of each mode individually. Fig. 7 shows the coupled line model of DPT, where each section of DPT is considered as coupled lines. The DPT consists of two octagons with a line that connects the center of the octagons. In this figure, each octagon is divided into two sections, each having even and odd mode characteristic impedances, Z_{0e1} Z_{0o1} and electrical lengths, θ_1. Similarly, the middle line is also divided into two sections, each having even and odd mode characteristic impedances, Z_{0e2} Z_{0o2} and electrical lengths, θ_2. Input and output terminals are also shown in this figure.

1) Mode1: In mode 1, the current flow is similar to Fig. 6(a). Therefore, the middle line has no current flow and DPT is simplified as shown in Fig. 8. The resulting structure is similar to two fully differential transformers. Before solving this structure, we assume the Vdd terminal is connected to an ac ground. With this assumption, the Y-Parameter matrix of each transformer in this mode of operation is given by (1), as shown at the bottom of the next page.

Based on this equation, we have

$$\begin{bmatrix} I_{\text{dev}} \\ I_L \end{bmatrix} = \begin{bmatrix} -\frac{j}{2}Y_p\cot(\theta_1) & -\frac{j}{2}Y_m\cot(\theta_1) \\ -\frac{j}{2}Y_m\cot(\theta_1) & -\frac{j}{2}Y_p\cot(\theta_1) \end{bmatrix} \begin{bmatrix} V_{\text{dev}} \\ V_L \end{bmatrix} \quad (2)$$

where, $V_{\text{dev}} = V_1 - V_2$, $V_L = V_3 - V_4$, $I_{\text{dev}} = I_1 = -I_2$, $I_L = I_3 = -I_4$. Also, $Y_p = (Y_{0e} + Y_{0o})/2 = (Z_{0e} + Z_{0o})/2$ and $Y_m = (Y_{0e} - Y_{0o})/2 = (Z_{0o} - Z_{0e})/2$. Using (2), and the fact that $I_L = -(1/2)Y_L V_L$, (I_L, and V_L are load current and voltage, respectively), we calculate input admittance which should be equal to the conjugate of optimum differential output admittance of one differential pair

$$Y_{\text{in}} = \frac{Y_{\text{dev}}}{I_{\text{dev}}} = -\frac{j}{2}\cot(\theta_1)\left(Y_p + \frac{{Y_m}^2\cot(\theta_1)}{Y_L - jY_p\cot(\theta_1)}\right). \quad (3)$$

2) Mode 2: In mode 1, due to the symmetry of the structure, the DPT is divided into two separate transformers (left and right), and it was analyzed. In mode 2, however, currents from terminals 1 and 3 both enter the middle line and return to their respective negative terminals (2 and 4). Therefore, DPT in mode 2 can be decomposed into two distinct transformers: the upper and the lower. In this way, coupled line analysis can be applied. Fig. 9 shows the upper half of DPT in mode 2. When analyzing the upper and lower half of DPT in this mode, characteristic impedances of the middle line need to be doubled in the upper and lower halves to account for currents from T1 and T3 flowing into the middle line. Also, the electrical length of the middle line is different than the other sections. This structure is composed of four coupled lines in a cascaded form. The two sections in the middle are similar in terms of their characteristic impedance and electrical lengths. Also, the first and last sections are similar in the same way. By multiplying the ABCD parameter of the first and second

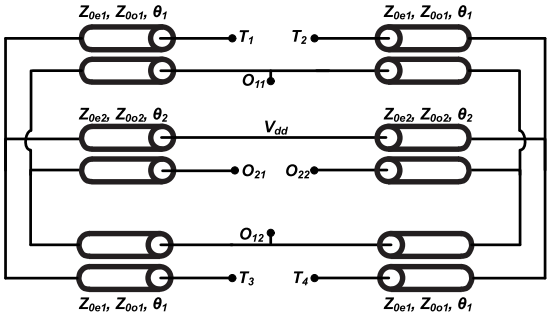

Fig. 7. Coupled line model of DPT.

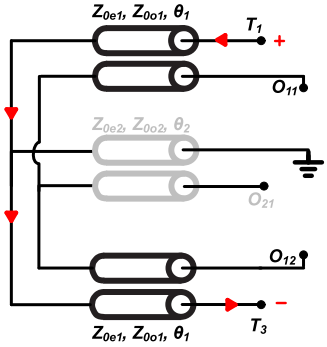

Fig. 8. Left half of the coupled line model of DPT in mode 1.

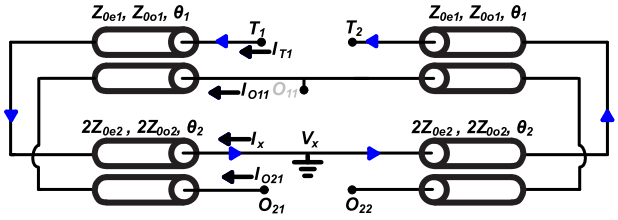

Fig. 9. Upper half of the coupled line model of DPT in mode 2.

sections, terminal voltage and current of the left half circuit is achieved.

Equation (4), as shown at the bottom of the next page, provides the ABCD parameter of the left half of Fig. 9. We may calculate the ABCD of the right half in the same way, and then after applying $Vx = 0$ and algebraic manipulations, input admittance of the upper half of DPT in mode 2 is calculated

III. DPT-Based PA

Section II presents the basics of DPI and DPT in detail. In this section, we incorporate the developed DPT into a PA's output and input matching circuits and demonstrate the feasibility of incorporating the proposed low-loss DPT in amplifier design. In this work, we use a conventional class-AB for the active devices and implement the DPT at the input and output matching networks. The design of differential class-AB amplifiers is presented in detail in [21] and [22], therefore we will not focus on the basics of differential PA design here.

TABLE I
Summary of Load-Pull Simulation Results

	39GHz	28GHz
Optimum Load Impedance	10.5+20j (48.5‖25.5j)	15+25j (56‖34j)
$Pout_{Active}$(dBm)	15.1	16.3
PAE_{Active}(%)	47	54
$Gain_{Active}$(dB)	9.7	10.4
Compression(dB)	2.5	2.7
Input Impedance	2.8-24.9j	2.5-35.3j

A. DPT as Output Matching

Earlier it was mentioned that the currents at the secondaries of DPT are combined. Therefore, DPT operates as a parallel power combiner. Different architectures of power combiners such as series, parallel, and series-parallel are described in prior works [21], [22], [23]. DPT is a two-way parallel power combiner that can operate in two different frequency bands based on the phases of excitation signals at the primary coil in a compact area compared to prior two-way parallel combiners.

Fig. 10(a) shows the top view of the output matching network. As shown in this figure, all the terminals of the DPT are located at the center of this inductive element. In order to connect the terminals of the DPT to loads and transistors, specific transmission lines are required to connect T_1–T_4 to the drain of M1–M4, as well as output terminals, O_{11}–O_{22} to loads 1 and 2. Vias from AP layer to metal 9, and from metals 9 to 8 are shown in this figure to provide a clear view of signaling in this structure. Metal 9 and eight layers are used for the primary and secondary coils. AP plus metal 8 and nine layers are used for making interconnections. Also, Fig. 10 shows the location of VDD connection. The midpoint of the center line on the primary coil can be used to apply the power supply to the active devices, similar to the center tap in conventional transformers acting as ac ground. The supply voltage is provided from each side of DPT through the AP layer using underpasses connected to the midpoint of the center line. Fig. 10(b) shows a 3-D view of the output matching network occupying 250 × 92 um.

$$\begin{bmatrix} I_{T1} \\ I_{T3} \\ I_{O11} \\ I_{O12} \end{bmatrix} = \begin{bmatrix} -j\dfrac{2Y_P^2\cos(\theta_1)-Y_m^2}{Y_p\sin(2\theta_1)} & j\dfrac{Y_m^2}{Y_p}\csc(2\theta_1) & -jY_m\cot(2\theta_1) & jY_m\csc(2\theta_1) \\ j\dfrac{Y_m^2}{Y_p}\csc(2\theta_1) & -j\dfrac{2Y_P^2\cos(\theta_1)-Y_m^2}{Y_p\sin(2\theta_1)} & jY_m\csc(2\theta_1) & -jY_m\cot(2\theta_1) \\ -jY_m\cot(2\theta_1) & jY_m\csc(2\theta_1) & -jY_p\cot(2\theta_1) & jY_p\csc(2\theta_1) \\ jY_m\csc(2\theta_1) & -jY_m\cot(2\theta_1) & jY_p\csc(2\theta_1) & -jY_p\cot(2\theta_1) \end{bmatrix} \begin{bmatrix} V_{T1} \\ V_{T3} \\ V_{O11} \\ V_{O12} \end{bmatrix} \quad (1)$$

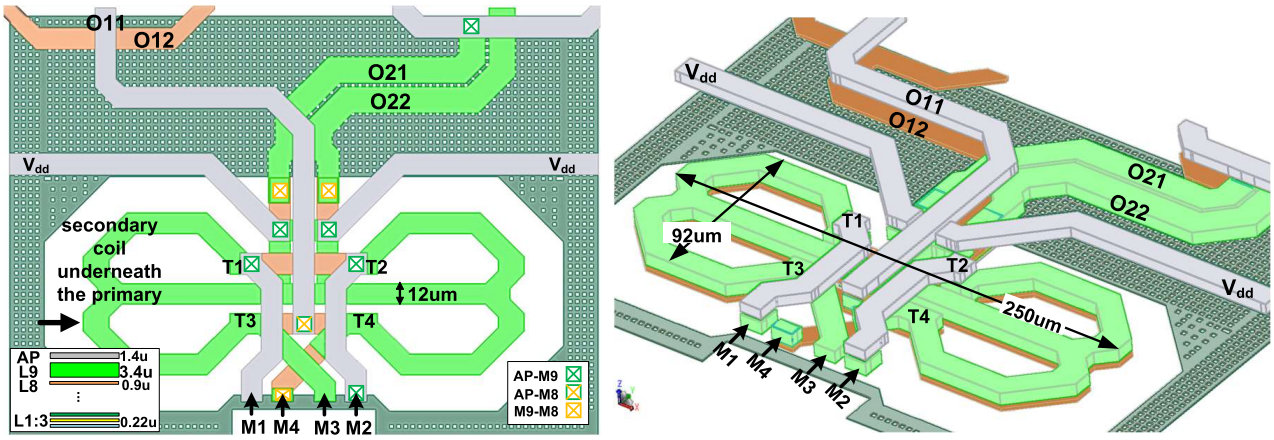

Fig. 10. DPT layout as output matching network and parallel power combiner with 3-D view.

Fig. 11 shows a simplified schematic of the DPT-based dual-band PA. In this schematic, the signal source in red (In1) is operating at a higher frequency band corresponding to mode 1 and the source in blue operates at a lower frequency band corresponding to mode 2. Also, Loads 1 and 2 are associated with outputs of modes 1 and 2, respectively. As mentioned in Section III-A, the DPT can be used as a matching element and power combiner/divider on the output/input side. Therefore, the signal launched at In1 enters to input DPT and is divided between the differential pairs through (T_{i1}–T_{i4}). In addition to power division and power matching at the input of differential pairs, it generates the proper signal phases for each transistor (Fig. 11). For example, if the input DPT is excited from the I_{11}–I_{12} ports in Fig. 11, the corresponding signal polarities shown in red are generated. If the input DPT is excited from the I_{21}–I_{22} ports, signal polarities shown in blue in Fig. 11 are generated. Also, the currents injected to output DPT are summed at Loads 1 or 2 based on the operation mode defined by the input sources. The PA consists of four transistors forming two differential pairs, emulating the current sources of Fig. 6. In this implementation, no switch is incorporated in the design of the output and input matching circuit to select the operating frequency.

Since the output terminals of DPT are separated for each differential output port, two sets of differential transmission lines are needed to connect those ports to associated pads. IM1, IM2, and OM1, OM2 in Fig. 11 are dedicated to this purpose and are absorbed into the corresponding matching networks Therefore, In1 and In2 are connected to the input DPT through IM1 and IM2, and Loads 1 and 2 are connected to the output DPT through OM1 and OM2, respectively.

B. Active Devices and Circuit Topology

DPT-based PA is proposed for mm-wave 5G communication PAs when noncontiguous operation bands exist. To implement this PA, the performance of the active devices is important since the passive devices can be optimized for each frequency

$$\begin{bmatrix} V_{T1} \\ V_{O11} \\ I_{T1} \\ I_{O11} \end{bmatrix} = \begin{bmatrix} \cos(\theta_1+\theta_2) & 0 & j\dfrac{Y_p \sin(\theta_1+\theta_2)}{{Y_p}^2-{Y_m}^2} & -j\dfrac{Y_m \sin(\theta_1+\theta_2)}{{Y_p}^2-{Y_m}^2} \\ 0 & \cos(\theta_1+\theta_2) & -j\dfrac{Y_m \sin(\theta_1+\theta_2)}{{Y_p}^2-{Y_m}^2} & j\dfrac{Y_p \sin(\theta_1+\theta_2)}{{Y_p}^2-{Y_m}^2} \\ jY_p \sin(\theta_1+\theta_2) & jY_m \sin(\theta_1+\theta_2) & \cos(\theta_1+\theta_2) & 0 \\ jY_m \sin(\theta_1+\theta_2) & jY_p \sin(\theta_1+\theta_2) & 0 & \cos(\theta_1+\theta_2) \end{bmatrix} \begin{bmatrix} V_X \\ V_{O21} \\ -I_X \\ -I_{O21} \end{bmatrix} \tag{4}$$

$$I_{T1} = -j\frac{-\frac{1}{2}[\cos(\theta_1-\theta_2)+3\cos(\theta_1+\theta_2)]\left[\left({Y_m}^2-2{Y_p}^2\right)V_{T1}+{Y_m}^2V_{T3}\right]+2Y_mY_p(V_{O21}-V_{O22})}{Y_p[3\sin(\theta_1+\theta_2)+\sin(\theta_1-\theta_2)]} \tag{5}$$

$$I_{T3} = j\frac{+\frac{1}{2}[\cos(\theta_1-\theta_2)+3\cos(\theta_1+\theta_2)]\left[{Y_m}^2V_{T1}+\left({Y_m}^2-2{Y_p}^2\right)V_{T3}\right]+2Y_mY_p(V_{O21}-V_{O22})}{Y_p[3\sin(\theta_1+\theta_2)+\sin(\theta_1-\theta_2)]} \tag{6}$$

$$I_{O21} = j\frac{-\frac{1}{2}\left(Y_m(V_{T1}-V_{T3})[2\cos(\theta_1-\theta_2)+6\cos(\theta_1+\theta_2)]+Y_pV_{O21}[\cos(2\theta_1-2\theta_2)-9\cos(2\theta_1+2\theta_2)]+8Y_pV_{O22}\right)}{[3\sin(\theta_1+\theta_2)+\sin(\theta_1-\theta_2)][3\cos(\theta_1+\theta_2)+\cos(\theta_1-\theta_2)]} \tag{7}$$

$$I_{O22} = j\frac{\frac{1}{2}\left(Y_m(V_{T1}-V_{T3})[2\cos(\theta_1-\theta_2)+6\cos(\theta_1+\theta_2)]+8Y_pV_{O21}+Y_pV_{O22}[\cos(2\theta_1-2\theta_2)-9\cos(2\theta_1+2\theta_2)]\right)}{[3\sin(\theta_1+\theta_2)+\sin(\theta_1-\theta_2)][3\cos(\theta_1+\theta_2)+\cos(\theta_1-\theta_2)]} \tag{8}$$

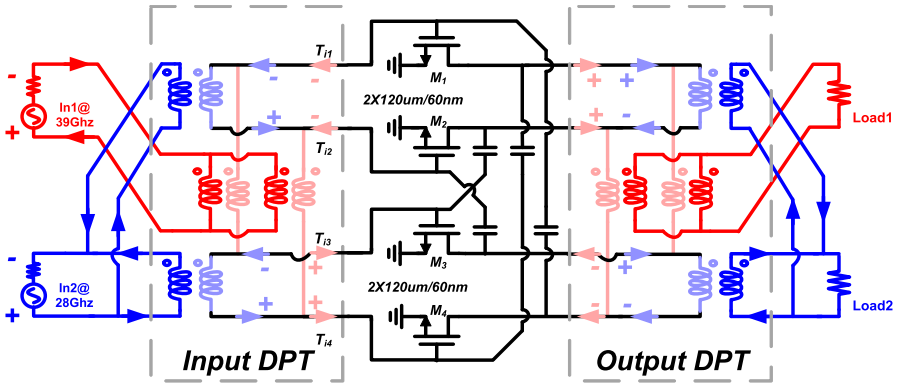

Fig. 11. Simplified schematic of the DPT-based dual-band PA.

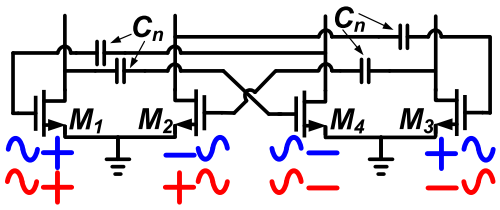

Fig. 12. Capacitive neutralization scheme proposed for DPT-based PA.

band. If the active device performance is not optimized for both frequency bands, the performance of the final amplifier is under optimal conditions.

Capacitive neutralization is a very efficient way to boost the performance and stability of differential PAs. They are achieved by reducing the reverse signal transmission [24]. However, to apply the neutralization technique to DPT-based PA it is important to consider the fact that neutralization should be applied in both modes of operation. Obviously, by examining the polarity of signals at the gate and drain of transistors in Fig. 11, we realize if the neutralization capacitors are applied between the M_1–M_2 and M_3–M_4 (the traditional way), $C_{\rm gd}$ of those transistors are neutralized in mode 2 but $C_{\rm gd}$ is doubled in mode 1. To solve this problem and take advantage of capacitive neutralization in both modes, finding a pair of transistors that have out-of-phase signal polarities in both operation modes is necessary.

By examining the polarity of signals at the drain and gate of M1 and M4 (Fig. 11), it is clear that both modes keep their signal polarities out of phase. Similarly, M_2 and M_3 have out-of-phase signal polarities but interchange them. Therefore, we consider these two transistors as the second differential pair. Fig. 12 shows the proposed differential pairs of DPT-based PA. In this figure, the neutralization capacitor C_n that equals to $C_{\rm gd}$ of the transistors is placed between the gates and drains of M_1–M_4 and M_2–M_3. In this way, $C_{\rm gd}$ of the transistors is neutralized in both operation modes. To implement the neutralized differential pairs, there are two possible ways. One is described in Fig. 12. For example, the designer can connect the neutralization capacitor from the gate of M1 to the drain of M4 in the layout which belongs to the other differential pair. By following the same approach for other connections, the layout of differential pairs needs to be done concurrently, making it complicated. The second way is to position M4 adjacent M1 and M2 next to M3. In this way, the layout of the differential pair is similar to a conventional differential pair. The only thing we need to consider is the connection of the drains of the transistors to DPT. In this work, the second method is used and C_n is implemented using high-density MOM capacitors available in the technology we used.

In addition, DPT-based PA can be designed to provide wide operation bandwidth in each mode or both modes (i.e., wideband in lower or higher frequency band or both bands). There are different techniques to increase the bandwidth of the amplifier. In this work, we choose the method presented in [22]. Although we are focusing on dual-band operation, different techniques such as increasing the bandwidth, improving efficiency, or linearity can also be applied to design DPT-based PA. In this case, the transistors are designed to show output resistance close to the load impedance, resulting in a very small impedance transformation ratio. With a 1.2 V supply voltage in the 65 nm CMOS process, we choose 120 μm for the size of each transistor with 0.125 mA/μm current density for each transistor in the pair which provides close to 50 Ω output resistance.

Fig. 13 shows the load-pull simulation results of two RC-extracted differential pairs with the capacitive neutralization presented in this section. The simulation results are summarized in Table I. The differential pairs are connected in parallel to the source and load of the load-pull testbench. As observed, the optimum output resistances are slightly different, while the equivalent output capacitors are nearly identical (160 f and 167 fF at 39 and 28 GHz, respectively). The output capacitor is determined by the physical shape and size of the device, whereas the output resistor comes from the ratio of the transistor's output current and its output voltage swing, in other words, the load-line. Output voltage swing depends on the output current of the device. A good representation of the speed characteristics of transistors is the maximum-available-gain versus frequency. As frequency goes higher, the available gain of the device drops and so does the value of the output resistance of the device. In 65-nm CMOS process, $G_{\rm max}$ of the differential pair drops by more than 2 dB in the frequency range of 28 to 39 GHz, representing a significant degradation. Therefore, the real part of the output

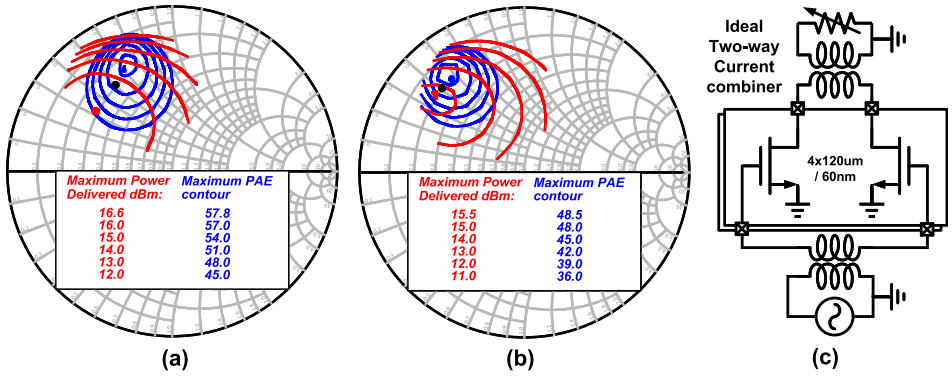

Fig. 13. Load pull simulation results of two-way current combined differential pair. (a) Lower. (b) Higher frequency band. (c) Loadpull test setup.

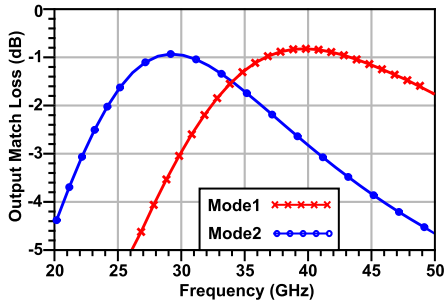

Fig. 14. DPT-based output matching performance at higher and lower frequency bands.

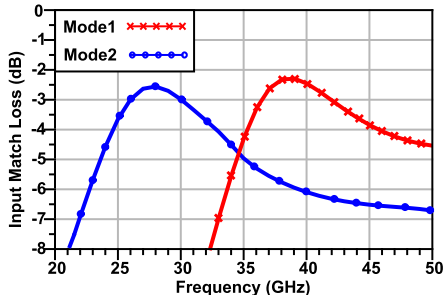

Fig. 15. DPT-based Input matching performance at higher and lower frequency bands.

impedance can not remain the same. On the other hand, a fixed output capacitor at the output of the differential pair requires different values of inductance at different frequencies. Obviously, at 28 GHz, it needs a larger inductance value compared to 39 GHz. Therefore, to get the best output performance for the devices, the optimum load impedances should be designed for each frequency band individually, highlighting the DPT's role in providing those impedances.

C. DPT as an Input Matching Network

DPT's operation depends on the relative phases of signals that enter the primary terminals of DPT so that one of the output loads can be activated. The circuit duality relationship allows us to excite the DPT from O_{11}–O_{12} (O_{21}–O_{22}) and get the proper phases associated with mode 1 (mode 2). Therefore, there is no need for extra circuitries to implement relative phases for operating DPT-based PA. DPT is a transformer that is one of the conventional ways to match the source impedance to the load. Therefore, DPT can perform impedance transformation. As shown in Fig. 11, the DPT at the input of PA is used for input matching, power division, and required phase shift. The optimum impedances of the two differential pairs (shown in Fig. 13(a) and (b) and listed in Table I) are used to design the output and input matching networks using the DPT. The output DPT needs to transform 10.5-20j at 39 GHz and 15-25j at 28 GHz to Loads 1 and 2 in Fig. 8. In our case, both Loads 1 and 2 are 50 Ω. Using EM simulation tools from Keysight we have designed and optimized the size and shape of the DPT. Fig. 14 shows the performance of the DPT-based output matching network in modes 1 and 2. DPT achieves a peak output match loss of 0.8 and 0.9 dB at higher and lower frequency bands, respectively while the 50 Ω load is matched to the optimum impedance of transistors shown in Table I. Fig. 15 also shows the DPT-based input matching performance in modes 1 and 2. The input matching network achieves a peak input match loss of 2.2 and 2.5 dB in modes 1 and 2, respectively. 50 Ω source impedance is matched to the input impedance of transistors shown in Table I in each mode of operation. Fig. 16 shows the voltage swing at the input of each transistor. As we can see in mode 1, $V_{\mathrm{Ti1,2}}$ and $V_{\mathrm{Ti3,4}}$ have similar phases, and in mode 2 $V_{\mathrm{Ti1,3}}$ and $V_{\mathrm{Ti2,4}}$ have similar phases.

D. Performance Estimation of DPT-Based PA

This section presents a useful estimation of PA performance based on load-pull simulation and output/input matching network performance. The topology of the proposed DPT-based PA is a single-stage amplifier; therefore, the total gain, output power, and input power of the amplifier could be written as

$$\mathrm{Gain}_{\mathrm{Amp}} = \mathrm{Gain}_{\mathrm{Active}} \times \frac{1}{\mathrm{Loss}_{\mathrm{Output}} \times \mathrm{Loss}_{\mathrm{Input}}} \tag{9}$$

$$P_{\mathrm{out}_{\mathrm{Amp}}} = \frac{P_{\mathrm{out}_{\mathrm{Active}}}}{\mathrm{Loss}_{\mathrm{Output}}} \tag{10}$$

$$P_{\mathrm{in}_{\mathrm{Amp}}} = P_{\mathrm{in}_{\mathrm{Active}}} \times \mathrm{Loss}_{\mathrm{Input}} = \frac{P_{\mathrm{out}_{\mathrm{Active}}}}{\mathrm{Gain}_{\mathrm{Active}}} \times \mathrm{Loss}_{\mathrm{Input}}. \tag{11}$$

On the other hand, assuming the matching networks at the output and input do not consume power, dc power

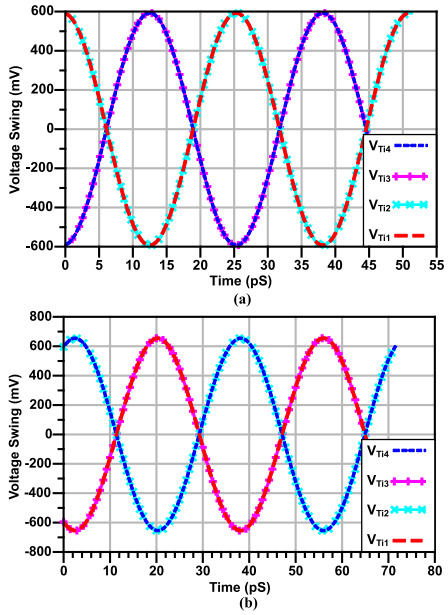

Fig. 16. Voltage swing and relative phases at the gates of each transistor (a) mode 1 and (b) mode 2.

TABLE II

CALCULATION OF AMPLIFIER PERFORMANCE PARAMETERS BASED ON KNOWN ACTIVE AND PASSIVE PERFORMANCE PARAMETERS

		39GHz	28GHz
Known Parameters	**PAE_{Active}**	47 %	54 %
	$Gain_{Active}$	9.7 dB	10.4 dB
	$Pout_{Active}$	15.1 dBm	16.3 dBm
	$Loss_{output}$	0.8 dB	0.9 dB
	$Loss_{Input}$	2.2 dB	2.5dB
PA Performance Calculations	**PAE_{Amp}**	30.9 %	34.4 %
	$Pout_{Amp}$	14.3 dBm	15.4 dBm
	$Gain_{Amp}$	6.7 dB	7 dB

consumption is the same as the active device. Thus,

$$P_{\mathrm{dc}} = \frac{P_{\mathrm{out}_{\mathrm{Active}}} - P_{\mathrm{in}_{\mathrm{Active}}}}{\mathrm{PAE}_{\mathrm{Active}}}. \tag{12}$$

By putting (9)–(12) to into PAE formula we have

$$\mathrm{PAE}_{\mathrm{Amp}} = \mathrm{PAE}_{\mathrm{Active}} \times \frac{\mathrm{Gain}_{\mathrm{Active}} - \mathrm{Loss}_{\mathrm{Output}}\mathrm{Loss}_{\mathrm{Input}}}{\mathrm{Loss}_{\mathrm{Output}}(\mathrm{Gain}_{\mathrm{Active}} - 1)}. \tag{13}$$

Equation (13) is an important relation between the active devices' gain and input and output matching losses. If $\mathrm{Gain}_{\mathrm{Active}} \gg 1$ then (13) can be written as

$$\mathrm{PAE}_{\mathrm{Amp}} = \mathrm{PAE}_{\mathrm{Active}} \times \frac{1}{\mathrm{Loss}_{\mathrm{Output}}}. \tag{14}$$

This equation roughly gives an idea of how the output matching loss degrades the efficiency of a given amplifier. Using 13 and parameters of the active devices from load-pull and EM simulation results of output and input matching circuits, an estimation of the performance of the resulting PA can be obtained. Having an estimation of achievable PA performance in the early stages of the design is beneficial.

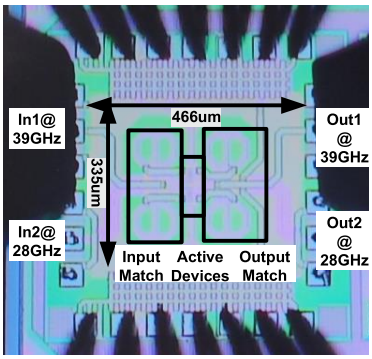

Fig. 17. Chip microphotograph of implemented dual-band DPT-based PA.

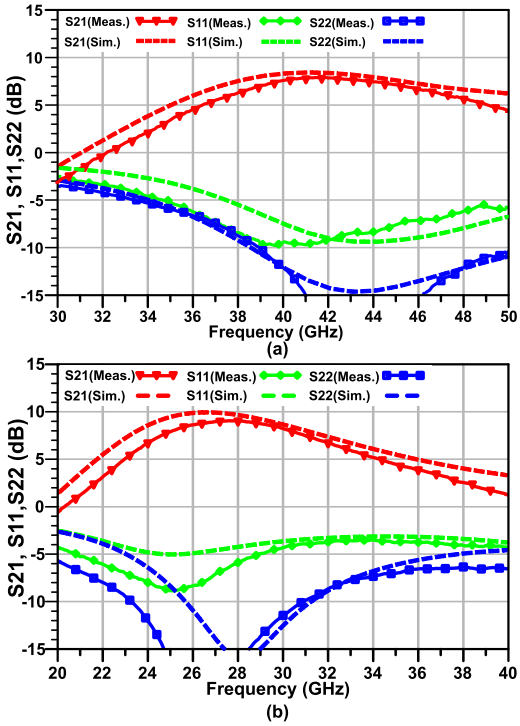

Fig. 18. Small signal measurements of DPT-based PA (a) higher band and (b) lower band of operation.

IV. IMPLEMENTATION AND MEASUREMENTS

DPT PA presented in this article is a single-stage amplifier design, however, it can be extended to a multistage design. Since DPT is a current combined transformer the design methodology used in [21] and [23] can be applied to DPT-based PA design. In this design 50 Ω source impedances are matched to inputs of transistors, However, the coil connected to the input signal source could be used to resonate out the output capacitor of the driver amplifier, in this way, DPT can be incorporated in the interstage matching network between the output of the driver and the inputs of the output stage. On the other hand, any other form of input matching network that generates proper phases for the correct operation of output DPT network can serve as an input or intermediate matching network. This could include but is not limited to switched matching networks. In this case, since the switches are implemented at the low power side of the amplifier,

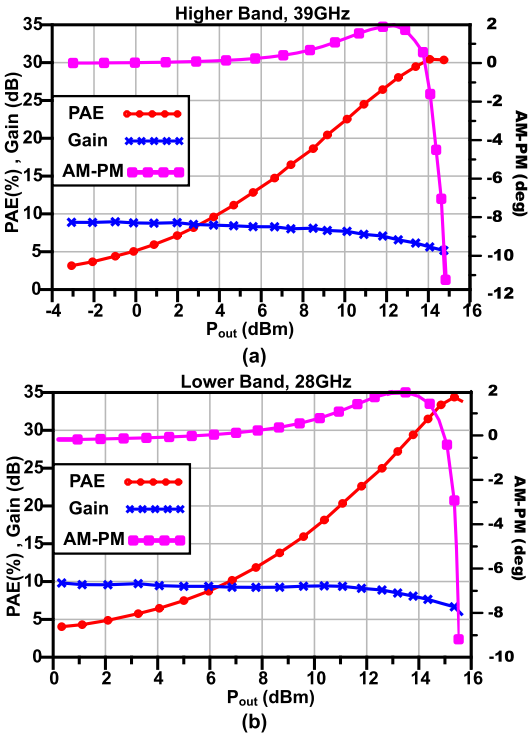

Fig. 19. Large signals measurements (a) higher band, 39 GHz and (b) lower band, 28 GHz.

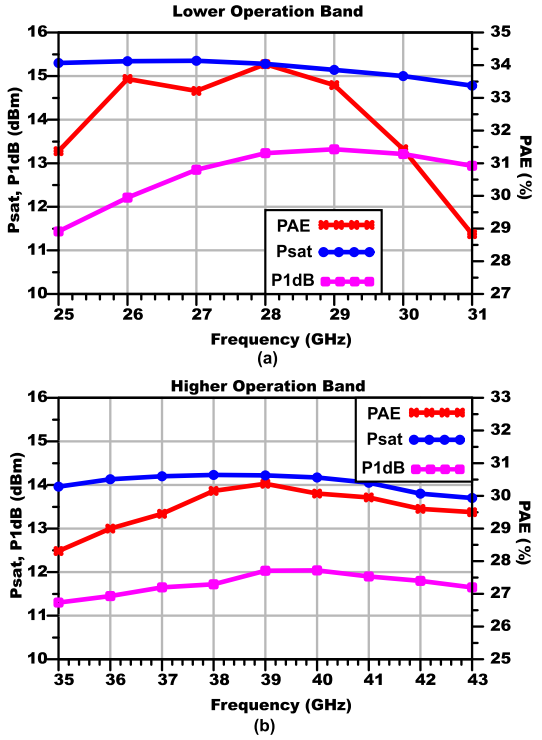

Fig. 20. Psat, P1dB and PAE of DPT-PA (a) lower band and (b) higher band.

the effect of switch losses on the amplifier's efficiency is smaller, according to (13). Fig. 17 shows a single-stage DPT-based PA prototype implemented in TSMC 65-nm CMOS process. The PA core occupies 466 by 335 μm. Input–output matching networks and active devices are shown in this figure. Transistors are sized at 120 μm/65 nm with a current density of 0.125 mA/μm under a supply voltage of 1.2 V.

There are two GSG probe pads on the input and two GSG pads on the output side (Fig. 17). In this figure, the GSG probes are landed on In1 and Load 1 pads. Our available probing system does not allow us to probe all 4 GSG pads at the same time, however, As it was described before, since the DPT operation is based on the relative phase of excitation signals when the DPT-based PA is operating in one of its operation modes, the other mode is isolated meaning that the impedance connected to input–output GSG corresponding to the other mode has virtually no effect on the performance of the active operating mode. Therefore, having an open or short termination on input–output pads of mode 1 (shown in Fig. 17) does not have any effect on the operation and performance of DPT-based PA in mode 2.

A. Small and Large Signal Measurement

Fig. 18(a) and (b) show the small-signal measurements of dual-band DPT-based PA in the lower and higher bands of operation, respectively. Small signal measurements are carried out using N5047A PNA-X from Agilent and i67-A-GSG-75 probes from Cascade Microtech. Calibration is done up to the probe tips using the short-open-line-through (SOLT) routine and impedance standard substrates (ISS). The single-stage DPT-based PA achieves a peak gain of 9 dB at 28 GHz and 8 dB at 42 GHz. In the lower band of operation, the PA has 4.9 GHz (25.2–30.1) and 6.5 GHz (39.1–45.6) of 1 dB bandwidth which reasonably supports most mm-wave 5G frequency bands. An excellent agreement between the simulation and measurements is achieved.

Continuous-wave large-signal measurement is done using PSG E8257D and N9030A vector signal analyzer. The PA prototype archives 15.3 and 14 dBm of saturated output power while having 34.1% and 30.2% efficiency at 28 and 39 GHz bands, respectively. Fig. 19(a) and (b) show the large-signal performance of the DPT-based PA in lower and higher bands of operation, respectively. Fig. 20 shows the saturated output power, P1dB, and power-added efficiency of DPT-PA at higher and lower operation frequency bands. As it was mentioned earlier the PAE of the PA is largely affected by the active devices gain and it limits the maximum achievable PAE of the DPT-based PA.

B. Modulated Signal Measurement

High-order modulation schemes require very stringent linearity characteristics for PAs. To make sure the PA can amplify the high-order modulated signals with good linearity performance, it is necessary to characterize the PA under modulated signals that are present in today's communication systems.

A custom test setup for the modulated signal measurements is incorporated. In this test setup, a ZCU111 evaluation board from Xilinx which has 8× 12bit, 4.096 GSPS RF-ADCs, and 8× 14 bit 6.554 GSPS RF-DACs is used for signal generation and analysis purposes. The modulated signals are uploaded into the high-speed DAC memory. The IQ signal is upconverted using quadrature mixers in the digital domain and

TABLE III
COMPARISON WITH THE STATE-OF-THE-ART SILICON-BASED MM-WAVE PAS

	This Work	[25]	[26]	[10]	[27]	[28]	[29]	[19]	[30]	[31]	[32]	[33]	[34]	[35]	[13]	[8]
Tech.	65nm CMOS	130nm SiGe	40nm CMOS	28nm CMOS	28nm CMOS	28nm CMOS	22nm FD SOI	45nm SOI	45nm SOI	65nm CMOS	130nm SiGe	65nm CMOS	65nm CMOS	45SOI	28nm CMOS	65nm CMOS
Operating Frequency	25-30* 39-45*	24-38	27	29-57	38.5	36	28	24-42	29	26-42	28	28	28	28	26.5 37	24-29.5
P_{sat} (dBm)	15.3 14.0	14 13	15.1	16.6 15.9 15.1	16.8	22.6	22.5	20.0 17.9	22.7	19.6	19	23.2	23.2	17.9	20.2 19.1	16.8 18
P_{1dB} (dBm)	13.2 12.1	11 12	13.7	13.4 11.1 10.9	14.9	19.6	21.1	19.6 15.7	-	19.1	-	22	22.7	15.6	18.7 18.6	16 17.6
PAE_{max} (%)	34.1 30.2	25 26.7	33.7	24.2 18.4 14.9	32.9	32	28.5	38.9 35	42.6	24	34	33.5	35.5	22	33.6 32	20.8
Gain (dB)	9, 8	11.2 10.2	22.4	20.8	25.8	18	26.1	20.5	(TX)30	13.5	9.7	15.9	18	16.8	13.0 10.7	(TX)24.5
Supply (V)	1.2	2.4	1.1	0.9	1.8	1	2.4	2	2	1.1	3.7	2.4	2.2	1.2	2.2	1.0/1.8
Modulation Scheme	64 QAM	64 QAM	64 QAM OFDM 8CC	64 QAM	64 QAM OFDM	64 QAM	64 QAM	64 QAM OFDM 2CC	64 QAM	64 QAM OFDM	64 QAM OFDM	256 QAM	64 QAM	64 QAM OFDM	64 QAM	NR 64,256 QAM
Data Rate (Gbps)	2.4	1.8-4.8	4.8	3	8.4	12 18	2.4	4.8	3	12	0.6	0.8	15	2.4	0.6	2.4 0.8
P_{avg} (dBm)	6.5 5.5	8.4 7.4	6.7	6.8 8.1 8.9	10.3	16 15.5	10.9	10.9 8.4	16	9.7	11.9	18.02	16.1	8	14.7 12.3	10.5, 7.2
PAE_{avg} (%)	12 10	17 17	11	2.9 3.9 4.4	16.9	22 20	9.2	14.2 10.3	23.8	10	20.2	17.6	14.9	7	21.6 16.8	-
EVM (dB)	-25.3 -25.4	-27 -29	-25	-25	-25.3	-25 -25.1	-25.1	-25.1 -25.1	-25.3	-22.4	-26.2	-31.2	-26.2	-30	-25.3 -24.1	-25, -29
ACPR (dB)	-29.25, -30.1	-29	-31	-37.6 -34.2 -30.2	-32.9 -30	-	-30.4	-25.2 -26.4	-29.8	-25	-33	-30	-28.32	-30	-22 -23	-25
Area (mm^2)	0.156	0.14	0.23	0.16	0.07	1.44	0.2	0.21	0.96	1.35	0.56	0.25	0.2	1.5	0.11	-

*1dB Bandwidth

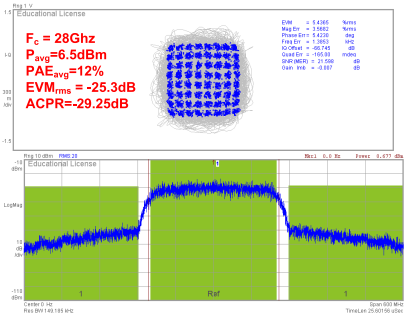

Fig. 21. Modulated signal measurements at the lower frequency band.

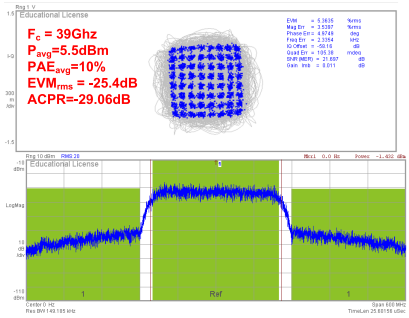

Fig. 22. Modulated signal measurements at the higher frequency band.

then converted into analog using one of the DACs on ZCU111 at 1966 MHz. The IF signal is then upconverted to the band of interest using the ADMV1013 microwave upconverter. After passing through the DUT, the signal is downconverted to an IF frequency to be digitized using ADC at 3072 MSPS. The digitized data is fed to and analyzed using VSA89600 software from Keysight.

The developed test setup has 2.8% and 2.9% EVM at 28 and 39 GHz when a 200 MSymbol/S 64-QAM signal is used. Thus, the effect of measurement setup linearity on the DPT-based PA is negligible. The roll-off factor of the RRC filter is 0.22, and the number of symbols analyzed is 4096. The peak-to-average power ratio (PAPR) of the 64-QAM signal is 6.5 dB. The average power measurement is done using an Agilent N9030A PXA signal analyzer. DPT-based PA is then measured with the same modulated signal and sample rates for the DACs and ADCs. The results of modulated signal measurements are shown in Figs. 21 and 22. At the higher frequency band (39 GHz), the DPT-based PA achieves 5.5 dBm of average output power and 10% average power added efficiency while having −25.4 dB EVM and −29.06 dB adjacent channel power ratio (ACPR). At the lower frequency band (28 GHz) the DPT-based PA achieves 6.5 dBm of output power and 12% average PAE while showing −25.3 dB of EVM and −29.25 dB ACPR.

Table II shows calculation of amplifier performance parameters based on known active and passive performance

parameters. Table III shows the comparison of the proposed DPT-based PA with narrow-band, wideband, and dual-band PAs in recent publications [10], [19], [25], [26], [27], [28], [29], [30], [31], [32], [33], [34], [35]. It shows the benefits of DPT-based PA in terms of performance metrics while supporting two different sets of frequency bands separated 8 GHz away from each other.

V. Conclusion

In this article, we present a multiband mm-wave 5G PA based on the DPT enabling two sets of inductive values for the optimum design of output and input matching networks. Considering the wideband mm-wave PA design, the dual-band DPT-based PA can provide better performance compared to two single-band wideband PAs while occupying less area. The prototype PA is implemented in a 65 nm CMOS and achieves 15.3 and 14.0 dBm output power at 28 and 39 GHz frequency bands while having 34.1% and 30.2% PAE, respectively. The core PA occupies 0.156 mm^2 which is suitable for mm-wave 5G phased array beamforming transceivers.

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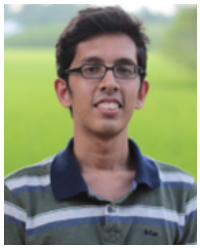

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