7.9 An 8b 6-12GHz 0.18mW/GHz DC Modulated Ramp-Based Phase Interpolator in 65nm CMOS Process

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In CDR, to sample time-interleaved ADCs with 4-phase inputs, the utilization of local clock generators including phase interpolators (PI) with high precision is imperative to eliminate phase offsets and prevent spurs at the ADC output. This necessitates either the parallel operation of two PIs with differential quad inputs driven by a DLL or the addition of an extra quad-generator at the 2-phase PI output, resulting in increased power consumption (Fig. 7.9.1). Similarly, baseband beamforming systems [1] for large-antenna arrays with wide signal bandwidth also require high-speed, linear, and fine-resolution PI for each antenna to compensate for the delay mismatch, while maintaining low power consumption (Fig. 7.9.1). This work proposes a low-power PI with power efficiency of 0.18mW/GHz implemented in 65nm CMOS with the capability to directly generate 4-phase PI outputs at clock frequencies of up to 6GHz without any DLL or quad generator at the input side suitable for CDR applications and 2-phase PI outputs of up to 12GHz.

Figure 7.9.1 illustrates various PI architectures. Both current (CMPI) [2] and voltage (VMPI) [3] mode PIs require extra slew-rate control to have overlapped input, resulting in increased overall power consumption. CMPI exhibits linearity issues, while VMPI experiences higher dynamic power consumption. In integrating mode PI (IMPI), integrated outputs with lower slope have higher noise and the integration slope varies a lot due to independent variations in the integrating current and capacitor [4]. In a ramp-based PI [1], the reduced swing ramp signal is noisy due to the noise coming from the integrating current source. Furthermore, the utilization of a static op-amp-based comparator, responsible for comparing the ramp signal with DAC outputs, limits the operational speed to 1.6GHz and contributes to 30% of the overall PI power, while the inclusion of a duty cycle controller (DCC) adds another 15% to the total power consumption. Additionally, it is worth noting that all these PIs need quad generators at their inputs, which is a challenging and power-consuming design at 12GHz.

The proposed PI produces signals with 50% duty cycle eliminating the need for a DCC and the need for an extra quad generator and input slew circuitry, while showcasing better linearity and high-frequency operation in 65nm CMOS. The proposed PI effectively mitigates the speed limitations and noise challenges commonly associated with ramp-based PIs. Importantly, it can generate both 4-phase and 2-phase outputs suitable for CDR applications, and these phases and operating speed can be further increased with technology scaling.

Figure 7.9.2 illustrates the proposed PI architecture and concept of operation. The ramp generator produces differential ramp signals using differential clock inputs. A low-power high-speed inverter-based comparator is designed to replace the static op-amp-based comparator. Further, a 6b input code D_{IN}<5:0> is fed to the DAC to generate 64 multi-level outputs, which are then used to modulate the DC level of the differential ramp signals. To implement this, the ramp signals are passed through series capacitors, with the other end of the capacitors connected to the DAC via a resistor. As the DAC code increases, the DC level of the ramp signals (V_{XI} and V_{XIB}) also rises proportionally. Subsequently, these differential DC-modulated ramp signals are compared with the threshold of the inverter (V_{TH}), resulting in PWM outputs (PWM_I and PWM_{IB}). The DAC output levels are set to vary within ±75mV from V_{TH} to accommodate the $300mV_{pp}$ ramp signal resulting in linear and power-efficient comparison in the mid-region of the ramp signal. This comparison generates PWM outputs with varying duty cycles and distinct delays ranging from 45° to 135° (up to 90° shift) depending on the 6b input code to the DAC. These PWM outputs can be converted to a 50% duty cycle output by injecting them into the ring oscillator (RO). However, injecting current directly into the RO through PWM signals with programmed delays leads to non-linear behavior at the RO output caused by phase shifts resulting from variations in injection strengths based on the duty cycle of the PWM signals. To mitigate this non-linearity, the PWM signals are routed to a pulse generator to create fixed-width pulses (V_A and V_B), which are perfectly aligned with the rising edges of the PWM signals. This ensures consistent injection strength at the fundamental frequency, regardless of the duty cycle of the PWM signal thereby mitigating the non-linearities at the output. Other higher-frequency components arising from the pulses are effectively filtered out due to the loop quality-factor of the oscillator. This synchronization makes the 4-stage RO lock-in alignment with the differential injection signal (V_A and V_B with phase shifting up to 90°) producing delayed 4-phase outputs. The phase delay varies based on the timing of injected pulsed signals (V_A and V_B) and is defined by the input code. For full 360° coverage, the quadrant select bits (D_{IN}<7:6>) toggle after the completion of every 90° quadrant in the 4-stage RO. To maintain uniform loading across the 4-stage RO, dummy loads are applied to the two nodes that are not receiving injections. Further, the quadrature outputs from the 4-phase signals from the RO are edge-combined using an XOR gate to produce differential outputs with twice the RO frequency as shown in Fig. 7.9.2.

Figure 7.9.3 shows a detailed circuit diagram of the ramp generator, which integrates capacitor current based on the differential input clocks to generate differential ramp signals. The internal loop within the replica bias sets the DC level of the ramp signal. To ensure the ramp's linearity across process corners, a V-to-I with switched cap load (C_L, using the same type of capacitor as C) is employed to generate bias current (I_{BIAS}) for the ramp generator. I_{BIAS} is directly proportional to C_L ensuring that the integrating current (I_{INT}) tracks variation in the capacitor (C) across PVT. Additionally, the inclusion of dummy switches in the design helps mitigate clock feedthrough at high frequency, preserving ramp linearity. A V_{TH} tracking circuit is introduced to ensure that the inverter's V_{TH} remains at $V_{DD}/2$ across PVT variations in the inverter-based comparator (Fig. 7.9.3). This circuit employs a feedback loop utilizing an op-amp to precisely control the current flowing through the PMOS and NMOS transistor to set the inverter output at $V_{DD}/2$ for $V_{in}=V_{DD}/2$ across PVT variations.

Low-swing ramp signals exhibit higher levels of phase noise primarily originating from the integrating current source, which is further amplified by the bias circuits due to the current mirror gain. These noise currents get sampled by the clock inputs and subsequently integrated at the capacitor (C), thereby affecting the phase noise in the ramp. However, this noise current undergoes high-pass filtering by the DC-modulated ramp signal by DAC architecture, effectively eliminating the low-frequency flicker noise (Fig. 7.9.3). To further reduce high-frequency noise, the bandwidth of the op-amp in the replica bias is strategically optimized, ensuring that there is no current gain in the high-frequency range from the bias circuit to the integrating current source. Furthermore, a 4-stage RO with pulses injected behaves like a first-order phase-locked loop (PLL) in the final stage, effectively rejecting high-frequency noise originating from the ramp generator. Noise generated by the inverters within the RO is mitigated through the injection loop. Additionally, the bandwidth of the injection-locking mechanism can be adjusted by varying the injection strength in accordance with the system jitter requirements. To ensure locking happens properly, an off-chip calibration circuit has been implemented to tune the bias voltage of the voltage-controlled current source responsible for driving inverters within RO.

Figure 7.9.4 shows the phase noise measured for five PI chips for two phase outputs operating at 12GHz with $68fs_{rms}$ jitter integrated from 100KHz to 1GHz. For PI linearity measurements, as the input code increases, the output is measured with respect to the reference clock signal. The PI presented in this work shows a maximum INL_{P-P} of 1.7LSB and DNL_{P-P} of 0.8LSB at 12GHz with a quad-error of max 0.8° at 6GHz (Fig. 7.9.5). This linearity can be improved through implementation in smaller technology nodes, where the comparator, functioning as a VTC (voltage-to-time delay converter), can linearly compare high-frequency, DC-modulated ramp signals with its threshold due to the lower parasitic cap. References [1] and [2] implemented in 65nm CMOS exhibit better linearity but [1] operates at a much lower frequency (1.6GHz) and [2] uses a CML architecture, consuming higher power. A power breakdown plot is shown in Fig. 7.9.5. The total power consumption of the PI is 2.2mW at 12GHz with a power efficiency of 0.18mW/GHz which is 2× better than prior state-of-the-art. Figure 7.9.6 shows a performance comparison of the proposed PI design with state-of-the-art PIs. The proposed PI is fabricated in a 65nm CMOS process, with an active area of 0.025mm², as shown in the chip micrograph in Fig. 7.9.7. In summary, this work proposes a low-power, low-noise, high-speed DC-modulated ramp-based PI for CDR and baseband beamforming applications.

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References:

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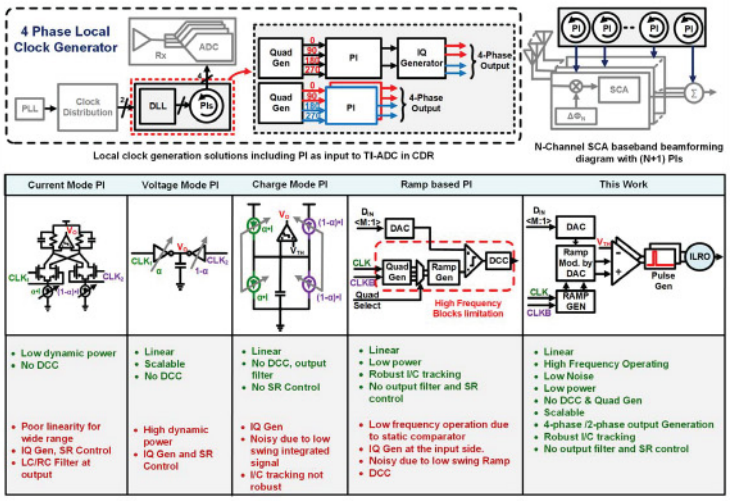
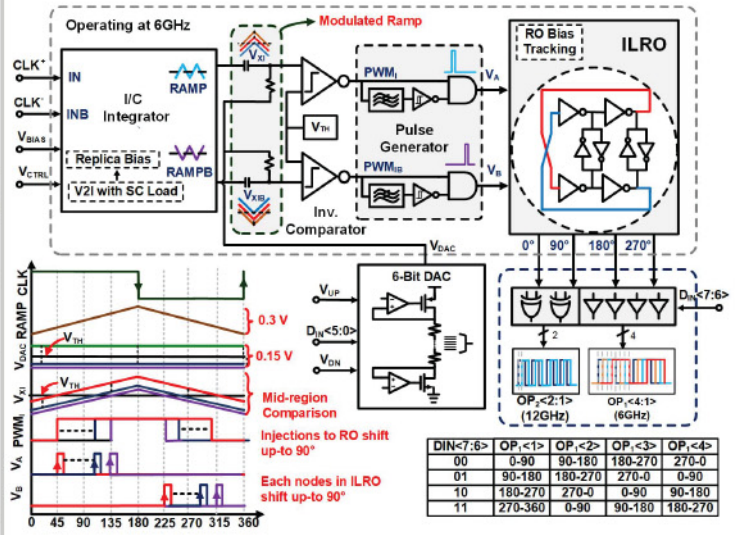


Figure 7.9.1: CDR and baseband beamforming application of PI, comparison of the prior PIs and the proposed architecture.



DIN<7:6>	OP1<1>	OP1<2>	OP1<3>	OP1<4>
00	0-90	90-180	180-270	270-0
01	90-180	180-270	270-0	0-90
10	180-270	270-0	0-90	90-180
11	270-360	0-90	90-180	180-270

Figure 7.9.2: The top level of the proposed PI architecture, illustrated with a timing diagram of its internal nodes.

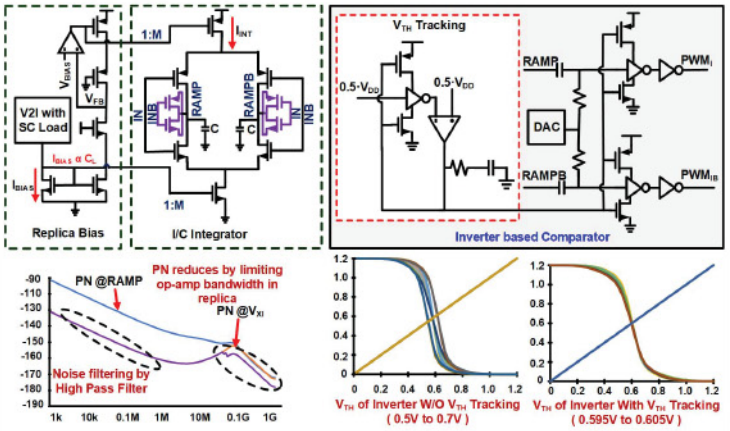


Figure 7.9.3: The ramp generator and inverter-based comparator circuit diagram with V_{TH} tracking; V_{XI} node phase noise after high-pass filtering and bandwidth control of op-amps.

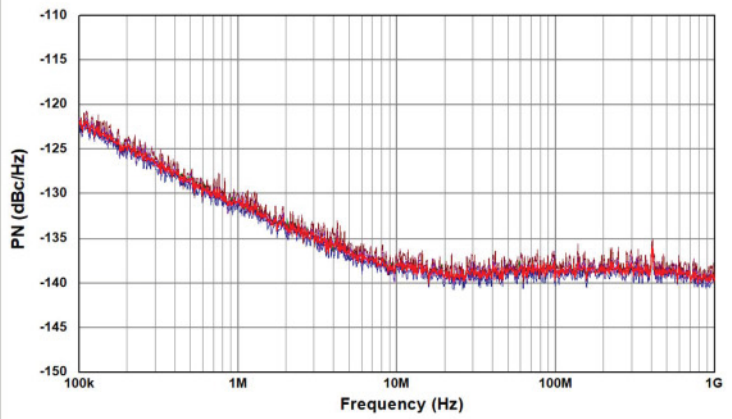


Figure 7.9.4: Phase noise plot for 5 PI chips operating at 12GHz. To show robustness across corners, 5 randomly selected chips have been tested and their phase noise is measured where the red curve shows the average phase noise.

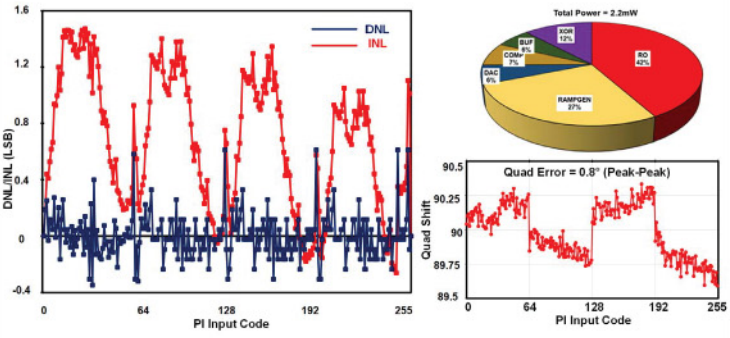


Figure 7.9.5: Measured INL/DNL of PI at 12GHz, quadrature error at 4-phase output at 6GHz (bottom right) and power breakdown plot (top right).

Metrics	This Work	Mohapatra JSSC'23[1]	Mishra ISSCC'22[4]	Huang ISSCC'19[5]	Wang ISSCC'22[2]	Chen ISSCC'18[3]
Arch.	DC Modulated Ramp based	Ramp based	IMPI	Injection Locked PR	CMPI	VMPI
Tech. (nm)	65	65	5	16	65	7
Res. (bits)	8	7	9	8	7	7
Freq. (GHz)	6-12	1.6	14	2-7	3.5-11	4-16
DNL (LSB)	0.8	0.52	2	1-1.45	1.1	1.2
INL (LSB)	1.7	0.52	3.47	1.06-1.84	1.14	1.8
Power (mW)	2.2	0.503	6	11.4 @7GHz	9.5 @7GHz	24.8
P.E. (mW/GHz)	0.18	0.315	0.43	1.63	1.36	1.55
Jitter (ps)	0.068 @12GHz (100 kHz-1GHz)	0.412 @1.6GHz (100Hz-10MHz)	0.071 @13.3GHz (3MHz-3GHz)	0.254 @7GHz (4MHz-3GHz)	0.06 @7GHz (0.1MHz-1GHz)	0.08
Supply (V)	1.2	1	0.75	1.2	1.2	1.2
Area (mm²)	0.025	0.021	0.006	0.0043	0.024	N/A

Figure 7.9.6: Table of comparison.

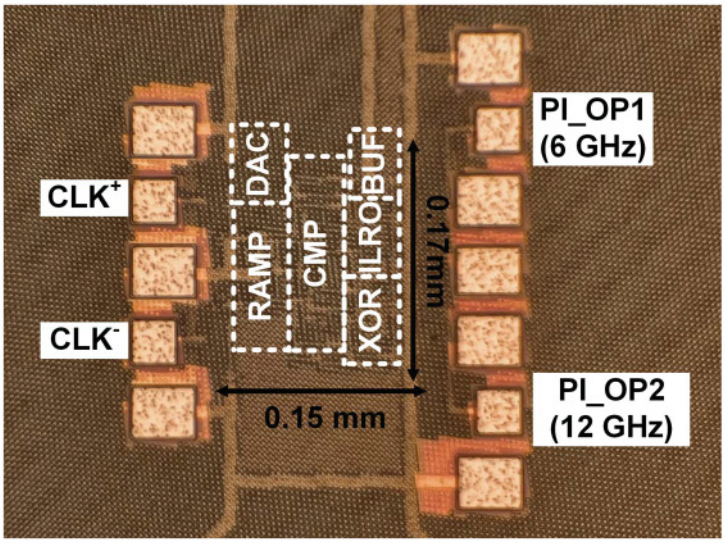


Figure 7.9.7: Chip micrograph of the PI in 65nm CMOS (active area = 0.0255mm²).

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