A 14 GHz Integer-N Sub-Sampling PLL With RMS-Jitter of 85.4 fs Occupying an Ultra Low Area of 0.0918 mm^2

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***Abstract*— This paper presents a 14 GHz sub-sampling PLL (SSPLL) with its phase noise analysis for Ku-band wireless transceivers. The performance enhancement of the phase-locked loop (PLL) over single-stage PLL in terms of jitter and power consumption is theoretically presented and verified with measured results. The proposed capacitor multiplier reduces the size of the loop filter capacitor by 28 times. The active capacitor VCO decreases the out-band phase noise while consuming less power. Fabricated in a 65 nm CMOS process with a core active area of 0.0918 mm^2, the SSPLL operates at 1.2 V supply achieving 13.2-14.8 GHz tuning range, 85.4 fs integrated jitter at 14 GHz, 8.42 mW power consumption, and -252.12 dB figure-of-merit (FoM). The measured results in-band and out-band phase noises of -108.6 dBc/Hz at a 1 MHz offset and -128.9 dBc/Hz at a 10 MHz offset, respectively.**

***Index Terms*— 5G, CPPLL, sub-sampling PLL, reduced area PLL, reduced capacitor, active capacitor voltage controlled oscillators, small area SSPLL.**

I. Introduction

HIGH-FREQUENCY PLLs are essential in creating carrier frequencies for data transmission and reception. In high-speed communication domains like satellite communication (SATCOM) [1], [2], the importance of low-jitter, low-power PLLs becomes more apparent. The need for more transmitters and receivers grows as beam-forming applications for space increase. RF transceivers for these applications require carrier frequencies, which results in a large silicon footprint occupied by multiple LC PLLs [3], [4] [5]. Also, enabling LO phase shifting necessitates the use of multiple PLLs. LC PLL consumes a large area due to the LC oscillator and the loop filter capacitor. Ring PLLs [6] occupy a small area, but the generation of high jitter creates a main blockage to use them in the transceivers where low jitter is essential.

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In frequency synthesizers, the loop filter is a significant barrier to full integration, especially when loop bandwidths are below 5 MHz. An optimal loop filter occupies a large amount of space in a high-performance PLL to achieve low-phase noise. Loop filters require low frequency zero to create low bandwidth PLL for low in-band jitter performance. Low-frequency zeros need either a large capacitor or a large resistor. But large resistor can add thermal noise and increases the reference spurs of the PLL. Thus, a large capacitor is preferred for low in-band noise performance resulting in an increased area. By combining a large resistor with a small capacitor, the authors in [7] were able to minimize the capacitor's surface area. In this case, using a feed-forward noise cancellation circuit, the resistor's thermal noise is suppressed. Since this is a ring oscillator-based implementation so this is not suitable for very low-jitter-high frequency applications.

Digital PLLs are considered an alternative solution to reduce the size replacing the loop filter, and the PFD/CP with their digital counterparts such as a digital loop filter and time-to-digital converter (TDC) [8]. However, the quantization noise of the TDC and digital control oscillator (DCO) put a fundamental limitation on the phase noise performance [9]. Another alternative solution to reduce area could be the use of type 1 PLLs [10], [11] [12]. The type I PLL with low bandwidth is essential for high-frequency LC PLLs to limit the reference signal noise. The finite static phase error and its dependencies on the input frequency also prove undesirable, also the type I PLLs have a limited acquisition range. So, when the VCO frequency and the input frequency are significantly different during startup, there is a possibility that the loop may fail to achieve lock.

Sub-sampling PLL (SSPLL), which has a lower in-band phase noise (PN) than its frequency-divider-based PLL competitors, has grown in popularity for frequency synthesis [13]. In an SSPLL, the charge pump noise is not multiplied by N^2(where N is the dividing ratio of the SSPLL), resulting in low in-band phase noise, making the SSPLL a suitable choice for high-frequency applications compared to a charge pump PLL. The SSPLL uses a sub-sampling phase detector (SSPD) instead of a conventional phase frequency detector/charge pump (PFD/CP) to sense the phase difference between the reference signal and the VCO output. The SSPD has a higher gain compared to the conventional PFD/CP, but this also

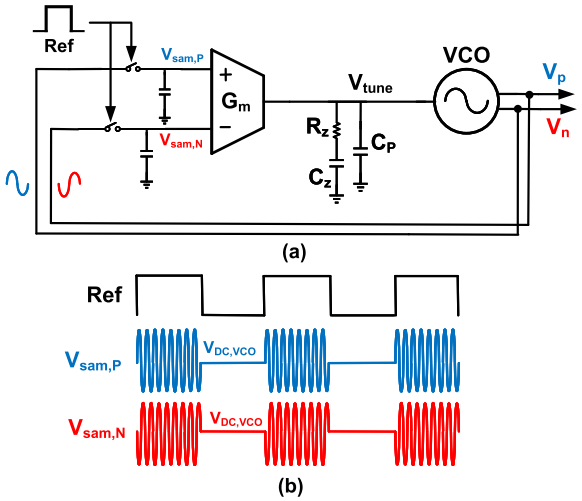


Fig. 1. (a) Sub-sampling PLL. (b) The behavior of V_{sam} at locking condition.

requires the use of a larger capacitor to achieve a low-frequency zero. When a transceiver has multiple frequency synthesizers [4], [5] to cover wide frequency bands, reducing the loop filter capacitor area can significantly decrease the overall area and thus the cost of transceivers.

Moreover, a voltage-controlled oscillator (VCO) contributes out-of-band noise to the SSPLL. Hence, maintaining good phase noise performance in the VCO is a key challenge in high-quality signal generation. The out-of-band noise of the SSPLL is determined by the VCO phase noise, which also significantly contributes to the overall phase noise performance of the PLL. To address these issues of SSPLLs, we propose two innovative techniques which are the key contributions:

1) To reduce the loop filter capacitor area, the conventional capacitor is replaced by a capacitor multiplier circuit which multiplies the value of capacitance thus requiring low capacitance and lesser area.
2) We propose an active capacitor multiplier-based VCO (AC VCO) that boosts the Q of the LC tank by enhancing the effective quality factor of the capacitor thus reducing the phase noise.

This paper is organized as follows. Section II includes SSPLL characteristics, mm-wave signal generation methods, and a comparison with charge-pump PLL. Section III presents the reduced-size loop filter of SSPLL using the proposed capacitor multiplier. The complete active capacitor VCO is described in section IV. In section V, the other building blocks of the SSPLL are reported. The measurement results are discussed in section VI. Finally, conclusions and acknowledgments are in sections VII and VIII, respectively.

II. Comparative Analysis of Sub-Sampling PLL and Charge-Pump PLL in Loop Filter Design

Conventional charge-pump PLLs, which use phase-frequency detectors (PFD) and charge pumps (CP), have been extensively employed in communication systems. However, the non-idealities of the CP lead to the generation of unwanted spurs in the PLL, resulting in a deterioration of the PLL output spectral purity. Moreover, the PFD/CP noise power is multiplied by N^2 at the PLL output, which further degrades the phase noise of the PLL, especially for large dividing ratios N. In contrast, Integer-N sub-sampling PLLs offer exceptional performance in terms of integrated phase noise (or jitter) and figure-of-merit (FoM). This superior performance is achieved since the charge pump noise is not multiplied by N^2. However, this phase noise performance is achieved by using the larger loop filter capacitor in SSPLL. This section presents a detailed comparison between the size of the capacitor (C_Z) of the SSPLL and CPPLL.

In general, sub-sampling PLLs in Fig. 1(a) consist of SSPD/CP, loop filter, and VCO. A low-frequency reference clock samples the high-frequency VCO output V_p and V_n of amplitude A_{VCO} and DC voltage $V_{DC,VCO}$. At the PLL locking condition, when the VCO and Ref signal phases are matched and their frequency ratio N is an integer number, the sampled voltage V_{sam} has a constant value equal to the DC voltage of the VCO ($V_{DC,VCO}$), as shown in Fig. 1(b). When the SSPLL is not at locking condition, V_{sam} will not be the same as the DC voltage of the VCO outputs. The same amount of phase difference $\Delta\phi$ between the input reference and VCO signal is converted to the differential voltage ΔV_{sam}. A current is generated by the transconductance g_m circuit in proportion to the input voltage ΔV_{sam}. The current generated by the g_m circuit is converted to a voltage by the loop filter, which consists of a resistor (R_z) in series of the capacitor (C_z) and capacitor C_p in parallel with R_z, C_p in series. This voltage generated by the loop filter controls the VCO output signal. Due to its sinusoidal nature, SSPD has a limited locking range [13], [14], and SSPLL can be locked to any harmonics of the reference signal. As a consequence, the SSPLL requires an additional frequency-locked loop (FLL) to guarantee the PLL locking.

In the proposed SSPLL, as shown in Fig. 2, the FLL consists of a divide by N and a PFD/CP with a dead zone (DZ) detector. Near the locking period the PFD/CP does not inject any current to the loop filter thus FLL charge-pump noise in not introduced into the output. For a given phase margin and VCO gain K_{vco}, the open loop bandwidth $f_{c,BW}$ can derived by the method in [13] as follows:

$$f_{c.BW} = \frac{\omega_c}{2\cdot\pi} \approx \frac{\beta_{\mathrm{CP}}\cdot R_z\cdot K_{\mathrm{VCO}}}{2\pi} \tag{1}$$

$$f_z = \frac{1}{2\cdot\pi\cdot R_z\cdot C_z} \tag{2}$$

where f_z is the frequency of the zero of the SSPLL. From Eqn. 1 and Eqn. 2 we get C_z

$$C_Z = \{(\frac{K_{vco}}{4\cdot\pi^2})\cdot(\frac{f_{c,BW}}{f_{zero}})\}\cdot\frac{\beta_{cp}}{f_{c,BW}^2} \tag{3}$$

A VCO analog tuning range is determined by K_{vco}, while a phase margin is determined by $f_{c,BW}/f_{zero}$ in (3) is constant once they specified. Thus the value of C_z is proportional to the ratio of β_{CP} and $f_{c,BW}$.

$$C_Z \propto \frac{\beta_{cp}}{f_{c,BW}^2} \tag{4}$$

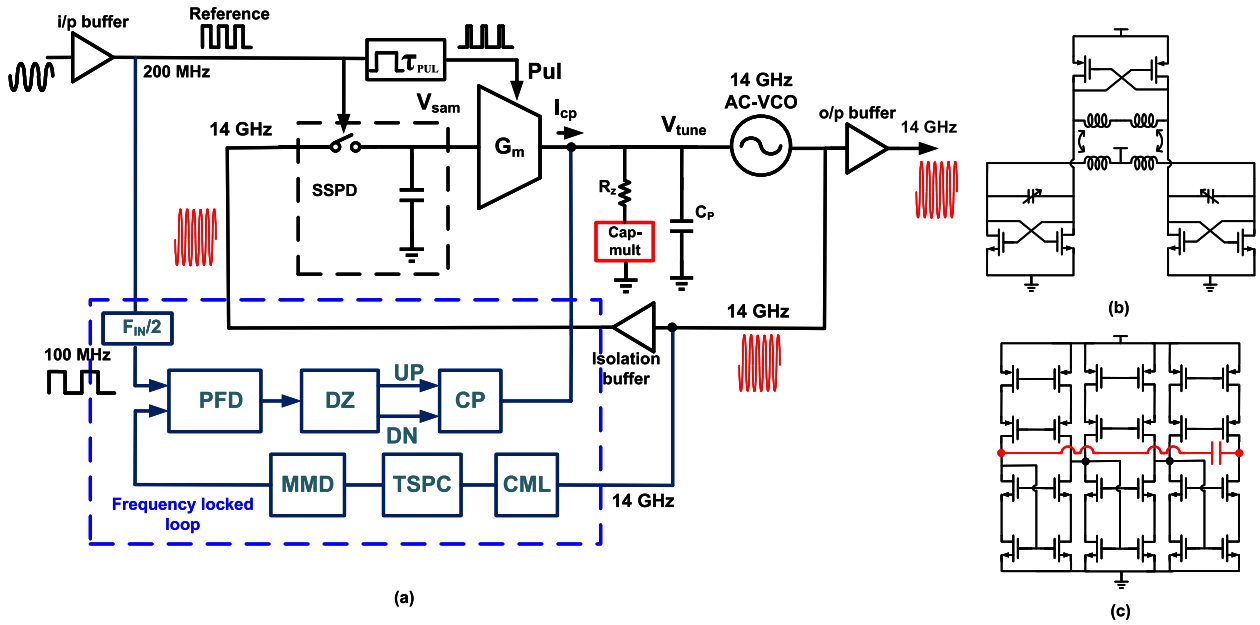


Fig. 2. (a) Proposed sub-sampling PLL. (b) Active capacitor VCO. (c) 3-stage capacitor multiplier.

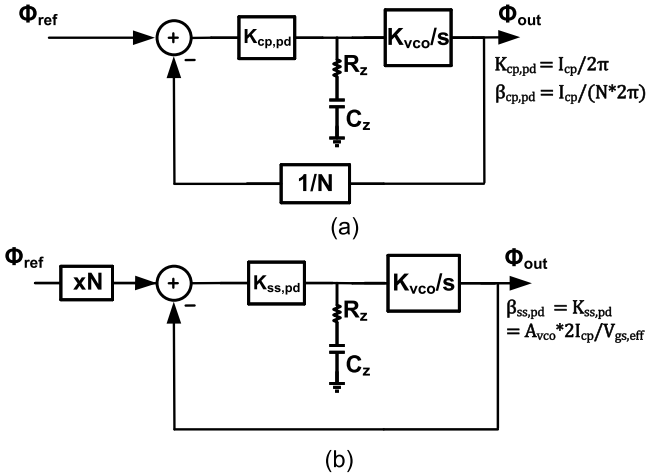


Fig. 3. Comparison between sub-sampling PLL (SSPLL) and conventional charge pump PLL (CPPLL) (a) CPPLL. (b) SSPLL.

from Fig. 3, we can get the ratio of CP feedback gain between the SSPLL and CPPLL

$$\frac{\beta_{SS,PD}}{\beta_{CP,PFD}} = 4 \cdot \pi \cdot N \cdot \frac{A_{vco}}{V_{gs,eff}} \tag{5}$$

For the same optimum bandwidth $f_{c,BW}$, K_{vco}, f_{zero} of SSPLL, and CPPLL from equation (4) we get the ratio, C_R between capacitors C_z of SSPLL and CPPLL

$$C_R = C_{Z,SSPLL}/C_{Z,CPPLL} = \frac{\beta_{SS,PD}}{\beta_{CP,PFD}} = 4 \cdot \pi \cdot N \cdot \frac{A_{vco}}{V_{gs,eff}} \tag{6}$$

where $\beta_{SS,PD}$ is the gain of the SSPD/CP and $\beta_{CP,PFD}$ is the gain of tri-state CPPFD/CP. $V_{gs,eff}$ is the effective gate-source voltage of the MOS transistor, A_{vco} is the amplitude of VCO output, and N is the frequency dividing ratio. For a 4 GHz SSPLL with 40 MHz reference frequency N = 100, for 65 nm process $V_{gs,eff}$ = 0.2 V, and A_{vco} = 0.4 V this capacitor ratio, C_R becomes = 2512. So, in comparison to CPPLL, the SSPLL with the same loop bandwidth ($f_{c,BW}$), K_{vco} parameters, the capacitor C_z will be much larger.

In SSPLL, this huge capacitor is compensated by adding a pulser which enables the SSCP for a particular smaller period of time reducing the gain of SSPD/CP. Even if this reduces the gain of SSPD/CP, a large capacitor is still required due to the absence of the dividing ratio in the SSPD/CP gain. The capacitor area can be further reduced by increasing the resistor size to keep the location of the zero in the same place, but a higher value resistor will add more thermal noise to the loop, as discussed earlier. To solve this problem of large occupancy, in this proposed SSPLL we have used a capacitor multiplier in the loop filter capacitor. Although the capacitor multiplier has been existing for several years [15], [16], its potential of achieving very low in-band phase noise in sub-sampling PLL is not fully appreciated to the best of the author's knowledge.

In addition, a VCO introduces out-of-band noise into an SSPLL, which significantly increases jitter. By lowering the SSPLL's BW and VCO phase noise, the jitter can be reduced. Increasing the Q factor of the LC tank is necessary to lower the phase noise of the VCO, but this is challenging because the Q-factor of the capacitor declines as the frequency rises. By raising the capacitors' quality factor, the proposed active capacitor also lowers the VCO's phase noise. In this proposed SSPLL, we have implemented the capacitor multiplier and AC VCO to reduce the area and jitter respectively.

III. Compact Loop Filter Based On The Proposed Capacitor Multiplier

In SSPLL, the loop filter converts the current generated by the g_m/CP circuit to a control voltage of the VCO. As the VCO inherently provides a pole at the origin, the order of SSPLL is always one order higher than the one of loop filter. To maintain stability, a zero needs to be added for the SSPLL loop, and this is achieved by adding a capacitor C_z and a resistor R_z to the

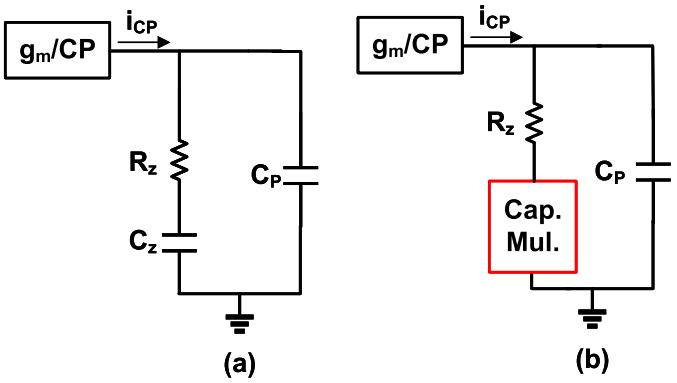


Fig. 4. (a) Loop filter of SSPLL. (b) Loop filter using a capacitor multiplier.

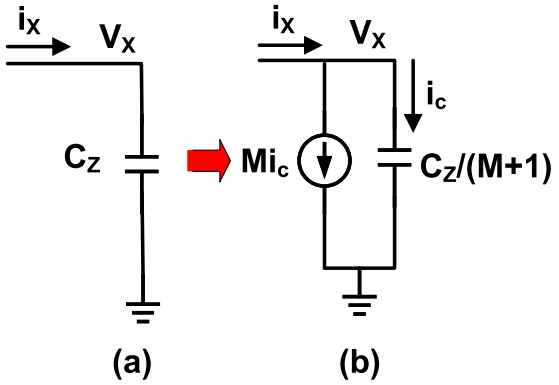


Fig. 5. (a) Passive capacitor (b) Working principle of the proposed capacitor multiplier.

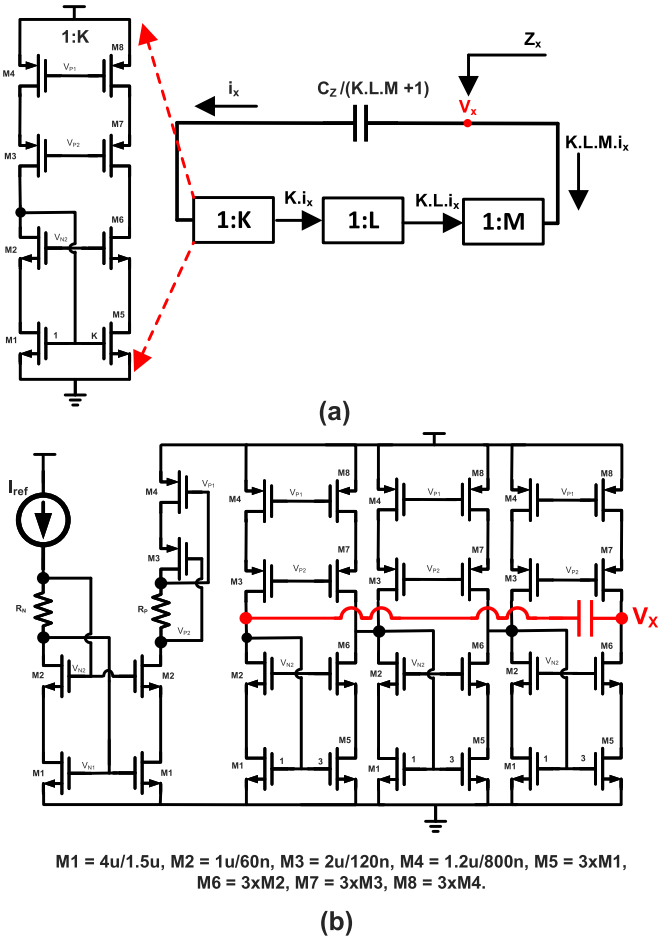


Fig. 6. (a) The conceptual diagram of 3-stage capacitor multiplier. (b) Schematic of the 3-stage current mirror for the proposed capacitor multiplier.

loop filter. C_z produces the second pole at the origin, which can make the SSPLL unstable when combined with the pole from the VCO. The addition of R_z and C_z generates a zero that ensures loop stability. To further smooth control voltage ripples, a capacitor C_p is added, which generates the third pole in the SSPLL after the unity gain bandwidth.

Generally, a small R_z value has been used, keeping C_z larger to decrease thermal noise at the cost of the larger area due to C_z. In this SSPLL, for a reference frequency of 200 MHz, optimized bandwidth of $\approx$ 1 MHz is chosen where the reference and VCO noise match. Due to the high gain of the SSPD/CP, SSPLL inherently requires a large capacitor C_z compared to the conventional PFD/CP-based PLL as discussed in section II. To achieve the required bandwidth, $R_z = 3.5$ kΩ and $C_z = 150$ pF are chosen.

In Fig. 4(a) putting C_z of 150 pF directly in the loop filter would increase the area of the SSPLL significantly. To address this area issue, we implemented a capacitor multiplier inspired by prior works [15] and [17], operating in the MHz order frequency to reduce the required area while ensuring stability. While [15] implemented a capacitor multiplier circuit for analog filters, it did not provide noise analysis and optimization for noise and power perspectives. In Fig. 4(b), the capacitor multiplier has multiplication factors of 28, reducing the chip size of the capacitor C_z from 150 pF to 5.35 pF. In a conventional 65 nm CMOS technology, 150 pF MIM capacitor occupies around 0.08 mm^2. The capacitor multiplier along with the active circuit only consumes 0.0026 mm^2. Active circuits involved in implementing the capacitor multiplier contribute to the overall noise as this noise is band-pass filtered to the output. The MOSFET sizes have been chosen so that MOSFETs' noises do not impact the overall phase noise performance. The detailed operating principle of the capacitor multiplier is shown below.

A. Operating Principle of Capacitor Multiplier

As shown in Fig. 5(a), the current flowing from node V_X through the physical capacitor C_z is i_x. Looking-in impedance equals $V_X/i_x = 1/s{\cdot}C_z$. In Fig. 5(b), i_x splits into i_c, which passes through capacitor $C_z/(M+1)$ and mirror current of the capacitor with multiplication factor M, i.e., $M{\cdot}i_c$. Total current coming out of V_x i.e. $i_x = (M+1){\cdot}i_c$, where $i_c = V_x \cdot s{\cdot}\, C_z/(M+1)$. Therefore, looking-in impedance at node Z_x equals $V_x/i_x = V_x/((M+1).i_c) = 1/s{\cdot}C_z$ same in Fig. 5(a). This is the operating principle of the capacitor multiplier where C_z/(M+1) effectively shows the impedance which is equal to the impedance of the physical capacitor of C_z.

B. Implementation of a Stable Capacitor Multiplier With More Than 25 Multiplication Factor

Due to the mismatch issue, we have chosen to maintain the current mirror ratio below 10. To have a higher capacitor

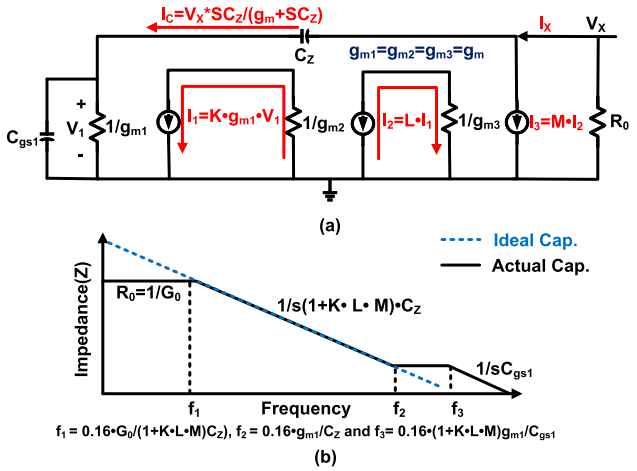


Fig. 7. (a) Small signal model of the capacitor multiplier (b) Impedance looking into capacitor multiplier circuit.

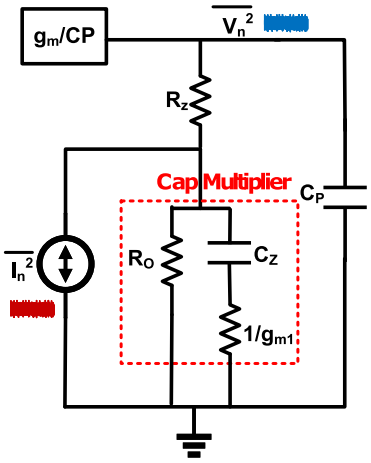


Fig. 8. Calculation of noise generated by the capacitor multiplier.

multiplication factor, the cascaded current mirror stages need to be implemented. In Fig. 5, three stages of the current mirror are added with current gains of K, L, and M for the first, second, and third stages, respectively. This results in a total current multiplication of $(K \cdot L \cdot M + 1)$. Total current coming out of node V_x is $(K \cdot L \cdot M + 1) \cdot i_x$ resulting in looking-in impedance $(Z_x) = 1/s \cdot C_z$ using capacitance of $C_z/(K \cdot L \cdot M + 1)$. The impedance looking at V_X, i.e. (Z_x) is as shown in Fig. 7. In DC and low frequencies below f_1, the impedance will no longer be $1/s \cdot C_z$. Instead, it will be a flat resistance R_o, which is the impedance of the last current stage. In low frequency, this fixed impedance R_o causes current leakage issues in overall SSPLL. Thus, cascode current stages have been used to have higher R_o causing fewer leakage currents in the SSPLL loop filter.

The capacitor multiplier operates properly only in the mid-frequency range from f_1 to f_2, where the impedance matches with the one of the ideal C_z. A zero is introduced at f_2 by a series capacitor with the impedance created by diode transistor M_1, i.e., $1/g_{m1}$. Beyond f_2, impedance is flat with $1/g_{m1}$. At high frequencies above f_3, impedance is decreased with the slope of -20 dB/decade where the impedance is $1/s \cdot C_z$.

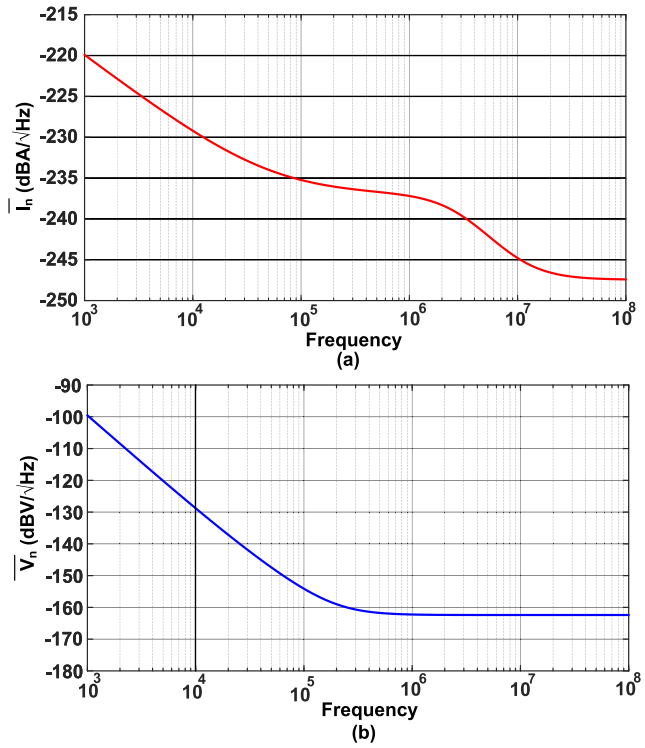


Fig. 9. (a) Capacitor multiplier current noise. (b) Corresponding voltage noise of the loop filter.

C. Design Challenges in The Proposed Capacitor Multiplier

It needs to be ensured that the impedance of this capacitor multiplier circuit does not get flat until the unity gain bandwidth of SSPLL. This can be achieved by maximizing the value of g_{m1} as zero at f_2 depending on g_{m1}. In order to have a high value of g_{m1}, it is necessary to ensure a high (W/L) ratio for transistor M_1 as shown in Fig. 6. On the other hand, to obtain a high output resistance (R_o) in the order of mega-ohm, the length of M_1 has to be higher. Thus the width of the transistor M_1 must be scaled accordingly to have the same W/L ratio. A higher area $(W \cdot L)$ of M_1 will have less flicker noise at the cost of large parasitic. The presence of parasitic can significantly diminish the operating range of the capacitor multiplier and have a detrimental effect on overall loop stability. Therefore, it is imperative to optimize the size of the transistor M_1 to mitigate these issues. Thus, the W/L ratio of 4μm/1.5μm has been chosen for M_1. Additionally, it is crucial to optimize the overall multiplication factor, as the noise current due to transistor M_1 is multiplied by the multiplication factor $K \cdot L \cdot M$ and affects overall phase noise at the output. In Fig. 8, $\overline{I_n}$ represents the current noise generated by the capacitor multiplier and $\overline{V_n}$ is the total voltage noise at the input of the active capacitor-based VCO, which is due to the capacitor multiplier $(\overline{V_{n,cm}})$ and thermal noise of R_z.

$\overline{V_n}$ is primarily dominated by the current noise $(\overline{I_n})$ generated through the impedance of the last stage of the capacitor multiplier, R_o, as shown in Fig. 9. Thus, with high impedance, though we get rid of the current leakage issue, the noise power is higher at low frequencies, as expressed in

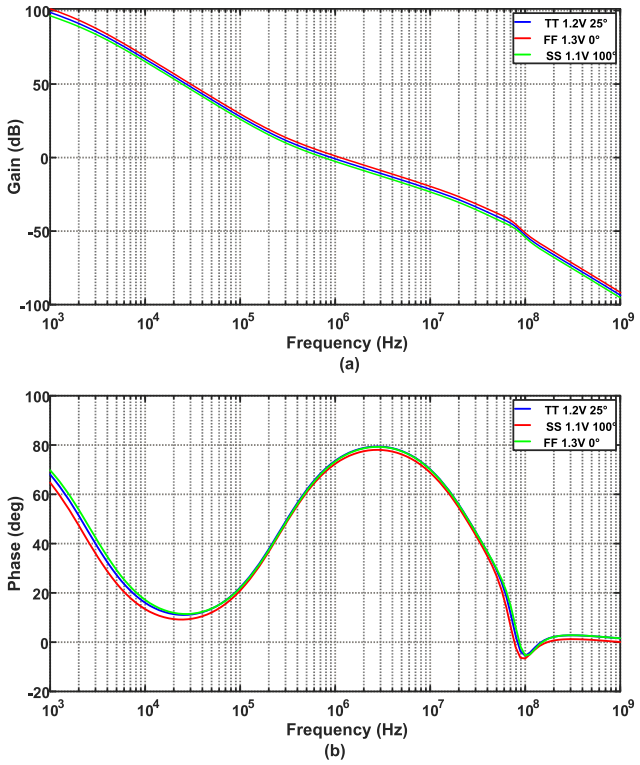


Fig. 10. (a) Simulated open loop gain (b) Phase of the SSPLL across different process corners.

Eqn. 7. This loop filter noise is further band-pass filtered by the SSPLL so this does not affect the in-band noise.

$$\frac{\overline{V_{n,cm}}}{\overline{I_n}} = \frac{R_o||(1/sC_z + 1/g_{m1})}{R_z + 1/sC_p + (R_o||(1/sC_z + 1/g_{m1}))} \cdot \frac{1}{sC_p} = \frac{R_o(g_{m1} + sC_z)}{s^2 C_P C_z R_z R_o + s(C_p R_o + C_z R_o + C_p R_Z) + 1} \tag{7}$$

In this proposed capacitor multiplier, we have chosen the multiplication ratio is 28. To achieve this ratio, 3 combinations of multiplication factors for capacitor multiplier stages were possible i.e. K, L, and M of 1, 3, and 9 or 9, 3 and 1 or 3, 3, and 3. The first one causes more current leakage issues due to higher current flow in the last stage of the capacitor multiplier, whereas the second case causes maximum noise voltage at the output due to multiplications of high R_o, as shown in Eqn. 7. Thus, to reduce the noise contribution and current leakage through R_o of the capacitor multiplier, we have chosen the third combination of multiplication factors as 3,3,3. To ensure the functionality of the capacitor multiplier, stability simulation has been done for a typical corner i.e. TT, 1.2V, 25° along with two worst PVT corners i.e. SS, 1.1V, 100°, and FF, 1.3V, 0°. Results show that the phase margin using the loop filter with the proposed capacitor multiplier stays more than 65° across PVT, as shown in Fig. 10, and the impedance of the loop filter is shown in Fig. 11 across all PVT corners.

IV. Low Phase Noise Active Capacitor VCO

Low-phase noise and low-power VCO is a key sub-block to implementing SSPLL for future communication systems.

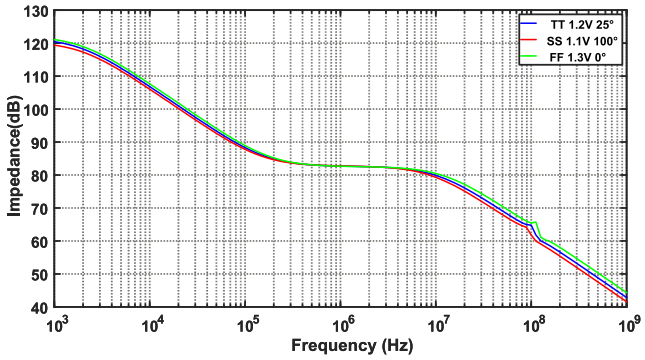


Fig. 11. Simulated impedance plot of the loop filter.

However, achieving these specifications can be challenging due to the trade-off relationship between a wide tuning range and low-phase noise performance.

The oscillation frequency of an LC oscillator is determined by $1/(2\pi\sqrt{L_{tank}C_{tank}})$ and the values of the inductance and capacitance in the resonant tank circuit. In a voltage-controlled oscillator (VCO), the total capacitance across the resonant tank, $C_{tank} = C_B + C_{var} + C_{par}$, is made up of several components: the capacitance from a switched capacitor bank (C_B), a variable capacitor (C_{var}), and parasitic capacitance (C_{par}). The phase noise of the oscillator is influenced by the loaded Q of the resonator at the resonant frequency, as described by Leeson's equation [18].

The loaded Q of an LC resonator is typically influenced by the quality factors of both the inductors (Q_L) and the capacitor (Q_C). In other words, the reciprocal of the loaded Q is proportional to the sum of the reciprocals of (Q_L) and (Q_C) (i.e., $\frac{1}{Q} \propto \frac{1}{Q_L} + \frac{1}{Q_C}$). In the past, researchers [19], [20] have tried to improve the phase noise performance of VCO by boosting the Q of the resonator, with a focus on increasing the Q of the inductors. However, at millimeter-wave frequencies, the quality factor of the switched capacitor bank and the varactor tend to dominate the quality factor of the resonant tank, so only enhancing the Q of the inductors may have a limited impact on the overall loaded Q of the resonator. To address the limited impact on overall Q when only improving inductor Q at millimeter-wave frequencies, we propose using a tuned transformer-based active impedance converter to increase the quality factor of the capacitive component of the resonator. By incorporating this impedance conversion circuit with a current-reuse core, we are able to design a low-power, low-phase noise, compact VCO operating at 14 GHz.

A. Proposed Impedance Converter

This work uses a transformer-based Q-enhanced VCO for low-phase noise performance while consuming low DC power. In [21], two separate inductors were used to implement the VCO with an active capacitor. In [22] and this work, a transformer is used instead to reduce the area while keeping the same performance. To achieve a wider tuning range, the value of M_{boost} varies from 0.85 to 1.65 for a large capacitance tuning ratio of 7.8 in [21]. As a result, the loaded quality

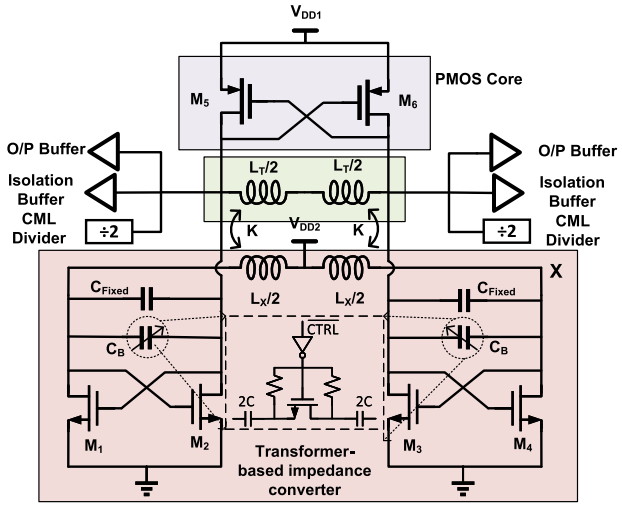


Fig. 12. Schematic of the proposed 14GHz Active Capacitor VCO.

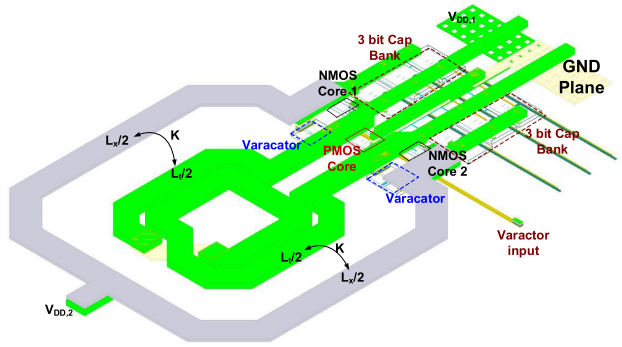


Fig. 13. 3D view of the Active Capacitor VCO.

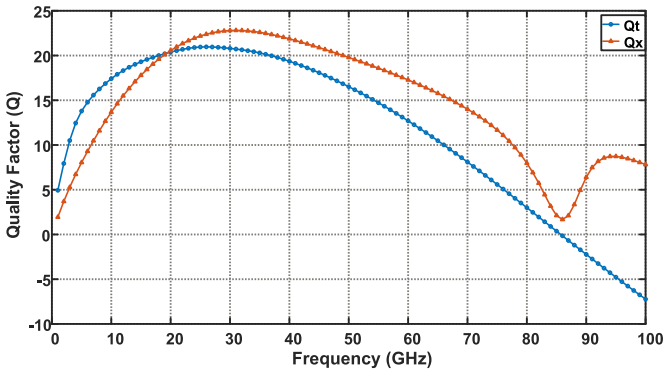


Fig. 14. Simulated quality factor (Q) of the primary and secondary inductors of the transformer vs. frequency.

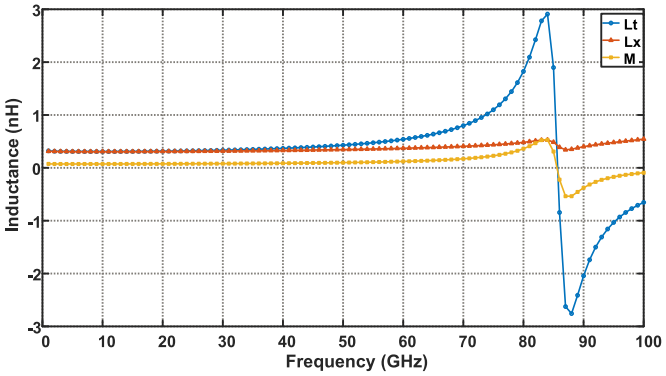


Fig. 15. Simulated inductance (L) of the primary and secondary inductors of the transformer vs. frequency.

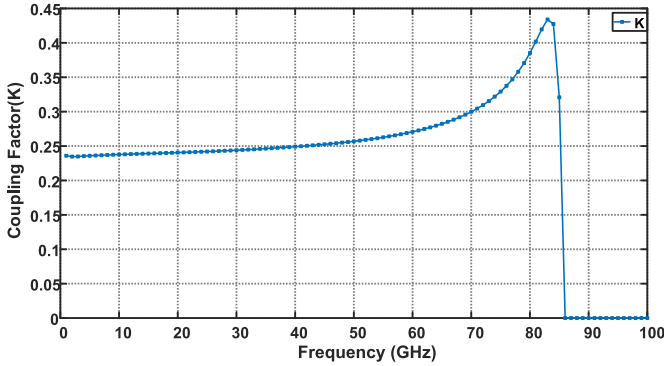


Fig. 16. Simulated coupling (K) of the primary and secondary inductors of the transformer vs. frequency.

factor is decreased for part of the tuning range. In this work, the VCO is operated in the region where the multiplication factor is greater than one, resulting in superior phase noise performance. In the resonator tank, a fixed capacitor (C_{Fixed}) is used in parallel with a switched capacitor bank and a small varactor cell (together denoted as C_B). The schematic of the proposed VCO based on the transformer-based impedance converter is shown in Fig. 12. The pair of NMOS cores, together with the inductor L_x and the capacitor bank (with varactor) C_B, forms an active impedance converter. The multiplication factor of the quality factor and total capacitance of the capacitor bank with varactor can be derived from Fig. 12 as follows

$$M_{boost} = 1 + \frac{L_X \cdot (1 - K^2) \cdot {G_m}^2 \cdot (\frac{\omega^2}{\omega_m^2} - 1)}{C_B \cdot (1 - \frac{\omega^2}{\omega_X^2})} \quad (8)$$

where $\omega_m = \frac{G_m}{C_B + C_P'}$, $G_m = g_m - g_B$, $\omega_X = \frac{1}{\sqrt{L_X(1-K^2)C_X}}$, $C_X = C_B + C_{Fixed} + C_{PX}$. C_{PX} is the parasitic capacitance at node X (shown in Fig. 12), g_m is the transconductance of the NMOS devices, K is the coupling factor of the transformer, and g_B is the loss of the capacitor C_B. Here, ω_X is the resonance frequency at node X, which is designed such that $\omega_X > \omega_o$, where ω_o is the oscillation frequency of the VCO output. The impedance looking into node X behaves inductively at the desired output frequency (ω_0). The cross-coupled MOSFET pair transform the inductive load to a positive capacitance and a negative gm in the frequency of operation.

The impedance converter circuit provides a positive capacitance and negative transconductance at ω_o; a resonator is formed by placing an inductor (L_T) in parallel to the output node of the impedance converter. Instead of two separate inductors, the tank inductor is placed in proximity of the other inductor (L_X) to save area. The simulated coupling coefficient of the two inductors is 0.2, which provides the optimum quality factor of the resonator and the best phase noise performance. The final oscillation frequency of the VCO

can be derived as

$$\omega_o = \frac{1}{\sqrt{L_T(C'_B + C_{load})(\frac{L_X}{L_T} + 1 - \frac{\omega_m^2}{\omega_X^2})}} \quad (9)$$

Here, C'_B is the boosted capacitor that is seen from the output of the impedance converter circuit, and C_{load} is the loading capacitance of the VCO output. In this implementation, the VCO drives the output buffer, the isolation buffer, and the CML divider. The component values L_X, L_T, k, and C_B are chosen such that the multiplication factor $M_{boost} > 1$ around the desired oscillation frequency of 14 GHz.

B. Design of The Transformer for Improved Phase-Noise Performance

To implement the VCO with the transformer-based impedance converter, the secondary inductor of the transformer is used as the tank of the resonator. The L_X and L_T inductors are chosen to be 315 pH and 310 pH, respectively. The coupling factor between the two inductors is $k = 0.25$. The individual quality factors of L_X and L_T are $Q_X = 18$ and $Q_T = 20$, respectively. The tank inductor has more impact on the overall loaded quality factor of the resonator; hence, it is laid out in the technology's ultra-thick metal (M9). To achieve the inductance value, a two-turn inductor is designed. A 3D layout view of the transformer with other components of the VCO is shown in Fig. 13.

C. Active Capacitor VCO Implementation

A three-bit binary weighted switched capacitor bank is designed in parallel with a small varactor for continuous tuning for the capacitor implementation. The capacitance value (with varactor) ranges from 260 fF to 340 fF without the impedance converter. To improve the overall quality factor of the capacitor, a fixed MOM capacitor of 80 fF with a high-quality factor is placed in parallel with the resonator. After the impedance converter, the capacitance varies from 350 fF to 470 fF. The impedance converter provides a multiplication factor M_{boost} of 1.30 to 1.40 across the tuning range for both the capacitance and the quality factor. A current reuse PMOS core is used for complimentary VCO operation with improved DC-to-RF efficiency. The two supply voltages of the VCO are $V_{DD1} = 1$ V, and $V_{DD2} = 0.5$ V. The core area consumption of the VCO is 0.05 mm^2 (200 μm X 250 μm).

V. Other Building Blocks of SSPLL

A current-mode logic (CML)-based divide-by-2 divider (DIV2s) is implemented to divide the frequency by two and is used as the prescaler to operate up to 14.8 GHz. The CML consumes high current from the supply. To lower the power consumption of the overall SSPLL, True-single-phase-clock (TSPC) divider has been used, followed by the multi-mode divider (MMD) to further divide input frequency to the 100 MHz range. The differential to single-ended converter (D2S) has been used after CML to convert the differential signal to single-ended followed by the TSPC. The MMD divider, based on the architecture on [23], can change the division ratio by external control bits. The divider chain DZ and PFD keep operating even after the PLL is locked so that the PLL can automatically relock when it loses locking due to unexpected interference. The simulated transient locking behavior and phase noise are shown in Fig. 18 and Fig. 17, respectively. The g_m circuit, DZ detector in the SSPLL, is used based on [13]. The sampling capacitor value of SSPD is kept at 40 fF, which is large enough to hold the charge of the V_{sam}.

The Pul signal implemented using delay cells and two MUX gates as shown in Fig. 19 illustrates the timing of the signals controlled by the input control bits. The individual delay cell is realized with a series of inverters with a minimum delay of 25 ps. The width of the Pul signal is determined by the delay of the cell, which has a minimum value of 75 ps. By controlling the input MUX bits (S_0, S_1, S_2, S_3), the delays can vary from 75 ps to 350 ps with a resolution of 25 ps due to an inverter delay. Since the open loop gain of the sub-sampling

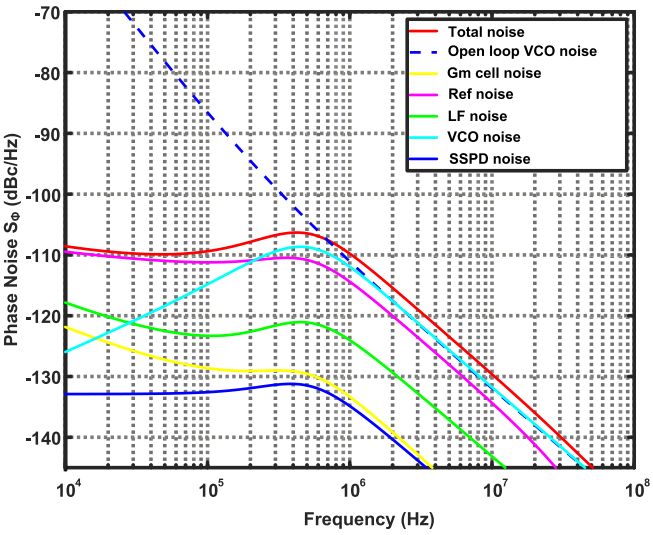


Fig. 17. Simulated SSPLL phase noise.

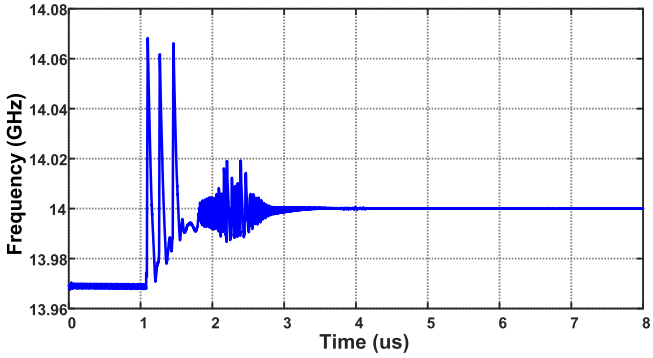


Fig. 18. Simulated locking behavior of the SSPLL.

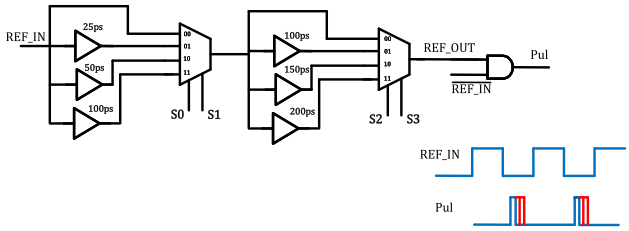


Fig. 19. Pulse generator circuit.

TABLE I
COMPARISON WITH STATE-OF-THE ART PLLS

	This Work	[25] JSSC'22	[26]JSSC'20	[27] TCAS1'19	[6]JSSC'22	[28] ISSCC'21
Tech. (nm)	**65**	65	7	65	65	16
Type	**LC AC VCO SSPLL**	LC SSPLL	LC BBPLL	Injection Locked ADPLL	Ring VCO PLL	Digital SPLL
Supply voltage (V)	**1.2**	1.2	0.75/1.5	1.2/0.95	1.2	NA
Output frequency (GHz)	**13.2-14.8**	12.0-14.5	14	18-23	5.3	12.-16.6
F_{ref} (MHz)	**200**	50	350	1125-1437.5	100	245.76
Int. Jitter (fs)	**85.4** @ 14GHz(10k-100M)	83 @ 13.5GHz(1k-100M)	143 (1k-100M)	57.4 (1k-100M)	365 (10k-30M)	47.3 (10k-100M)
Ref. Spur (dBc)	**-65.72**	-75	NA	-42/-38.5	-77	-75.1
Power (mW)	**8.42**	7.7	40	13.7	9.27	56
FoM(dB)*	**-252.12**	-253	-240.9	-253.5	-239.1	-249.0
Active area (mm^2)	**0.0918**	0.23	0.06	0.462	0.146	0.5
FoMa (dB)**	**-262.48**	-259.38	-247.67	-256.85	-247.4	-252.01

* $FoM = 20\text{*}\log(Jitter/1s) + 10\text{*}\log(P_{dc}/1mW)$
** $FoM_a = FoM + 10\text{*}\log(Area/1mm^2)$

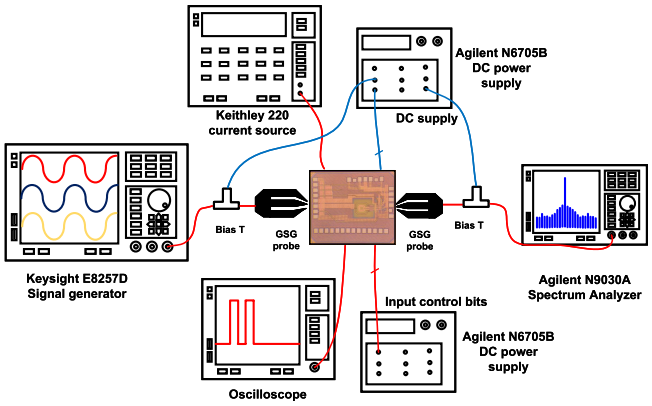
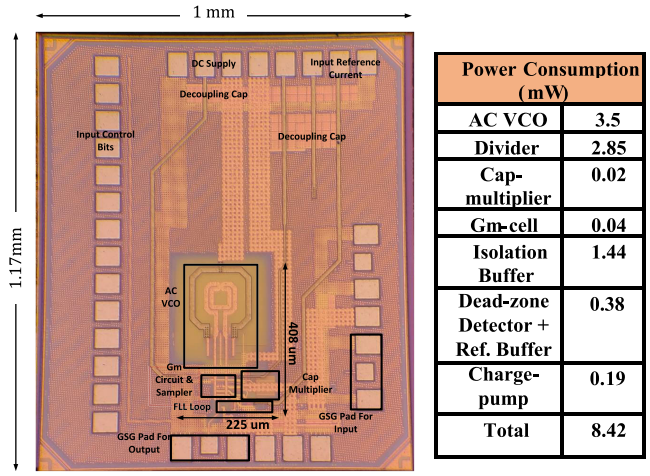


Fig. 20. Test Setup for the proposed SSPLL.



Power Consumption (mW)	
AC VCO	3.5
Divider	2.85
Cap-multiplier	0.02
Gm-cell	0.04
Isolation Buffer	1.44
Dead-zone Detector + Ref. Buffer	0.38
Charge-pump	0.19
Total	8.42

Fig. 21. Chip photograph and power breakdown table.

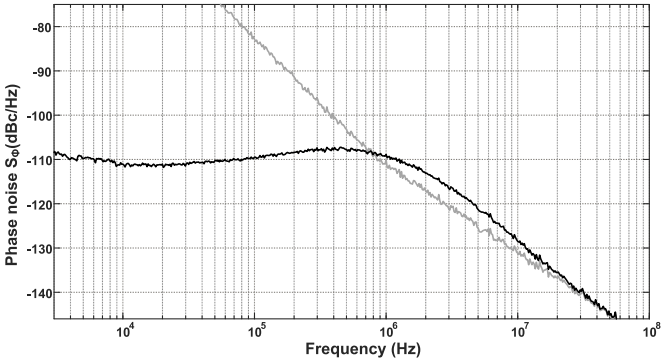


Fig. 22. Measured phase noise at 14 GHz output.

PLL is proportional to τ_{pul} [24], it is possible to change the SSPLL loop bandwidth by tuning the width of the Pul signal. This bandwidth tuning is done without affecting the operation point of the rest of the other circuits. During the measurement, the control bits are given externally as shown in measurement setup Fig. 20.

VI. MEASUREMENT RESULTS

The SSPLL was implemented in a 65 nm CMOS process. It occupies an active area of 0.0918 mm^2, as the chip photograph shown in Fig. 21. The supply voltage of the whole chip by Agilent N6705B DC power supply is 1.2 V, and the power consumption at 14 GHz, excluding the output buffer for testing purposes, is 8.42 mW, as the power consumption breakdown shown in Fig. 21. An Agilent analog signal generator E8257D was used as the reference source. The reference frequency is 200 MHz; by adjusting the division ratio of MMD from 33 to 37, the SSPLL can cover the output frequency range from 13.2 to 14.8 GHz with a 200 MHz output frequency resolution. Fig. 22 and Fig. 23 shows the measured phase noise and frequency spectrum at 14 GHz. With a power consumption of 3.5 mW, the proposed active capacitor VCO has a phase noise of -110.2 dBc/Hz at an offset of 1 MHz from the carrier corresponding to a FoM$_{VCO}$ of -187.68 dB.

As shown in Fig. 20, Keithley 220 current source is used to bias the capacitor multiplier. The output open drain buffer is biased through a bias-T with Agilent N6705B power supply. Measurements have been taken by varying the current to measure the noise contributed by the capacitor multiplier to the in-band noise. The measured root-mean-square (RMS) jitter integrated from 10 kHz to 100 MHz is 85.4 fs, and the reference spur is -65.72 dBc at the 14 GHz output. At 14.8 GHz, the measured root-mean-square (RMS) jitter integrated from 10 kHz to 100 MHz is 104.5 fs, and the reference spur is -64.39 dBc. The measured phase noise curve and integrated jitter match well with the calculated results shown in Fig. 22 and Fig. 23, respectively. Differences in

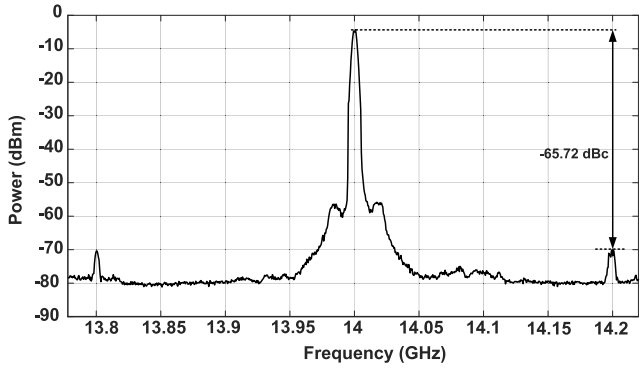


Fig. 23. Measured SSPLL output spectrum at 14 GHz.

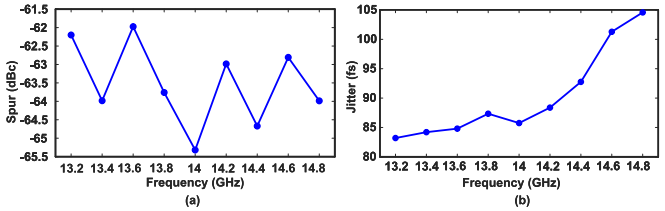


Fig. 24. Measured reference spur and integrated jitters from 13.2 to 14.8 GHz.

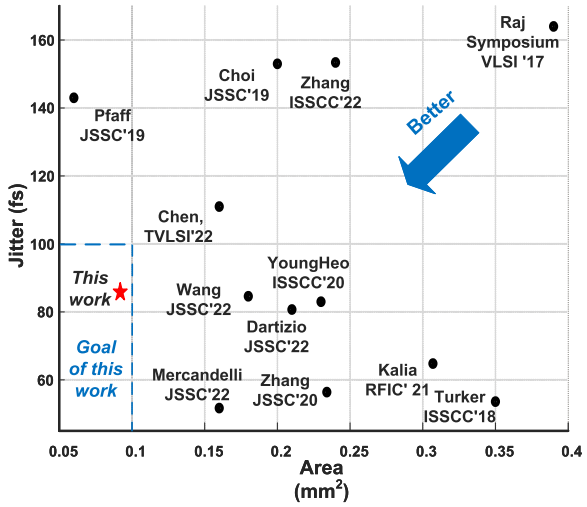


Fig. 25. Jitter and area comparison with other state-of-the-art PLLs.

measured and calculated results are mainly due to the limited accuracy of curve fitting phase noise contributed from the input clock and each building block and the difference between the simulated active capacitor VCO phase noise and the measured VCO phase noise.

Table I compares the measured performance of the proposed SSPLL with state-of-the-art. To the best of the author's knowledge, the proposed SSPLL has the lowest area and the lowest figure of merit based on the area (FOMa) among 14-24 GHz frequency synthesizers. In addition, the SSPLL also achieves a good jitter number which is suitable for mm-wave 5G applications. Fig. 25 compares the jitter of the proposed SSPLL with prior works of around 14 GHz range PLLs, showing that it is able to achieve sub-100 fs jitter while occupying an area of less than 1 mm^2. Fig. 24(a) and (b) show the measured integrated spur level and the jitter across the frequency range from 13.2 to 14.8 GHz with a resolution of 200 MHz, respectively.

VII. Conclusion

We have proposed an innovative sub-sampling phase-locked loop (SSPLL) architecture that uses an ultra-low-area capacitor multiplier to reduce the size of the SSPLL and a low-noise active capacitor-based VCO to reduce out-of-band phase noise of the SSPLL. This SSPLL can be used in high-frequency applications by adding frequency doublers or triplers, such as 5G beam-forming systems that require multiple PLLs for multi-frequency band coverage and LO distribution. The measurement results show that the SSPLL operates at a frequency range of 13.2-14.8 GHz with RMS jitter of 85.4 fs at 14 GHz, power consumption of 8.42 mW, FoM and FoMa of -252.12 dB and -262.48 dB, respectively. The SSPLL has a much smaller area than conventional SSPLLs due to the reduced capacitor area by a factor of 28 enabled by the proposed capacitor multiplier and low out-of-band phase noise resulting in lower jitter performance by the proposed VCO.

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