Highly Efficient Multiband Harmonic-Tuned GaN RF Synchronous Rectifier

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***Abstract*— This article presents a highly efficient GaN-based harmonic-tuned multiband RF rectifier for wireless power transfer (WPT) applications. The rectifier has been implemented by incorporating a microstrip coupler and a transmission line-based phase shifter to convert a power amplifier (PA) into a synchronous rectifier based on the time-reversal duality principle. The proposed rectifier provides a compact solution for wireless power charging systems while supporting dual-bands. The microstrip coupler is used to derive the gate driving signal for the device, which requires a weak coupling from the input RF signal. The coupler has been characterized separately for wideband operation from 1 to 3 GHz with only 0.3-dB insertion loss. Measurement results show that the rectifier has 77% and 75% efficiencies at 1.17 and 2.4 GHz, respectively, when the input RF power is 10 W. The rectifier shows >50% efficiency for input power levels down to 1.5 W. To the best of the authors' knowledge, this rectifier presents one of the highest RF-to-dc rectification efficiencies in dual-band operation for a watt-level RF input power.**

***Index Terms*— Class-F, inverse class-F, synchronous rectifier, wireless power transfer (WPT).**

I. Introduction

WIRELESS power transfer (WPT) refers to technology that allows a power source to transmit electrical power to the load without interconnecting cords. One of the popular applications of WPT is charging electronic appliances. Wireless charging is an emerging field, with a market value projection worth 15 billion by 2020 [2]. One of the essential parts of wireless charging systems is the ac-to-dc rectification circuit, which is the main focus of this work.

Since the early development of wireless energy harvesters has been presented [3], [4], [5], [6], several diode-based rectifiers have been proposed and demonstrated in the literature, with a comprehensive survey presented in [7]. Diode-based rectifiers are suitable for low-power applications such as remote sensors, the Internet of Things (IoT), and radio-frequency identification (RFID). Although the necessary power is often below 1 W, for some cases such as semiactive RFID sensors with rechargeable batteries (wireless charging), it needs more power [8], [9], [10], [11]. Diode-connected transistors available in standard CMOS technology are chosen as the rectifying element for most RFID applications. For solar-powered satellite (SPS) applications, the Schottky diodes are the predominant choice of rectification device for having low threshold voltage and lower junction capacitance compared to p-n junction diodes [12]. Apart from SPS applications, several others have been proposed that require higher RF power to be delivered wirelessly by directive RF beamforming. Remotely charging unmanned aerial vehicles (UAVs) [13], microwave-driven unmanned vehicles [14], [15], high-altitude electric motor-powered platforms (HAPPs) [16], [17], and stationary high-altitude relay platform (SHARP) [18], [19] are some of the applications in this area. Typically, an array of rectifying circuits is used to scale up the harvested power for these applications [20], [21], [22]. However, the integration of multiple rectifying circuits introduces higher loss and more complexity.

Another approach to designing highly efficient rectifiers handling high power emerges from converting high-efficiency power amplifiers (PAs) into rectifiers. According to the time-reversal duality theory introduced by Hamill [23], a PA can act as a rectifier by reversing the power flow. Using this theory, a class-E synchronous rectifier was presented in [24], and several other works have been demonstrated using different classes of PAs using highly efficient GaN HEMT devices to construct rectifiers such as class-AB [25], class-D [26], class-E [27], [28], [29], class-F [30], and inverse class-F [31], [32], [33], [34], [35]. A great deal of effort has been given to making PAs more efficient. Compared to

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diode-based rectifiers, PA-based rectifiers are generally more efficient and have higher power-handling capability, making them suitable for medium- to high-power WPT applications.

Demonstrations of synchronous rectifiers often use external samplers (or couplers) and phase shifters to generate the gate signal of the rectifier. Relatively few publications report on the design of an integrated gate feedback loop [31], [35]. Additionally, there has been an increasing demand for multiband circuits as the available spectrum gets crowded. Although there have been several dual-band, diode-based rectifiers proposed [36], [37], [38], [39], their efficiencies are limited to <70% in both bands, which are lower than the single-band PA-based rectifiers that exceed 80% quite often. The next generation of wireless charging systems requires a multiband, fully integrated, high-power (∼10 W), high-efficiency (>75%) RF synchronous rectifier.

In this work, we present a detailed circuit analysis and characterization of our previously reported work [1]. This article presents a compact harmonic-tuned dual-band load network, which simultaneously satisfies inverse class-F and class-F load characteristics in the L- and S-bands. The purpose of choosing these frequency bands is to demonstrate the design procedure of the dual-band harmonic-tuned network with more than one-octave frequency separation. For example, a prototype is designed that shows peak conversion efficiencies centered at 1.17 and 2.4 GHz. The salient features of this work are summarized below.

1) Mathematical analysis and design equations of the dual-band harmonic tuned matching network for the synchronous rectifier are presented.
2) The design procedure and considerations for the onboard integrated coupler and phase shifter are outlined.
3) Detailed experimental results and characterization of the dual-band PA, the wideband coupler, and the synchronous rectifier are presented.
4) The effects of load impedance and gate bias voltage on rectification efficiency are explored and outlined in detail.

This article is organized as follows. Section II provides a brief theoretical background for converting the PA into a synchronous rectifier. Section III presents the detailed design procedure of the circuit, and Section IV describes the integration and design considerations with a discussion on the overall efficiency of the whole rectifier. The effect of load impedance and gate bias on the rectification efficiency is also discussed. Section V demonstrates the performance results and a comparison with the state-of-the-art works.

II. Theoretical Background and Analysis

A. PA-First Design Approach

Recently, several works have focused on applying the time-reversal duality theorem [23] to design rectifiers from Pas. The power flow through the switching device should be reversed to transform a PA into a rectifier. The concept is graphically depicted in Fig. 1. In a typical PA, dc power is converted to RF power at the output with a small RF signal at the input port. To reverse the power flow in the rectifier,

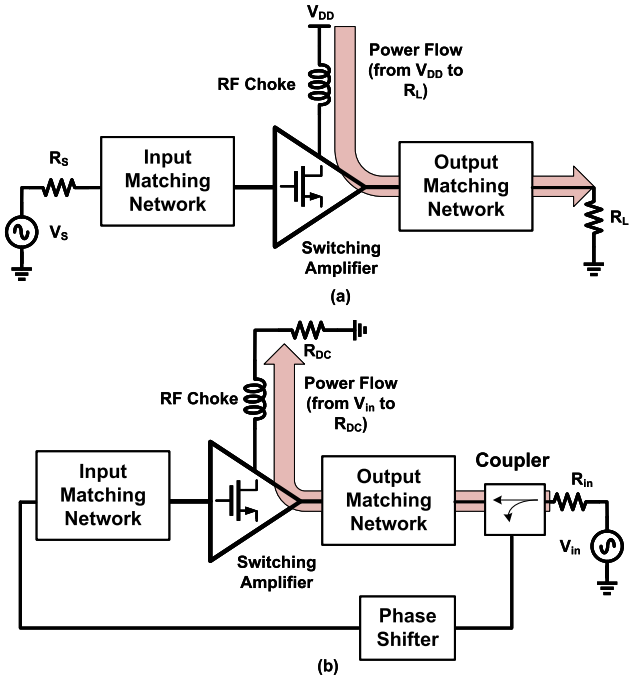

Fig. 1. Conceptual block diagrams of (a) PA and (b) synchronous rectifier.

RF power is applied to the output terminal of the PA, and appropriate ac excitation is provided to the switching device. The dc supply of the PA is replaced by an equivalent dc resistance R_{dc}. An appropriate gate drive signal is required for successful rectification, similar to the RF input signal in PA, which is amplified.

The gate drive is derived from the RF input signal applied to the drain in synchronous rectifiers. The phase of the gate signal must be adjusted for proper rectifier operation. Several previous works provide the phase shift by an external phase shifter [33], [34], which may cause impedance mismatch at the interfaces. Moreover, the required strength of the gate signal is much lower than the drain input signal for the rectifier. Hence, a coupler circuit is implemented to achieve the gate drive at the correct power level. The coupling coefficient should match the gain of the circuit in the PA mode. More on this will be discussed in the implementation section.

B. Dual-Band Matching Circuit

The multisection transmission line in the matching network can provide promising performance in dual-band PAs or rectifiers. The first demonstration of dual-band impedance transformation using a two-section transmission line network was in [40], where the target frequencies were separated by exactly one octave. Closed-form solutions for arbitrary frequency ratios were presented in [41], however, it was limited to real loads. Later, complex impedance transformation [42] and three-section dual-band transformers have also been proposed [43]. The three-section transformer method can be used for matching a single load to two different complex input impedances at two frequencies. Here, we have used a four-section impedance transforming network to match two different complex impedance values at two different frequencies, where the load impedance could also be a function

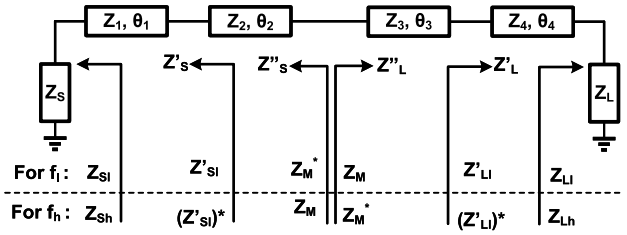

Fig. 2. Four-section network for complex load and source matching.

of frequency. The added section is utilized as a part of the coupler, and it also assists in achieving wider frequency bandwidth in each band.

We assume the required dual-frequency complex load and source impedance values are Z_L and Z_S with $Z_L = Z_{L,x} = R_{L,x} + jX_{L,x}$ and $Z_S = Z_{S,x} = R_{S,x} + jX_{S,x}$ for frequencies f_x, where $x = l, h$ (corresponding to the low- and high-frequency band). The characteristic impedances are referred to as Z_1, Z_2, Z_3, and Z_4 for the four-section transmission lines in Fig. 2. TL1 and TL4 are used to provide a conjugate condition between two operating frequencies for Z'_L and Z'_S, as shown in Fig. 2. The component parameters of TL1 and TL4 can be calculated [43], [44] and expressed as

$$Z_1 = \sqrt{\frac{R_{S1}|Z_{S2}|^2 - R_{S2}|Z_{S1}|^2}{R_{S2} - R_{S1}}} \tag{1}$$

$$Z_4 = \sqrt{\frac{R_{L1}|Z_{L2}|^2 - R_{L2}|Z_{L1}|^2}{R_{L2} - R_{L1}}} \tag{2}$$

$$\theta_1 = \frac{n\pi + \tan^{-1}\left[\frac{Z_1(R_{S1}-R_{S2})}{R_{S1}X_{S2}-R_{S2}X_{S1}}\right]}{\beta_1(1+m)} \tag{3}$$

$$\theta_4 = \frac{n\pi + \tan^{-1}\left[\frac{Z_4(R_{L1}-R_{L2})}{R_{L1}X_{L2}-R_{L2}X_{L1}}\right]}{\beta_4(1+m)}. \tag{4}$$

Here, n is an arbitrary integer, although, for practical implementation, its value is chosen 0 or 1; θ_1 and θ_4 are the electrical length of the transmission lines, TL1 and TL4, respectively. β_1 and β_4 are the phase constants for the corresponding transmission lines. The ratio between the two operating frequencies is given by a real number $m = (f_h/f_l)$. Consequently, the expression for Z''_L and Z''_S can be derived using transmission-line theory as

$$Z''_S = Z_2\frac{Z'_S + jZ_2\tan\theta_2}{Z_2 + jZ'_S\tan\theta_2} \tag{5}$$

$$Z''_L = Z_3\frac{Z'_L + jZ_3\tan\theta_3}{Z_3 + jZ'_L\tan\theta_3} \tag{6}$$

with $Z'_S = R'_S + jX'_S$ and $Z'_L = R'_L + jX'_L$. To satisfy the complex conjugate matching condition, we have

$$Z''_S = \left(Z''_L\right)^*. \tag{7}$$

After separating (7) into real and imaginary parts and some algebraic manipulation as described in [43], the equations can be summarized as

$$\tan(\beta_l l_2) \pm \tan(\beta_l l_1) = 0 \tag{8}$$

$$\tan(\beta_h l_3) \pm \tan(\beta_h l_3) = 0 \tag{9}$$

which results in multiple roots for l_2 and l_3. The equation for Z_2 is derived by replacing Z_3 in (5) and (6) as follows:

$$aZ_2^4 + bZ_2^3 + cZ_2^2 + dZ_2 + e = 0 \tag{10}$$

where the expressions of a, b, c, d, and e are given below

$$T = \tan\left(\frac{\pi}{1+m}\right) \tag{11}$$

$$a = -T^2R_L(R_L - R_S) \tag{12}$$

$$b = 2TR_L\left(R_SX_S - R_LX_L + T^2R_SX_L + T^2R_LX_S\right) \tag{13}$$

$$c = (R_L - R_S)\left[R_S\left(R_L^2 + X_L^2\right) - R_L\left(R_S^2 + X_S^2\right)\right] 2T^2(R_SX_L - 2R_LX_S)(R_SX_L + R_LX_S) - T^4(R_SX_L + R_LX_S)^2 \tag{14}$$

$$d = 2TR_LX_S\left(R_LX_S^2 + R_LR_S^2 - R_SX_L^2 - R_L^2R_S\right) 2T^3R_L\left[\left(R_S^2 + X_S^2\right)(R_SX_L + R_LX_S)\right] \tag{15}$$

$$e = T^2R_L\left(R_S^2 + X_S^2\right)\left[R_S\left(R_L^2 + X_L^2\right) - R_L\left(R_S^2 + X_S^2\right)\right]. \tag{16}$$

The fourth-order equation (10) can be solved numerically with the unreasonable or impractical roots ignored. The transmission lines are designed to operate in the two desired frequencies based on the equations listed above. Once the value of Z_2 is found, the value of Z_3 can be obtained by the following equation:

$$Z_3 = \frac{-B \pm \sqrt{B^2 - 4AC}}{2A} \tag{17}$$

where the A, B, and C parameters are defined as

$$A = -T^2R_S \tag{18}$$

$$B = (R_S - R_L)Z_2 - T(R_SX_L - R_LX_S) \tag{19}$$

$$C = T^2R_LZ_2^2 - T(R_SX_L - R_LX_S)Z_2. \tag{20}$$

From the two possible solutions of (17), the more practically realizable solution is considered for implementation. The solutions are applicable for both real and complex input–output impedances.

III. Proposed Dual-Band Rectifier

A. Dual-Band Power Amplifier Design

The first step in the design process is to define the PA parameters. Load–pull simulations are done with desired termination characteristics at harmonic frequencies based on our target frequency range. The load–pull simulation provides specific drain impedances at the fundamental frequencies. The output matching network provides fundamental matching at $f_l = 1.17$ GHz and $f_h = 2.4$ GHz. Upon performing load–pull simulation, load impedance values at fundamental frequencies are found as $Z_{\text{opt}}(f_l) = (30.46 + j26)\ \Omega$ and $Z_{\text{opt}}(f_h) = (13.8 + j28.9)\ \Omega$. The optimum impedances are shown in Fig. 3 and the simulated load–pull data is shown in Fig. 4. The load–pull simulation is performed with 27-dBm input power, a drain bias voltage of 28 V, and a gate bias voltage of −2.8 V.

We have chosen an inverse class-F and a class-F harmonic load network at low-band and high-band, respectively, to achieve high efficiency at both frequencies. The frequency

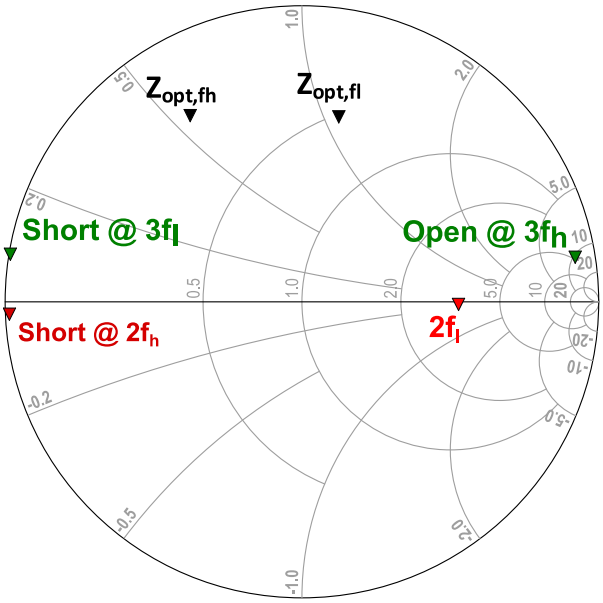

Fig. 3. Smith chart representation showing impedances at fundamental and harmonic frequencies for the two bands at the drain node of the PA.

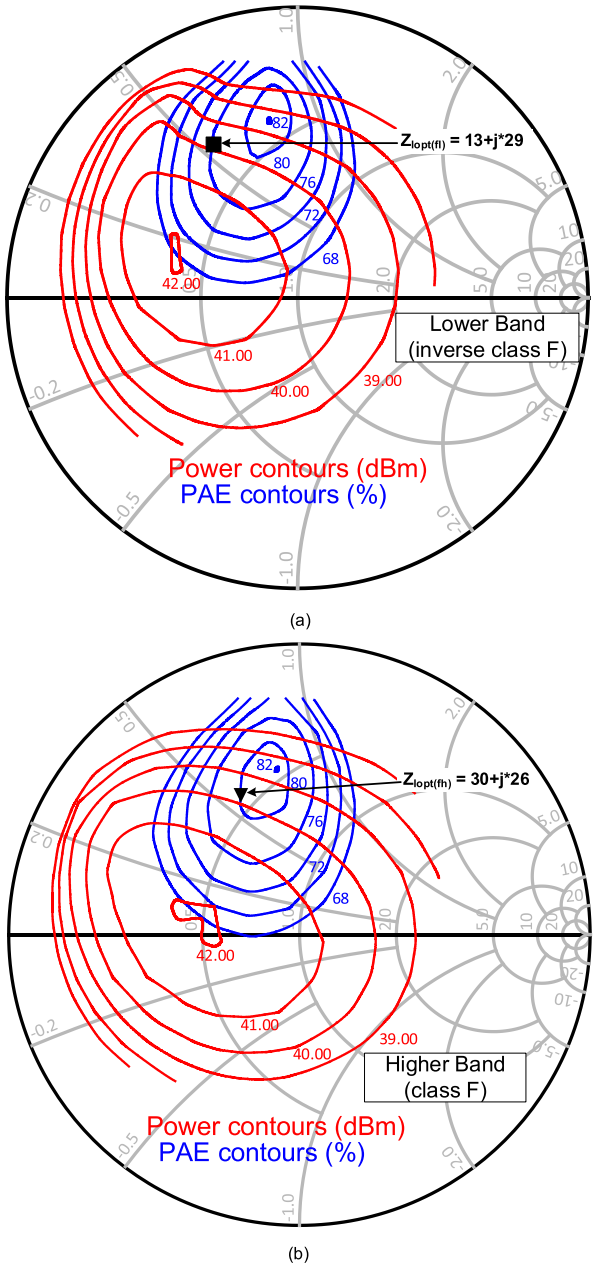

Fig. 4. Simulated load–pull simulation showing output power (dBm) and efficiency (%) contours of the PA in (a) 1.17 and (b) 2.4 GHz.

bands are one octave apart from each other. The harmonic termination conditions for the two class-F modes can be simultaneously satisfied by the same termination network. Fig. 5 shows the schematic of the proposed dual-band harmonic-tuned synchronous rectifier. The inductor L_d is chosen as an RF choke, which can be considered an open circuit at the desired frequencies. Here, two open stub microstrip lines (TL5 and TL6) are used for harmonic control, and the four-section series microstrip lines (TL1-4) are used to achieve the required fundamental load conditions for both bands concurrently. The design equations for the transmission lines are outlined in Section II.

For this operation, TL5 is designed as a quarter-wave open-ended stub at $3f_l$ and provides a short termination for the third harmonic at the drain node. Although the second harmonic impedance is critical for achieving high efficiency, for this design, the second harmonic frequency is quite close to the fundamental frequency of the high band (f_h). For this reason, the second harmonic open termination (very large impedance) is not used in this circuit. Instead, the impedance is about five times higher ($\sim$200 Ω) than the fundamental is used (as shown in Fig. 3). The odd harmonic short termination approximates an inverse class-F operation. An open termination at the second harmonic would further resemble an ideal inverse class-F operation and increase the efficiency [45]. To keep a compact footprint of the whole circuit, the second harmonic impedance was kept finite while maintaining reasonable rectification efficiency.

For the high-band harmonic tuning network, TL1 is designed to be $\lambda/2$ at $3f_h$, which makes the same impedances at nodes A and B at this frequency. The other two sections TL2 and TL6 are used to provide half-wavelength at $3f_h$, which ultimately makes an open termination at node A at $3f_h$. As a result, the class-F mode of operation is achieved at the higher frequency band. The physical dimensions of the transmission lines are enlisted in Table I. The characteristic impedance (Z_o) and effective electrical length ($\angle\theta^\circ$) are expressed with respect to f_l.

The output matching network is designed and simulated in Keysight ADS. Using these parameters of the matching circuits, the whole synchronous rectifier is designed, as shown in Fig. 5. The impedances seen at the drain node at the fundamental and harmonic frequencies are shown in the Smith chart (see Fig. 3).

Simulated and measured power-added efficiency of the PA are shown in Fig. 6. For this simulation and measurement, the load is terminated to 50 Ω, and the input dc power is 10 W. The plot shows a peak PAE of 76% at the low-frequency band and 74% at the high-frequency band in simulation. The peak

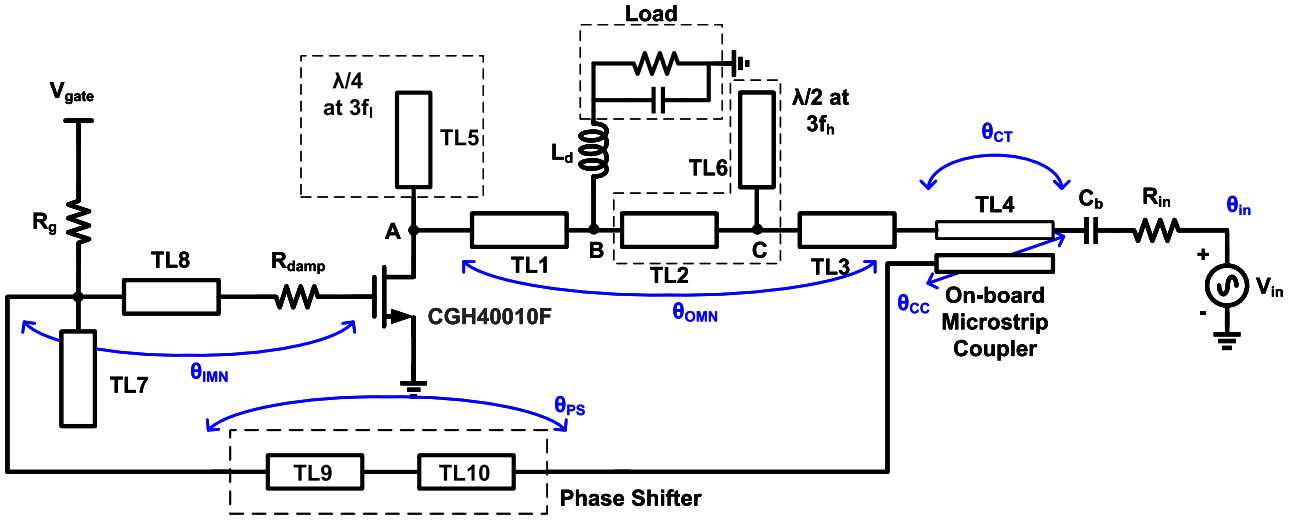

Fig. 5. Proposed dual-band harmonic-tuned synchronous rectifier with an integrated coupler and phase shifter.

TABLE I
PHYSICAL DIMENSIONS OF THE MICROSTRIP LINES (CORRESPONDING TO f_l)

TLine	Length (mm)	Width (mm)	Z_o	$\angle\theta°$
TL1	12.83	5	16.2	60
TL2	4.3	1.8	35	45
TL3	11.85	1.33	45	55.6
TL4	14.85	1.3	48	70
TL5	6.4	3.2	24	30
TL6	3.2	3.4	22.5	15
TL7	6.56	2.16	32.5	31.6
TL8	7.4	1.4	50	35
TL9	2.65	1.33	45	13
TL10	11.65	1.4	50	54.6

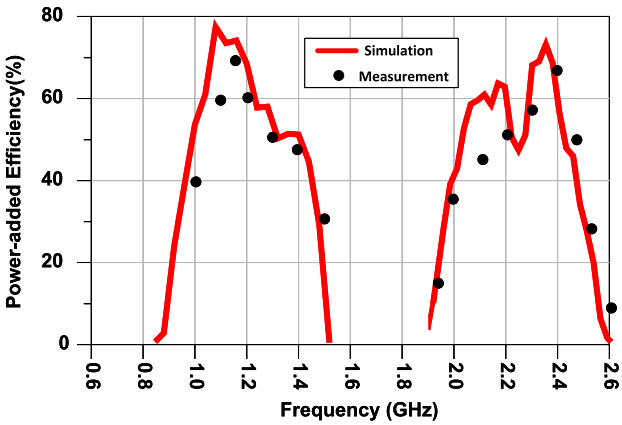

Fig. 6. Simulated and measured efficiency of the PA versus frequency. The efficiencies peak at 1.17 and 2.35 GHz.

efficiency occurs at 1.17 and 2.35 GHz in the lower and upper bands, respectively. The plot shows good agreement between simulation and measurement results.

Fig. 7 shows transient waveforms at the drain node of the PA with a power sweep. Fig. 7(a) shows the simulated waveforms at the lower frequency band. The PA operation approximates the inverse class-F mode, although the waveform is slightly distorted from the ideal class-F waveform. Fig. 7(b) shows the simulated waveform at the higher frequency band. In these simulations, input power is swept from 10 to 30 dBm so that the output power ranges from 22 to 42 dBm, with 40 dBm being the target input power for the rectifier circuit. The bias conditions of the PA are as follows: a drain voltage of 28 V and a gate–source voltage of −2.8 V. The point to be noted here is that the waveforms are simulated at the internal nodes of the device to get the actual characteristics of the voltage and current at the current generator plane. Additionally, the minimum drain–source voltage of the device always remains positive.

The small-signal characteristic of the PA is depicted in Fig. 8. The gain is 18 and 14 dB in the low-frequency and high-frequency bands, respectively. Fig. 8 also shows an exemplary input match across the desired frequency bands. S_{12} is also small, ensuring stable operation of the PA.

The stability of the PA is depicted in Fig. 9. Here, K is Rollett's stability factor that is defined as [46]

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{21}S_{12}|} \tag{21}$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21}. \tag{22}$$

From Fig. 9, we can observe that the PA is unconditionally stable, as $K > 1$, and $|\Delta| < 1$, for all frequencies.

The dual-band PA was fabricated separately for characterization, as shown in Fig. 10. This prototype does not include the microstrip coupler and gate feedback network which are required in the rectifier circuit only. The output and input matching networks are otherwise identical.

B. Wideband Coupler

Microstrip couplers have been employed extensively on PCB boards for various applications. When a pair of unshielded transmission lines are placed close to each other, the signal is coupled from one line to the other electromagnetically [46]. The propagation mode for this structure is assumed to be quasi-TEM. For simplicity, the analysis assumes pure TEM propagation to obtain a starting point in the design. With

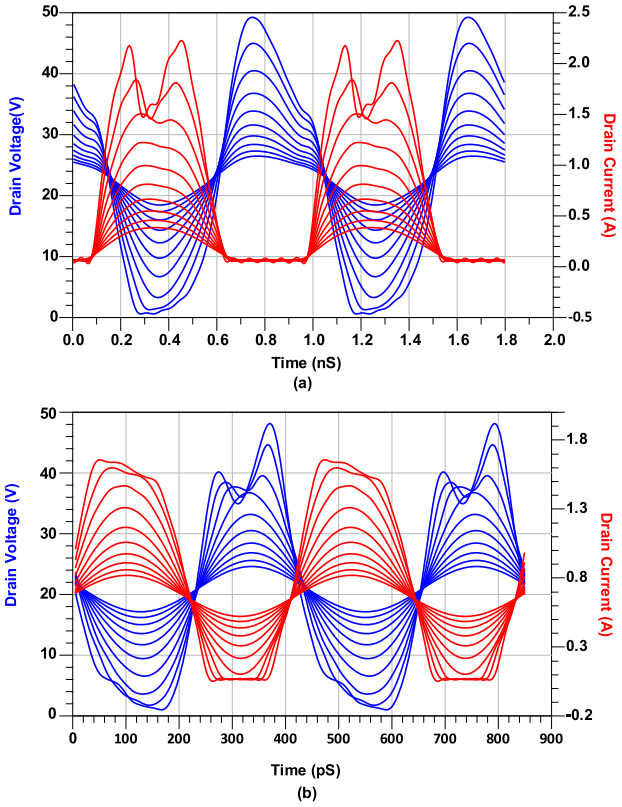

Fig. 7. Simulated transient waveform of the PA (swept power). (a) Low band operation approaching inverse class-F operation. (b) High band operation approaching class-F operation.

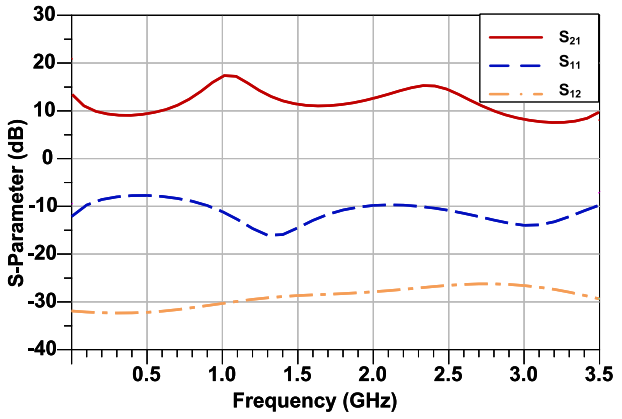

Fig. 8. Simulated small-signal characteristic of the PA. It shows gains of 18 and 14 dB at the low band and high band, respectively.

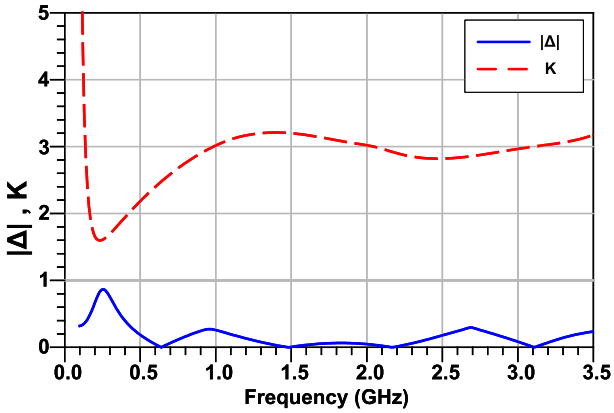

Fig. 9. Simulated stability characteristic of the PA with respect to the frequency.

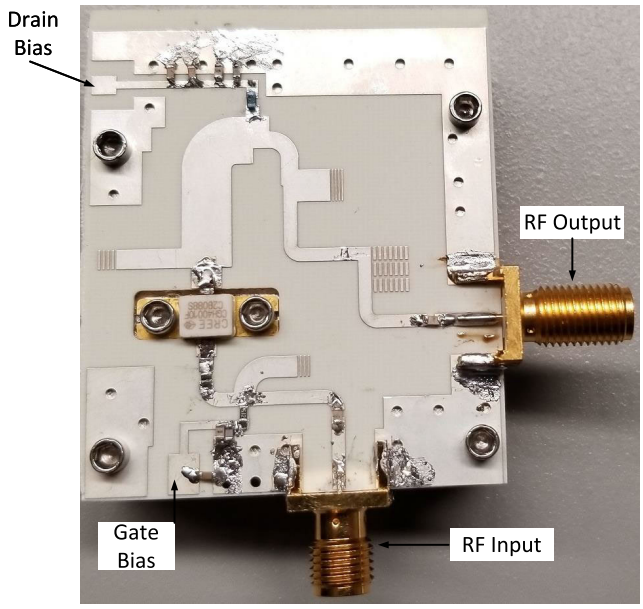

Fig. 10. Photograph of the fabricated dual-band harmonic-tuned PA circuit.

the help of CAD tools using numerical methods, more accurate design parameters are then calculated.

The microstrip coupler is a four-port network with power being supplied to port 1, which is coupled to port 3 with a coupling factor C. The coupling factor refers to the ratio of the input power to the power delivered to the coupled port. The remainder of the input power is delivered to port 2, which is the through port. In the ideal directional coupler, no power is delivered to port 4, which is the isolated port. For our case, we want to have a coupling factor close to the intrinsic gain of the PA, which is about 18 dB in the lower frequency band and 14 dB in the higher frequency band, so that the amplitude of the gate signal is similar to that in the PA mode. Since the coupling factor is low, we interchanged the location of the coupled port and isolated port. By keeping the coupled port (port 3) open, and feeding the gate signal from port 4, the layout is simplified, which also ensures the required gate signal strength is derived from the RF input signal.

The three design parameters for the coupler are trace width, trace length, and spacing between the through line and coupled line. The trace width was chosen at 1.33 mm as it provides wideband input matching from 1 to 3 GHz. The transmission line section TL4 is replaced with the through section of the coupler. The electrical length of TL4 is chosen as $\lambda/2$ at f_l, and the coupler has sufficient bandwidth around the two frequency bands of interest to maintain the characteristic of the directional coupler. Moreover, for f_h, the electrical length approaches one wavelength, essentially reducing the impact of impedance mismatch due to the addition of the coupler. The physical length of this section is 14.85 mm.

The spacing between the two traces determines the coupling factor. Using Keysight ADS, the spacing was chosen based

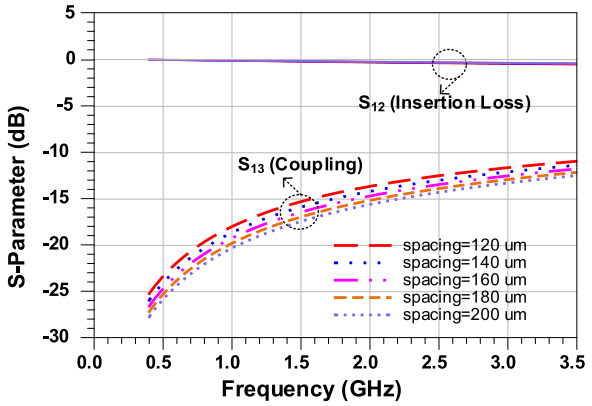

Fig. 11. Frequency response (simulation) of the coupler showing low insertion loss across a wide frequency range.

on the simulated results. Fig. 11 shows insertion losses and coupling factors for various spacing.

From the simulation results, the appropriate spacing is found to be 180 μm, as it generates a coupling factor of -18.6 dB at the low-frequency band and -14.1 dB at the high-frequency band. The coupling factors are chosen such that the same level of the gate drive is provided in the rectifier mode that is seen in the PA mode. Since the required gate drive power is around 22–23 dBm in the PA mode for maximum output power, the coupler provides 18–14-dB attenuation for an output power level of 40 dBm. The coupling factors compensate for the amplifier gain in the two bands, as shown in Fig. 8. The insertion loss in the through path is small, ranging from 0.2 to 0.3 dB for the low- and high-frequency bands, respectively. The cyclic phase shift introduced by the coupler is close to zero in the desired frequency bands, as shown in Fig. 12. A prototype for the coupler was fabricated for characterizing separately [as shown in Fig. 12(a)]. The measured insertion loss shows good agreement with simulated results.

C. Dual-Band Phase Shifter

The gate matching network lies between the coupled port of the coupler and the gate of the device. It provides appropriate harmonic termination for the gate drive and the required phase shift for rectifier operation. A two-section transmission line-based phase shifter is implemented for this design. The design procedure to determine the characteristics of the phase shifter is described next.

The required phase difference between the gate and the drain (θ_{req}) terminals is 180° or an odd multiple of 180°. Mathematically, it can be expressed as

$$\theta_{\text{req}} = (\theta_D - \theta_G) = (2n+1)\pi \ \text{(rad)} \tag{23}$$

where θ_G is the phase at the gate terminal, θ_D is the phase at the drain terminal, and n is an integer. This condition needs to be satisfied at both frequency bands. From Fig. 5, the phase at the gate is

$$\theta_G = \theta_{\text{CC}} + \theta_{\text{PS}} + \theta_{\text{IMN}} + \theta_{\text{in}}. \tag{24}$$

Here, θ_{CC} is the phase at the coupled port of the coupler, θ_{PS} is the phase shift provided by the phase shifter (consisting of

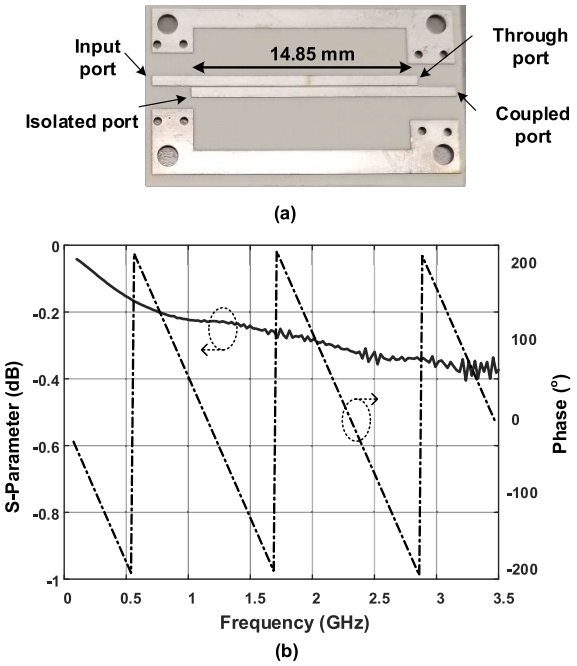

Fig. 12. (a) Photograph of the coupler prototype. (b) Insertion loss (measured) of the onboard coupler.

TL9, TL10), and θ_{IMN} is the phase shift of the input matching network provided by TL7 and TL8. Similarly, the phase at the drain terminal is expressed as

$$\theta_D = \theta_{\text{CT}} + \theta_{\text{OMN}} + \theta_{\text{in}}. \tag{25}$$

Here, θ_{CT} is the phase at the coupler through the port, and θ_{OMN} is the phase contribution of the output matching network consisting of TL1, TL2, TL3, TL5, and TL6. θ_{in} corresponds to the phase of the input power. From (23)–(25), a general equation of θ_{PS} is

$$\theta_{\text{PS}} = (2n+1)\pi + (\theta_{\text{CT}} + \theta_{\text{OMN}} + \theta_{\text{in}}) - (\theta_{\text{CC}} + \theta_{\text{IMN}} + \theta_{\text{in}}). \tag{26}$$

For convenience, the listed phase quantities are depicted in Fig. 5. Using the analysis provided in Section II, the physical parameters of TL9 and TL10 are derived. A simulation plot of the phase shifts is shown in Fig. 13. It is observed that the phase shift between the gate and drain terminal of the device approaches $-180°$ at the lower frequency band, which corresponds to $n = 0$ from (23). In the higher frequency band, the phase difference approaches $-540°$, which corresponds to $n = 1$ from (23).

D. Input Matching Network

From the datasheet of Cree Inc., the source impedance of the device varies from 7 to $(3.2–j4.5)$ Ω. The matching network at the gate is designed to provide close to these low impedances for higher efficiency. In addition, a small resistance of $R_{\text{damp}} = 1.5$ Ω has been added in series to improve stability. An even harmonic short using TL7 for a lower frequency band (1.17 GHz) is added to reduce harmonic injection through C_{gd} from the drain side. Since the second harmonic for the high-frequency band sees a short termination

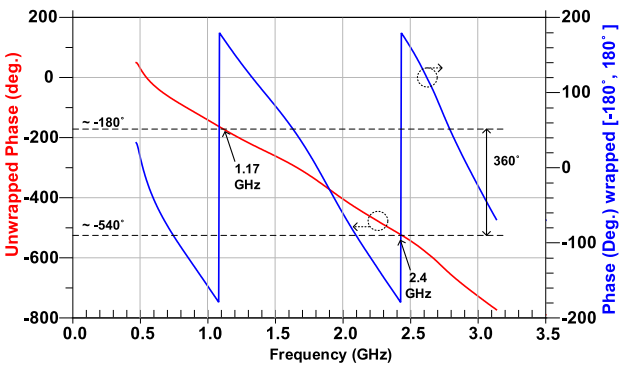

Fig. 13. Phase response (simulation) of the rectifier showing the difference in phase between the gate and drain (θ_{GD}). θ_{GD} approaches $-180°$ in the desired bands.

at the drain, even harmonics' injection of the high-frequency band is suppressed. The phase responses of the gate-matching network are described in detail in Section III-C.

E. Rectifier Integration

Once all the components are designed and tested separately, they are combined to form the synchronous rectifier. Upon forming the transmission line lengths based on the methodology discussed above, the electrical length of the phase shifter was adjusted to achieve the correct waveforms at the internal drain node of the active device. Transient waveforms obtained from harmonic balance simulation in ADS are shown in Fig. 14. Fig. 14(a) shows current and voltage waveforms in the low-frequency band in the inverse class-F mode, and Fig. 14(b) shows current and voltage waveforms in the class-F mode. The current waveform is negative, as expected from the time-reversal duality principle.

IV. Experimental Results and Discussion

A low-loss Rogers 20-mil 4350B substrate with $\epsilon_r = 3.66$ and $\tan\delta = 0.003$ is used to fabricate a PCB board for demonstrating the operation of the dual-band harmonic tuned rectifier. The active device is a 10-W Cree GaN-HEMT (CGH40010F) component. High-Q compact-size chip inductors from Coilcraft (0603CS) are used for biasing an RF choke. Decoupling and dc blocking capacitors are used from ATC (600S27). To provide the continuous-wave RF input power, a Keysight E8257D signal generator is used.

To boost the input power up to 40 dBm, a two-stage driving amplifier consisting of an amplifier from Cree (CGH27015-AMP) and the proposed dual-band PA is used. Since the drive amplifier from Cree has limited gain (especially at the lower frequency band), we had to use a second-stage amplifier. A directional coupler with a power meter attached to its coupled port is used to observe and calibrate the input power (P_{in}) to the rectifier. A fixed 0.5-dB attenuator has been added between the input of the directional coupler and the driver PA to desensitize the directional coupler to changes in the output impedance of the driver PA. In addition, an isolator is used between the directional coupler output and the rectifier input to ensure that the rectifier sees a 50-Ω impedance

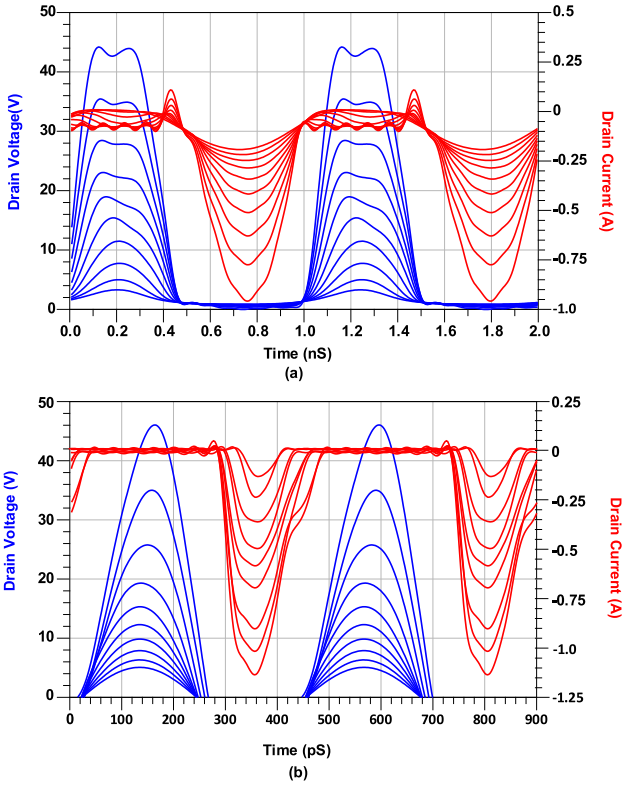

Fig. 14. Simulated transient waveforms of the rectifier (swept RF input power from 12 to 30 dBm). (a) Low band operation derived from the inverse class-F mode of the PA. (b) High band operation derived from the class-F mode of the PA.

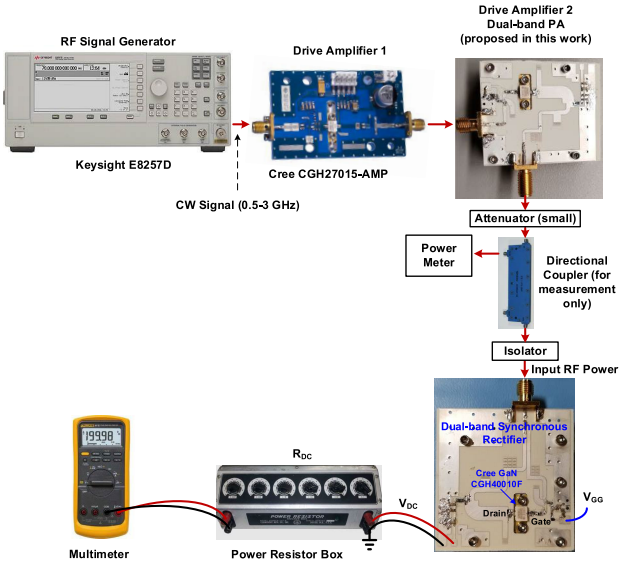

Fig. 15. Measurement test bench with a signal generator and a two-stage driver for the harmonic-tuned dual-band synchronous rectifier.

at its input port. The losses from the attenuator, isolator, and directional coupler have been de-embedded for accurate measurement. An external adjustable power resistor is used as the load. A dc source is used for providing negative gate bias to the active device. A photograph of the experimental test bench setup is shown in Fig. 15. Fig. 16 shows detailed photograph of the rectifier. The circuit occupies 5 × 5.2 cm in size.

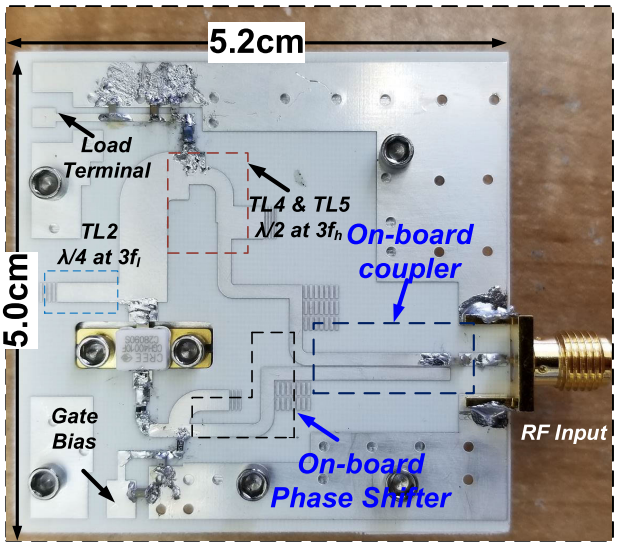

Fig. 16. Photograph of the fabricated dual-band harmonic-tuned synchronous rectifier circuit.

Fig. 17 demonstrates the output voltage and rectification efficiency versus frequency. In this measurement, the dc load resistance and the gate bias are not optimized to get maximum efficiency for each band. The rectification efficiency is the ratio of the output dc power and the input RF power mathematically expressed as

$$\eta_{\text{rect},\%} = \frac{V_{\text{dc}}^2}{R_{\text{dc}} \times P_{\text{in}}} \times 100\%. \tag{27}$$

Here, V_{dc} is the output dc voltage across the load R_{dc}. As shown in Fig. 17, there are two distinct peaks in efficiency, which shows the dual-band operation of the circuit. The bias condition and RF input power for this measurement are kept as follows: $V_{\text{gg}} = -4.5$ V, $P_{\text{RF,in}} = 40$ dBm. The dc load resistance is kept constant at 50 Ω.

The low band's peak efficiency is 77% achieved at an input power of 38.2 dBm. An input power sweep at this frequency is shown in Fig. 18, where the output dc power and efficiency are reported. The dc power at this level is 5.1 W. The overall trend at this frequency shows good agreement with the previously reported class-F-1 rectifier [33], [47]. Measured efficiency and output dc power for three load values are shown in Fig. 18. The optimum load resistance for this frequency is observed at $R_{\text{dc}} = 35$ Ω. Fig. 18 also shows a higher input power range compared to the 2.4-GHz operation, which is expected since, at 2.4 GHz, the rectifier operates in the class-F mode, whereas it operates in the inverse class-F mode at 1.17 GHz. The input power range is higher in this mode, maintaining at least 50% efficiency for 25-dBm input power.

Measurement results show that at 2.4 GHz, output dc power reaches 7.18 W for 9.5-W input, making the efficiency 75%, as shown in Fig. 19. The efficiency remains above 50% even when input power is 32 dBm (∼1.5 W), which shows good efficiency at the back-off input power region. The same variation of load resistance is carried out here. The optimum load resistance value for the high-frequency band is 50 Ω, as shown in Fig. 19.

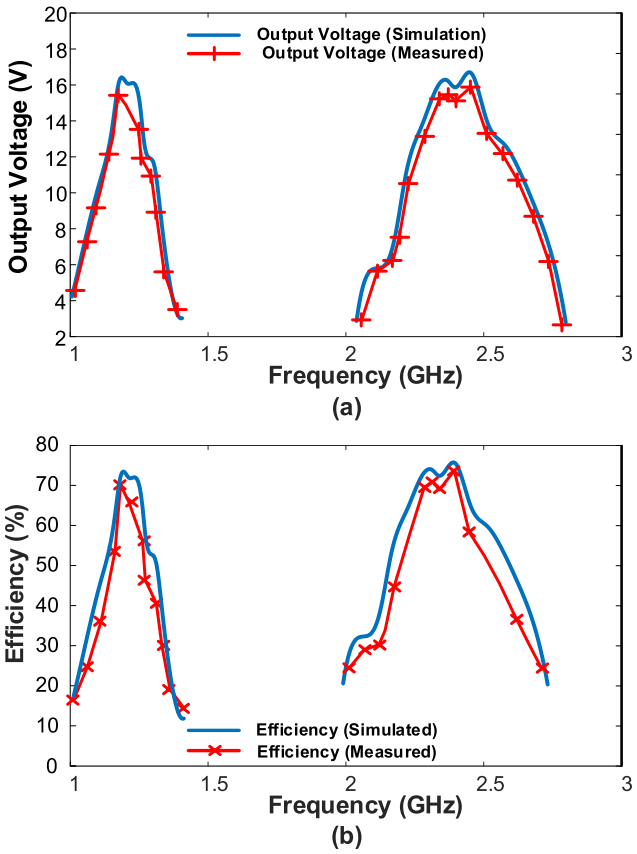

Fig. 17. Simulated versus measured output dc voltage and efficiency across frequency for a load of 50 Ω (only the frequencies around 1.17 and 2.4 GHz are shown).

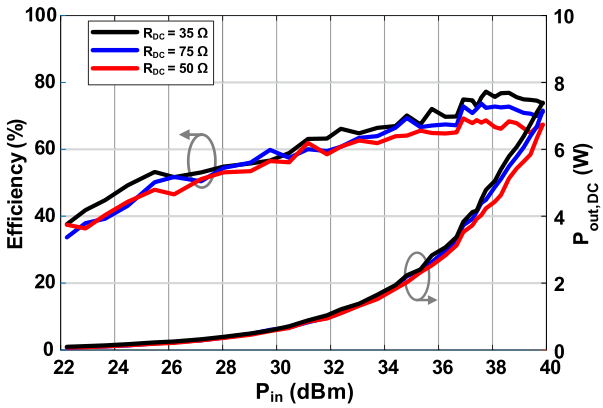

Fig. 18. Measured efficiency and output dc power versus input power at 1.17 GHz for three different load resistances. Peak efficiency is observed at $R_{\text{dc}} = 35$ Ω.

The gate bias has a significant effect on the performance of the rectifier. The gate bias is negative because the device is a depletion mode device. To show the effect of the gate bias on the efficiency of the rectifier, the gate bias is varied for both high- and low-frequency operations. Fig. 20 shows the rectification efficiency versus input power for different gate bias voltages. The peak efficiency is observed at $V_{\text{gs}} = -4.2$ V. Although the efficiency quickly drops as the input power level decreases, the efficiency is >60% when the input power is higher than 32 dBm (∼1.5 W), which shows good efficiency

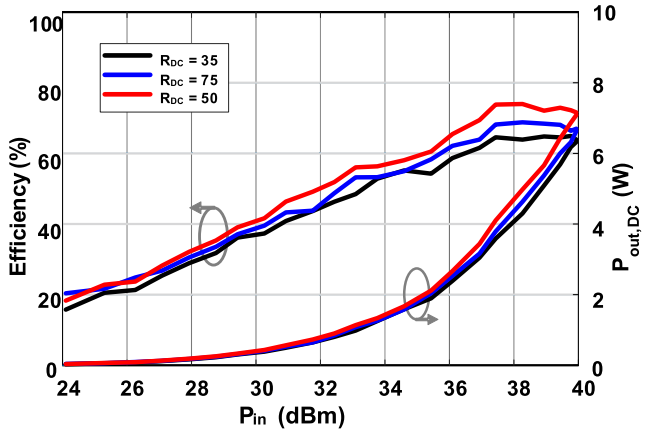

Fig. 19. Measured efficiency and output dc power versus input power at 2.4 GHz for three different load resistances. Peak efficiency is observed at $R_{dc} = 50\ \Omega$.

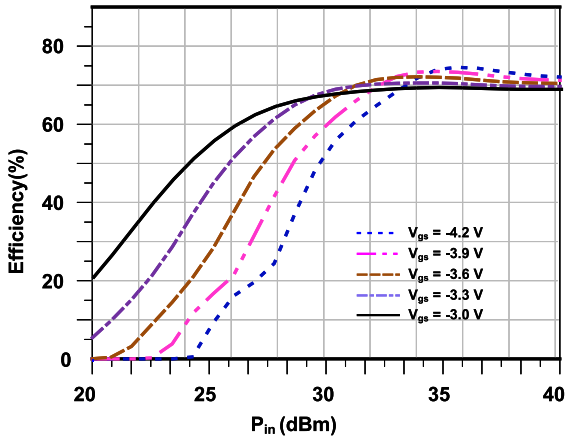

Fig. 20. Measured efficiency versus input power at 1.17 GHz for different gate bias voltages. Peak efficiency is observed at $V_g = -4.2$ V.

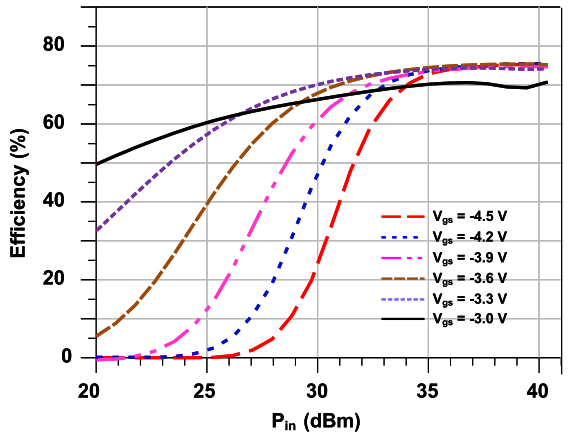

Fig. 21. Measured efficiency versus input power at 2.4 GHz for different gate bias voltages. Peak efficiency is observed at $V_g = -3.6$ V.

at the input back-off region. Since the PA operation is in inverse-class F at this frequency, we see a better performance in the back-off power region. Although the peak efficiency is reduced by ~4%, $V_{gs} = -3$ V shows a better dynamic range.

A similar trend is seen for the high-frequency band, which is shown in Fig. 21. The difference between the efficiency curves at the two bands is that the high-frequency case has a faster decline in efficiency at the power back-off. The peak efficiency in the high-frequency band is observed at $V_{gs} = -3.6$ V. The faster decline is attributed to the class-F operation of the amplifier at this frequency. With V_{gs} approaching -3 V, the peak efficiency of the rectifier is reduced while back-off efficiency improves.

In our observations of the efficiency characteristics of the rectifiers, we have seen an increase in efficiency compared to PAs in a similar mode of operation. The increase in efficiency at the back-off region can be attributed to the difference in the Thevenin equivalent resistance at the output of the amplifier/rectifier [33]. In the amplifier, the dc supply has a fixed voltage (V_{DD}) for the peak power condition. As input power reduces, the dc supply current decreases, and the equivalent Thevenin resistance of the supply changes significantly. For this reason, in the amplifier mode, efficiency reduces at a greater rate in the back-off region. In the rectifier case, load R_{dc} is fixed, and the value is close to the peak power Thevenin equivalent resistance in the amplifier mode. The dc load voltage at the output of the rectifier changes as the RF input power changes.

Another interesting observation as shown in Figs. 18 and 19 is that the efficiency in the back-off region is higher when the rectifier is operating in the inverse class-F mode. This can be explained by comparing the loss mechanisms of the two modes. In class-F, the voltage is switched, which means that there are losses associated with the discharge of the output capacitance of the device. In the inverse class-F, the current is switched, as a result, capacitive switching loss in the inverse class-F is lower. The theory is mathematically explained in [33], and similar characteristic trends have been presented in other publications [47], [48].

V. Performance Comparison With State-of-the-Art

In this section, a performance comparison of this work with state-of-the-art is presented in detail. Although there have been several multiband rectifiers in literature [36], [37], [38], [39], most of them are diode-based rectifiers with degraded efficiency (<65%) at lower operating power (<1.5 W). Our proposed work is the first demonstration of a dual-band harmonic-tuned GaN-based synchronous rectifier [1]. Only recently, there have been a couple of dual-band synchronous rectifiers demonstrated with comparable efficiency [49], [50]. Hence, the top section of Table II compares other single-band GaN-based synchronous rectifiers, along with the aforementioned papers. This part shows that our proposed work has similar or better rectification efficiency while operating at two different frequency bands.

In the bottom part of Table II, we have compared our proposed work with multiband Schottky diode-based rectifiers. Although these circuits can operate at multiple frequency bands, the output power level is much lower compared to our work. Moreover, the substrate loss becomes more prominent in these designs, resulting in lower efficiency. Compared to prior arts, our proposed work provides a complete solution with a gate feedback network, while maintaining high efficiency in dual-frequency bands with a 10-W power level.

TABLE II
PERFORMANCE SUMMARY OF SYNCHRONOUS RF RECTIFIERS

Ref.	Device	Freq. (GHz)	Pin (W)	Load resistance	Effi. (%)	Matching type	Mode/Class of operation	
This work	GaN HEMT	**1.17** **2.4**	**10** **10**	**35** **50**	**77** **75**	**Dual-band harmonic tuning**	Modified PA	**Class-F^{-1}** **Class-F**
MWCL'17 [34]		1.8	10	45	77	Harmonic tuning		Class-F^{-1}
IMS'14 [25]		10.1	3.18	100	63.9	Passive tuning		Class-C
TPE'18 [29]		2.8	10	17	70/8	Harmonic tuning		Class-E
EuMC'15 [30]		0.91	11.9	50	85	Harmonic tuning		Class-F^{-1}
TMTT'12 [31]		2.14	10	98	85	Harmonic tuning		Class-F^{-1}
TMTT'15 [47]		1.2	6.6	90	75	Harmonic tuning		Class-E
IMS'17 [28]		0.915	1.6	85	84	Harmonic tuning		Class-E
EuMC'15 [51]		1.85	8.5	50	83.6	Harmonic tuning		Class-C
MDPI'21 [52]		2.4	11.2	100	69.6	Independent 2nd harmonic tuning		Class-F
CSRSWTC '21 [49]		2/2.5	10	50	75/74	Dual-band harmonic tuning		Class-EFJ
MWCL'22 [50]		1.9/2.4	10	70	75/76	Dual-band harmonic tuning		Class-F
IMS'17 [37]	Schottky Diode	2.45/5.8	0.01	1000	64.8/62.2	Dual-band harmonic tuning	Diode Recitifiers	
WPT'13 [36]		2.45/5.8	0.01	1050	66.8/51.5	Dual-band harmonic tuning		
RWS'13 [53]		2.45/5.8	0.013	1000	64.2/67.9	Dual-band harmonic tuning		
TCAS-I'19 [54]		0.915/2.45	0.032	1500	74.9/71.2	Dual-band harmonic tuning		
TMTT'19 [38]		0.915/2.45	1.5	620/4700	66/58	2 branch impedance matching		
TIE'18 [39]		2.45/5.8	0.063	360	76.2/61	Dual-band harmonic tuning		

VI. CONCLUSION

This work presents a detailed design methodology for designing a dual-band harmonic-tuned synchronous RF rectifier with measurement data. The rectifier employs a GaN HEMT device with a harmonic-tuned load-matching network. A microstrip coupler is used to derive the gate excitation signal from the input RF power. An integrated transmission line-based phase shifter is used for proper gate excitation. The design methodology of each component has been thoroughly explained with design equations. The proposed rectifier integrates the coupler, phase shifter, and PA on the same board for the first time. As a result of the compact harmonic-tuned structure, the synchronous rectifier shows good efficiency in both target frequency bands. Detailed measurement results of the circuit are presented with different load values and gate bias voltages. The rectifier also demonstrates a wide input power range with efficiency above 50%, and a detailed discussion on the enhanced efficiency in the back-off region is provided. The rectifier could be an attractive candidate for high-power dual-band RF-dc energy harvesters.

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