

CCAT-prime: RFSoc Based Readout for Frequency Multiplexed Kinetic Inductance Detectors

Adrian K. Sinclair^a, Ryan C. Stephenson^b, Cody A. Roberson^c, Eric L. Weeks^c, James Burgoyne^a, Anthony I. Huber^d, Philip M. Mauskopf^{b,c}, Scott C. Chapman^{a,d,e}, Jason E. Austermann^g, Steve K. Choi^f, Cody J. Duell^f, Michel Fich^h, Christopher E. Groppi^c, Zachary Huber^f, Michael D. Niemack^f, Thomas Nikolaⁱ, Kayla M. Rossiⁱ, Adhitya Sriram^c, Gordon J. Stacey^j, Erik Szakiel^f, Joel Tsuchitori^a, Eve M. Vavagiakis^f, Jordan D. Wheeler^g, and the CCAT-prime collaboration¹

^aDept. of Physics and Astronomy, University of British Columbia, Vancouver, BC, Canada

^bDept. of Physics, Arizona State University, Tempe, AZ, USA

^cSchool of Earth and Space Exploration, Arizona State University, Tempe, AZ, USA

^dDept. of Physics and Astronomy, University of Victoria, Victoria, BC, Canada

^eHerzberg Astronomy and Astrophysics Research Centre, National Research Council Canada, Victoria, BC, Canada

^fDept. of Physics, Cornell University, Ithaca, NY, USA

^gNational Institute of Standards and Technology, Boulder, CO, USA

^hWaterloo Centre for Astrophysics, University of Waterloo, Waterloo, ON, Canada

ⁱCornell Center for Astrophysics and Planetary Sciences, Cornell University, Ithaca, NY, USA

^jDept. of Astronomy, Cornell University, Ithaca, NY, USA

ABSTRACT

The Prime-Cam instrument on the Fred Young Submillimeter Telescope (FYST) is expected to be the largest deployment of millimeter and submillimeter sensitive kinetic inductance detectors to date. To read out these arrays efficiently, a microwave frequency multiplexed readout has been designed to run on the Xilinx Radio Frequency System on a Chip (RFSoc). The RFSoc has dramatically improved every category of size, weight, power, cost, and bandwidth over the previous generation readout systems. We describe a baseline firmware design which can read out four independent RF networks each with 500 MHz of bandwidth and 1000 detectors for ~ 30 W. The overall readout architecture is a combination of hardware, gateway/firmware, software, and network design. The requirements of the readout are driven by the 850 GHz instrument module of the 7-module Prime-Cam instrument. These requirements along with other constraints which have led to critical design choices are highlighted. Preliminary measurements of the system phase noise and dynamic range are presented.

Keywords: CCAT-prime, RFSoc, MKID, frequency multiplexed, kinetic inductance

1. INTRODUCTION

The far-infrared sky, loosely defined from ~ 100 GHz to a few THz, has been a challenging band of the electromagnetic spectrum to observe. Atmospheric absorption and emission require strategic band selection and extraordinarily dry and high altitude observation sites. In part due to these challenges the far-infrared (far-IR) sky still has many motivating and clear science goals,¹ a few of these are highlighted below. The role of turbulence and magnetic fields can be studied through the polarized far-IR emission of interstellar dust grains. The variability in protostars which informs stellar accretion and planet formation models can be studied from mid to far-IR. Galaxy formation and star formation history can be tracked through redshifted lines such as CO, OIII,

Further author information: (Send correspondence to A.K.S.)

A.K.S.: E-mail: adriansinclair@phas.ubc.ca

and CII, which fall into the same band. High redshift proto-clusters of galaxies can be probed via the kinematic Sunyaev-Zel'dovich effect at hundreds of gigahertz. On the largest scales, the cosmic microwave background requires well calibrated sub-millimeter observations of polarized dust emission to remove its contaminating foregrounds. These are just a few of the motivating science topics for the Fred Young Submillimeter Telescope and first light instruments described next.

Seated high atop Cerro Chajnantor in the Atacama desert of Chile, the CCAT-prime observatory will include the Prime-Cam instrument on the Fred Young Submillimeter Telescope (FYST) and will map the sky with imaging polarimeters²⁻⁴ and spectrometers.^{5,6} The telescope's wide field of view and large optical throughput^{7,8} enables high detector count focal planes. Mod-Cam⁹ is a single instrument module receiver that is a precursor and testbed for Prime-Cam and is planned to achieve first light in 2024. The enabling detector technology is the Lumped Element Kinetic Inductance Detector (LEKID) which, due to its natural multiplexing, low fabrication cost, and low cryogenic readout complexity, can be scaled to the $> 100,000$ detectors required for Prime-Cam. A second enabling technology is the Xilinx Radio Frequency System-on-Chip (RFSoc) which has dramatically improved every category of size, weight, power, cost, and bandwidth over the previous generation KID readout systems.

Kinetic Inductance Detectors (KIDs) were developed nearly twenty years ago¹⁰ to enable ultra-wideband astronomical imaging at low fabrication cost with high multiplexing factors into the thousands. Since then, single photon sensitivity with modest energy resolution has been achieved from X-rays to the near-infrared.¹¹⁻¹³ At longer wavelengths in the millimeter and submillimeter, photon noise limited performance has been shown in linear power detection mode.¹⁴⁻¹⁸ There are recent encouraging results with sub-gap absorption KIDs,¹⁹ DC biasing,²⁰ and bi-layers,²¹ opening up even longer wavelength detection typical of CMB studies. KIDs have been antenna coupled,^{22,23} horn coupled,²⁴⁻²⁶ and packed into filled arrays,²⁷ each achieving high optical efficiency to allow dense focal plane packing. A shift from distributed to a lumped element kinetic inductance detector (LEKID)²⁸ design has simplified frequency placement and relaxed simulation requirements. The majority of the current and previously deployed mm/sub-mm imaging telescopes which utilize KIDs have adopted lumped element designs.²⁹⁻³⁵ Prime-Cam will employ a lumped element design that is horn coupled capitalizing on the development experience of the BLAST-TNG and TolTEC LEKID arrays.²⁶

Early KID readouts leveraged advancements in commercially available software defined radio technology³⁶ and previously developed radio astronomy spectrometers.^{37,38} Custom boards started to be developed in the early 2010s.³⁹⁻⁴¹ A reconfigurable open-architecture computing hardware (ROACH) based system, originally designed for radio astronomy, was repurposed by multiple groups,^{29,42,43} as well as the second generation of the board (ROACH2) a few years later.⁴⁴⁻⁴⁶ The open source firmware developed for the ROACH2 based readout of BLAST-TNG⁴⁴ has enjoyed use in the following experiments: OLIMPO,⁴⁷ MUSCAT,⁴⁸ SuperSpec,⁴⁹ and TolTEC.³⁴ The RFSoc by Xilinx arrived near the end of the decade and immediately generated interest in the community and spurred multiple parallel development efforts.⁵⁰⁻⁵⁵ This work presents an RFSoc based readout to be deployed on FYST for the Mod-Cam and Prime-Cam instruments and a future on-chip spectrometer.

2. REQUIREMENTS

The main driver of the readout system requirements are the detectors in five ways: Total number of detectors, number of detectors per RF network, bandwidth per network, added noise, and crosstalk. There are more stringent requirements for the frequency comb discussed in the gateway Sec. 3.3.1. For the 280 GHz, 350 GHz, and EoR-Spec detector arrays the baseline bandwidth of ~ 500 MHz with 600 resonators or less per RF network has been adopted. In order to adhere to thermal budget constraints, Prime-Cam's highest frequency instrument - the 850 GHz module⁵⁶ is planning for two octaves of bandwidth (1 GHz) for each RF network. The 850 GHz arrays push the bandwidth requirements from the detectors to the readout while previous KID arrays developed for BLAST-TNG¹⁵ and TolTEC²⁶ have been constrained by the instantaneous bandwidth of the ROACH2 based readout.⁴⁴ The readout noise and crosstalk requirements are derived from detector parameters in the next two sections.

2.1 Readout Noise Requirement

The readout system should not contribute significantly to the noise, which places a requirement on both the noise and dynamic range of the system. We use the method of Sipola et al.⁵⁷ to calculate an equivalent output noise temperature of the KID and compare this to other readout contributors such as the cryogenic low noise amplifier (LNA) and digital to analog converter (D/A). The detector equivalent output noise temperature is defined as,

$$T = \frac{(R \times \text{NEP})^2}{kZ_0}, \quad (1)$$

where R is the voltage responsivity to power, NEP is the detector noise equivalent power, k is Boltzmann's constant, Z_0 is the circuit's characteristic impedance of 50 Ω . The voltage responsivity can be derived from the complex forward transmission of a resonator,⁵⁸

$$S_{21} = 1 - \frac{Q_r}{Q_c} \frac{1}{1 + j2Q_r x}, \quad (2)$$

where Q_r and Q_c are the total and coupling quality factors respectively, and x is the fractional frequency shift. The voltage at the output of the resonator would be the product of the voltage incident on the resonator with the transmission, $V_{out} = V_{in} S_{21}(x)$. Appendix A.1 shows that the resulting voltage responsivity to power is then

$$\frac{dV_{out}}{dP} = V_{in} \frac{dx}{dP} \left(\frac{d\text{Re}\{S_{21}\}}{dx} + j \frac{d\text{Im}\{S_{21}\}}{dx} \right), \quad (3)$$

where V_{in} is the incident voltage of the bias tone, and dx/dP is the fractional frequency responsivity to optical power.

The two main readout noise contributors considered here are the LNA and D/A. We compare the noise at a reference plane after the resonator array and before the LNA. This is convenient for the LNA as the measured noise temperature reported is referred to the input of the amplifiers. The amplifiers to be used in initial deployment have input noise temperatures of approximately 5 K across the band.⁵⁹ The D/A noise however depends on the total attenuation to the reference plane. The quantization noise power can be estimated from the variance of the error first derived by Bennett⁶⁰ in 1948 as

$$P_{digi} = \frac{\Delta V^2}{12Z_0} = \frac{1}{12Z_0} \frac{V_{FS}^2}{2^{2N_{bits}}}, \quad (4)$$

where V_{FS} is the full scale voltage of the digitizer, N_{bits} are the effective number of bits. This can be converted into an equivalent noise temperature by dividing by the Nyquist bandwidth $f_s/2$, Boltzmann's constant k , and scaling by the total attenuation A to the reference plane to get,

$$T_{digi} = A \frac{P_{digi}}{k f_s/2}. \quad (5)$$

Using the measured in-flight median values for the BLAST-TNG 850 GHz array as a stand in for the PrimeCam 850GHz arrays, which are currently under development, we plot the noise temperature vs shift in linewidths in Fig. 1. The parameters used for Fig. 1 are: total quality factor $Q_r = 36000$, coupling quality factor $Q_c = 58300$, center resonant frequency $f_0 = 800$ MHz, $\text{NEP} = 10^{-16} \text{ W}/\sqrt{\text{Hz}}$, fractional frequency responsivity $dx/dP = 5.5 \times 10^{-6} \text{ x/pW}$, $V_{FS} = 0.7 \text{ V}$, $N_{bits} = 12$, attenuation from D/A to detectors $A = 35 \text{ dB}$, tone power at detectors $P_{tone} = -90 \text{ dBm}$, and a sampling frequency $f_s = 512 \text{ MHz}$. Figure 1 plots both components of the complex output noise temperature from Eq. 1 as Re and Im . In typical operation the complex signal is converted such that the response is mainly in one quadrature: the output noise temperature of the detectors is $\sim 40\text{K}$ in the Im quadrature on resonance. As the detector shifts away from its previous resonant frequency the output noise temperature decreases until falling to the level of the other contributors. LNA noise and D/A noise are approximately equal at the output of the detector arrays.

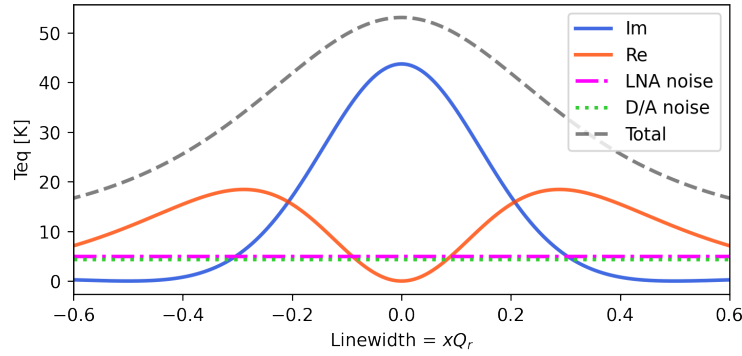


Figure 1. The effective noise temperature of the KID in both quadratures, LNA and D/A noise, plotted against the shift from resonance in multiples of a linewidth. The dashed grey line represents the total noise summing D/A, LNA, Re, and Im.

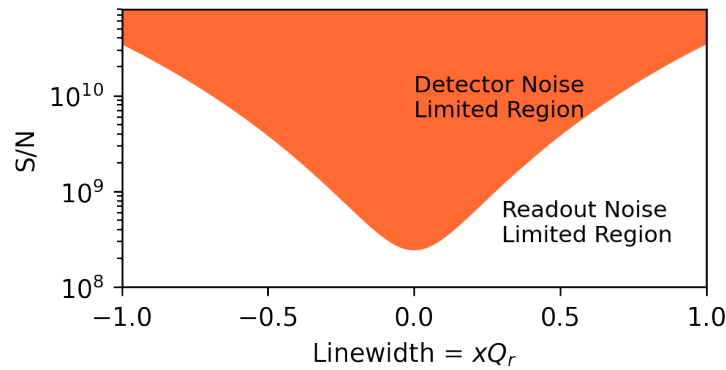


Figure 2. Signal to noise ratio from Eq. 6 measured at the output of the detector plotted against the shift from resonance in multiples of a linewidth. The solid orange section above the curve is considered the detector noise limited region and anything below or outside would be limited by the readout. For example if a readout system has a signal to noise of 100 dB (10^{10}) then it will be detector noise limited for shifts up to approximately $\sim 65\%$ of a linewidth.

To find the required dynamic range for the readout we must find the maximum signal to noise measured at the output of the detectors. This is calculated as the ratio of the bias tone power scaled by the detector transmission to the output detector noise power,

$$S/N = \frac{P_{tone}|S_{21}(x)|^2}{kT_{det}} = \frac{|S_{21}(x)|^2}{\left(\frac{dx}{dP} \left| \frac{dS_{21}(x)}{dx} \right| NEP\right)^2}. \quad (6)$$

The tone power drops out of the equation and the signal to noise is determined solely by properties of the detector. Plotting Eq. 6 as a function of linewidth with the same detector parameters from above produces the curve in Fig. 2. The minimum signal to noise measured at the output of the detectors occurs on resonance and increases further from this point. The readout systems dynamic range must be greater than the curve defined by Eq. 6 to not degrade the total signal to noise. Figure 2 shows that if the readout system has a measured dynamic range of 100 dB then detector noise limited performance is possible for shifts of up to $\sim 65\%$ of a linewidth. If the shifts are greater than that however, the signal to noise will become readout noise limited.

2.2 Channel Crosstalk

Kinetic inductance detectors suffer from electrical crosstalk when their frequency responses overlap. This is minimized by a combination of accurate frequency placement, high quality factors, and post-fabrication editing.^{61,62}

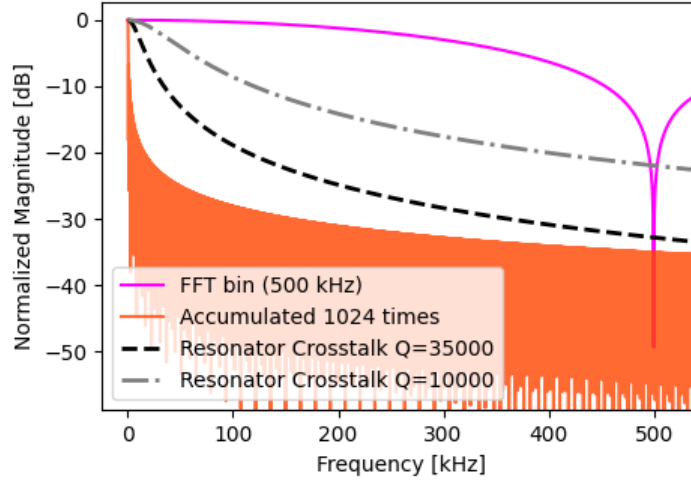


Figure 3. Accumulated spectrum with detector crosstalk for two different quality factors overlaid with the frequency response of the coarse and fine channelization (see Sec. 3.3.5).

We can calculate the overlap between two identical resonators which are frequency neighbors as,

$$X_{talk} = \frac{|S_{21}^n(f_0) - 1|^2}{|S_{21}(f_0) - 1|^2} = \frac{1}{1 + 4N^2}, \quad (7)$$

where S_{21}^n is the forward transmission of the neighboring resonator evaluated at the resonant frequency f_0 of the other and normalized by the on resonance transmission, N is the number of linewidths ($N = Q_r x$) of separation between the adjacent resonators. This electrical crosstalk takes place at the detector arrays and sets a fundamental requirement for the digital signal processing to meet. Figure 3 plots Eq. 7 for two different quality factors against the frequency response of the coarse and fine channelization stages within the gateway (see Sec. 3.3). The figure shows that a Fast Fourier Transform (FFT) based coarse channelization with a bin width of 500 KHz shown in magenta, does not meet the spec of both quality factors without an additional fine channelization stage. The frequency response of a fine channelization stage with 1024 accumulations is plotted in orange displaying sidelobes which fall below the intrinsic detector crosstalk for both quality factors. This suggests that for high rate applications such as pulse detection, side lobe minimizing windows or polyphase filterbanks would be necessary to keep channel leakage below the detector crosstalk levels.

3. BASELINE DESIGN

3.1 Overall architecture

The baseline design will use the Xilinx RFSoc which contains reconfigurable logic fabric, an ARM microprocessor (uPC), and high speed digitizers all integrated into a single chip. The first generation development board housing this chip (ZCU111) is the chosen platform for CCAT-prime due to its cost and familiarity from previous efforts by the author.^{54,63} The digital signal processing gateway which accomplishes the stimulus and demodulation of the detectors will sit in the reconfigurable fabric. The ARM uPC will run a lightweight version of Linux (petalinux) as an operating system. The software which directly interfaces the gateway and performs various array calibration tasks will reside on this ARM core. Many independently controlled RFSoc ZCU111 development boards will be operating simultaneously in the deployed system, with all communications occurring through an Ethernet network. A precision and stable time source will be distributed to each RFSoc to ensure pointing and detector data synchronization. The overall architecture can be roughly split into the following sections: hardware, gateway, uPC firmware, uPC software and networking, and analysis. A block diagram illustrating these systems and their general interconnections is shown in Fig. 4.

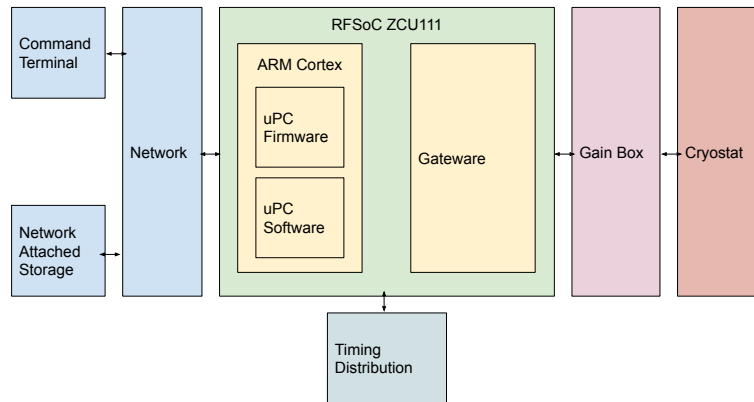


Figure 4. Block diagram of the overall readout architecture showing the main systems and interconnections between each.

3.2 Hardware

Most hardware components of the readout are commercially available but others require development including, an SMA breakout board for the ZCU111, a peripheral module sync board, and a rack-mountable enclosure. An optimized readout also depends on the cryogenic hardware such as the LNA, attenuators, and coaxial cables. The cryogenic attenuation to the arrays must reduce the room temperature thermal noise but not reduce the dynamic range of the tones produced by the D/A. The optimal cryogenic gain from the detectors to the A/D to prevent saturation should be balanced with available cooling power. See 56 for more information on this for Prime-Cam's 850 GHz instrument.

The ZCU111 development board and an SMA breakout board will be housed in a 1U rack-mountable enclosure with Ethernet, power, and SMA ports. Cerro Chajnantor has half an atmosphere of pressure and the instrument cabin will not be pressurized. This requires the RFSoc system to dissipate at high altitude without overheating. A method which was used for the balloon-borne project BLAST-TNG was to conduction cool with copper heat blocks with water filled heat pipes dumping the heat to the gondola frame. In this case the heat sink would be plates on the bottom of the enclosures and the electronics rack itself. Each enclosure will have 10 SMA ports (x8 for A/D and D/A, x1 for 10MHz reference, x1 for sync input), two 1GbE ports (x1 commanding, x1 streaming UDP detector packets), and one power port.

To allow for analog sync inputs to the FPGA fabric on the ZCU111, a small board which connects to the Peripheral Modules (PMOD) connector has been designed. The analog sync could come from a pulse-per-second of a GPS disciplined oscillator or halfwave plate or pointing sensor trigger. This signal would be digitized and incorporated with other timing signals such as free running counters and packets counters into the final data UDP packet.

Each RFSoc ZCU111 development board comes with the XM500 SMA breakout board, this has a variety of different connections in an effort to allow various use cases. However we would like to take the differential signals from the RF data converter pins and pass all of them through low frequency baluns (10 - 3000 MHz) to edge mounted SMA connectors. A prototype PCB of the new design is currently being tested.

3.3 Gateway

The gateway (FPGA firmware) is responsible for generating the detector array stimulus and producing demuxed, averaged, and downsampled detector data. The heritage for the design leans heavily on the design for BLAST-TNG,⁴⁴ and the pioneering designs of MAKO,²⁹ ARCONS,⁴³ and MUSIC.⁴² The digital signal processing chain consists of a lookup table which stores the frequency comb, two stage channelization accomplished with a polyphase-filterbank followed by a digital downconversion and accumulator. This section is split up between the different modules roughly outlined by the block diagram shown in Fig. 5.

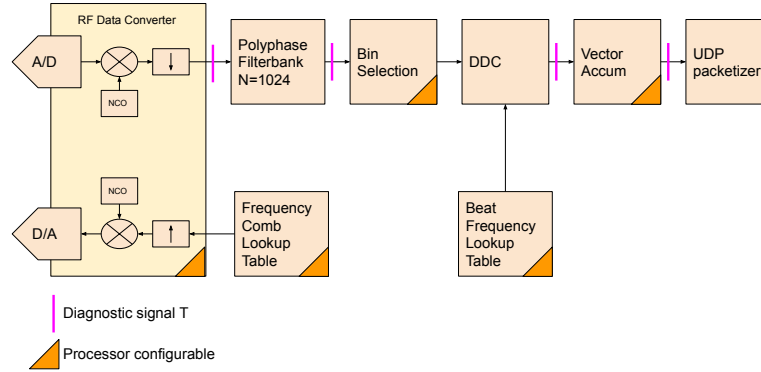


Figure 5. Block diagram of the digital signal processing gateway and connection to RF data converters implemented on the RFSoc programmable logic.

3.3.1 Frequency Comb Lookup Table

As the main stimulus for the detectors this part of the gateway design is closely linked to the array properties and their requirements. The frequency comb must be able to produce tones with high resolution that is significantly less than the resonator FWHM anywhere within the Nyquist bandwidth. Additional desirable features are quick re-writing of the waveform and to uniquely assign phase and amplitudes to each tone. To maximize the available D/A dynamic range the waveform crest factor and normalization method should be carefully constructed to not lose more than a typical OFDM peak-to-average power ratio of 12 dB.

The planned method of frequency comb generation is to utilize the programmable logic (PL) interfacing DDR4 memory. This is a large memory bank which operates at four times the PL fabric clock rate thus delivering four simultaneous samples. The initial reason for this choice is that in order to avoid spurious signals in the waveform we enforce phase continuity on the wrap around (meaning when the memory address to read goes from the maximum address to the minimum). A discontinuity in the time domain increases the spurious floor in the frequency domain. This can limit the dynamic range of the system and lower the mux factor. As an example, the baseline design has an effective Nyquist bandwidth of 512 MHz, and to generate a phase continuous waveform with a tone resolution of $\Delta f \sim 500\text{Hz}$ it would require a lookup table size of:

$$LUT = f_s / \Delta f \approx 1 \text{ Million.} \quad (8)$$

This is reasonable to place within the FPGA fabric for a single DSP chain but will not be when implementing four DSP chains. Therefore this must be placed in an external memory such as the PL connected DDR4.

3.3.2 RF Data Converter Configuration - Digital Mixers

The RF data converter in the Zynq UltraScale+ XCZU28DR-2FFVG1517E RFSoc⁶⁴ has a compile time configuration which allows for the use of internal digital mixers with a numerically controlled oscillator (NCO) as well as decimation and interpolation filters. This is shown as the RF Data Converter block at the front of the diagram in Fig. 5. The high speed sampling provide direct RF digitization without the need for analog mixers, eliminating the need for an intermediate-frequency (IF) system with analog mixers.

To understand how the RF data converters will be used in the baseline design, the three processing steps are shown in Fig. 6. In the first step starting on the left is the directly digitized Nyquist bandwidth of $f_s/2$. The orange block represents the band of interest that contains the resonators. Directly after digitization the signals get passed to the digital mixer with NCO. This NCO is tuned to match the center frequency of the band of interest thereby mixing the band center to DC, this is shown in the middle spectrum of the same figure. The mixer outputs a complex signal which is a combination of in-phase and quadrature complex signals which are then filtered and decimated, shown in the last figure as a factor of 2. This step is critical in that it allows us to pass only the required bandwidth through the FPGA gateway reducing the number of parallel paths and resource utilization. The same three steps are done in reverse for the generation of the frequency comb from the D/A.

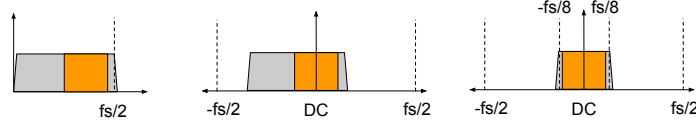


Figure 6. Three steps accomplished by the RF data converter for the A/D starting at the left and for the D/A starting from the right. The first spectrum is showing the Nyquist bandwidth from 0 to $f_s/2$ with some band of interest in orange. The second spectrum is post digital down-conversion to some frequency at the center of the band of interest accomplished with a numerically controlled oscillator (NCO). The third is the filtered and downsampled spectrum. In the reverse order, interpolation and up-conversion to the D/A.

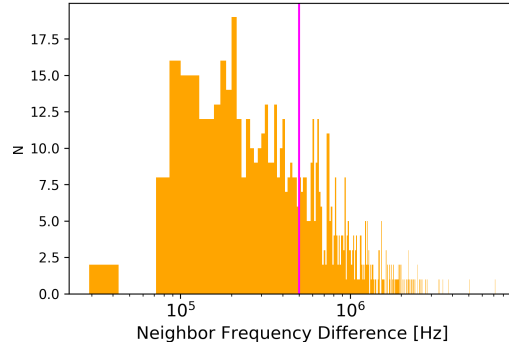


Figure 7. Neighboring resonator frequency difference from the BLAST-TNG $350\mu\text{m}$ array. The magenta vertical bar is at 500kHz which corresponds to the FFT bin width. Only 50.4% of the found resonators are above this line; about half of the resonators share an FFT bin.

3.3.3 Coarse Channelization

The first step in de-multiplexing is to perform an N -point Fast-Fourier Transform (FFT) which splits the input timestream into N channels of bandwidth f_{samp}/N , Where f_{samp} is the sampling rate post RF data converter. Each complex output from the FFT is considered a bin. The frequency response of a single FFT bin takes a sinc/x form with $x = \pi n$ where n is the ratio of sample rate and input frequency. This frequency response assures that the adjacent bin centers are zero at the cost of having a loss of signal at the bin edge and high side lobes. To prevent this loss and substantially lower the side band leakage many groups have employed the weighted overlap and add (WOLA) polyphase filter-bank (PFB). While the WOLA PFB recovers the bin edge attenuation and provides superior side lobe performance, its typical implementation requires significantly more resources than simple window functions. Earlier in Sec. 2.2 we showed that for lower bandwidth detector readout ($\sim 500\text{ Hz}$) that employs a fine channelization stage with many accumulations the frequency response of the coarse stage becomes insignificant. Future work will compare the PFB vs FFT baseline.

3.3.4 Bin Selection

The current frequency scatter for resonators with a 500MHz band centered at 750MHz assures that many will fall within the same bin ($\Delta f_{\text{bin}} = 500\text{kHz}$). A histogram of the difference between neighboring resonators from BLAST-TNG's $350\mu\text{m}$ array is shown in Fig. 7. The vertical magenta line is at 500kHz which corresponds to the FFT bin width and only 50.4% of the found resonators are above this line. Thus we require buffering the FFT bins to select the same bin multiple times. Post-FFT fine channelization can then be used to recover each resonator to maintain high detector yield. Future efforts to utilize post fabrication capacitor editing have the potential to eliminate the need for this module.

3.3.5 Fine Channelization

After the coarse channelization and bin selection we perform a fine channelization in two steps: digital down conversion, and vector accumulation. The first step is a time-division multiplexed complex multiply of an FFT

bin value with a pre-calculated waveform. This waveform is the complex conjugate of the beat frequency between a tone and its corresponding FFT bin center frequency,

$$(f_{beat})^* = e^{-2\pi i(f_{tone}-f_{bin})t}. \quad (9)$$

After this down conversion, the complex signal no longer oscillates due to this bin center offset and can now be coherently accumulated. If this step was not taken the signed values would accumulate quickly to zero.

The signals are then fed into a vector accumulator which accomplishes both an averaging and downsampling to reduce the output detector bandwidth. The number of accumulations can be programmed on the fly to allow for dynamic detector bandwidth sampling.

3.3.6 UDP packetizer

The integrated detector data is collected into a dual port memory which safely crosses a clock domain and then is passed to a UDP packetizer. User Datagram Protocol (UDP) is a lighter Ethernet packet protocol that does not handshake like TCP. This allows for reduced gateway complexity and high bandwidth Ethernet streams. An open-source VHDL implementation of a UDP streaming Media Access Controller (MAC) from Mike Field is used^{*}. The baseline design will use a four port 1GbE FMC card by Opsero/FMCEthernet[†] to simultaneously stream all four independent channels.

3.4 uPC Software and Network

A minimal implementation of the software and network architecture is shown in Fig. 8. The software and network must be discussed together as the commanding, diagnostics, and data capture are all occurring on different physical systems connected via an Ethernet network. Each RFSoc contains an ARM Cortex processor and will be configured to run the PYNQ image v2.6. The PYNQ image contains a Linux filesystem and a Python API to easily interact with the FPGA gateway and other hardware peripherals. Differing from the ROACH2 systems deployed in various instruments, the CCAT-prime readout takes advantage of the integrated microprocessors of each RFSoc. Each uPC acts as an independent computing node performing the majority of software computation and is provided with tasks from a command server, a model analogous to a distributed computing network. This method scales easily and eliminates the requirement of a high performance user terminal to perform the numerous computation tasks simultaneously. It also cuts down on the required data rate between the user terminal and each RFSoc. In normal operation only key value pairs will be needed to send command strings and status bits. Redis is an in-memory database and messaging service that uses TCP to send and receive messages in a server-client model. While written in C, Redis has Python bindings that are easy to integrate with the PYNQ framework. The built in messaging queue capabilities to publish and subscribe to various channels is ideal for commanding multiple RFSocs over the network. The implementation is discussed in detail below.

3.4.1 commander.py & drone.py

The two main Python programs implemented to control the readout are commander.py and drone.py. Commander.py runs on the user terminal and publishes commands to Redis, while drone.py runs as a Redis client and subscribes to the command channel and executes the received commands. This requires a command list to map the received key-value pair to a command.

Each RF network on the array will be controlled by an independent instance of drone.py. Each drone is given a unique designation that is linked to a DSP channel (1-4 in baseline) and RFSoc number in the server rack, these will eventually be mapped to detector array networks. The main functionality of drone.py is to execute commands received from subscribed Redis channels and publish status and exception flags. The required functions can be split broadly into two main files gateway.py and detector_functions.py. The first is dedicated to the calls that are directly interfacing with gateway on the FPGA for example reading and writing to registers with custom drivers utilizing the PYNQ library. The detector functions would contain most of the functionality specific to kinetic inductance detectors, such as creating frequency combs, find and fit resonances from sweeps, and calculate Δf .

^{*}https://github.com/hamsternz/FPGA_GigabitTx

[†]<https://opsero.com/product/ethernet-fmc/>

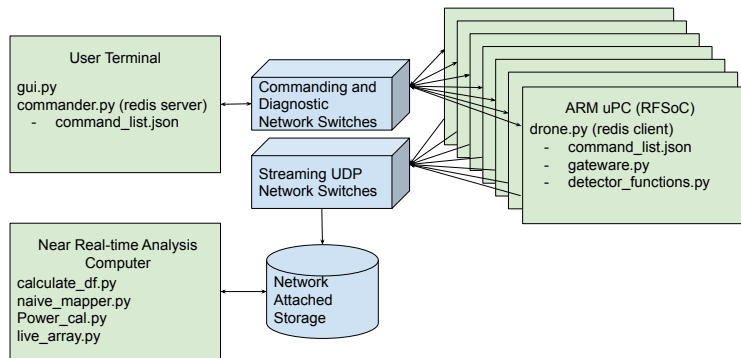


Figure 8. A block diagram of the software and network architecture for the CCAT-prime instrument. The software uses a server-client model where the user terminal acts as the server and each readout ARM uP is a client. The user command terminal is physically connected to each RFSoc via an Ethernet network. The commanding Ethernet network is separated from the streaming UDP packet network. The UDP data is saved to a network attached storage device which is accessible for near real-time analysis.

3.5 Analysis Software

Preliminary analysis software which provides useful data products and quick looks will be required for pre-deployment tests and commissioning. The first of which is to convert the raw in-phase and quadrature (I&Q) data streams to something proportional to power.

The shift in frequency is closely related to the power absorbed and is thus typically the metric to estimate. There are a few different methods for doing this and variations of each method: The IQ method which fits the resonance in the complex plane and moves its center to the origin and phase rotates such that the frequency response ends up in one quadrature. The change in signal can then be scaled by the derivatives of the loop with respect to frequency to convert the timestreams into a frequency shift. Another method finds the frequency shift assuming small perturbations from resonance which involves only taking derivatives of the complex sweep with respect to frequency, no fitting required, this is derived in 65. Typical implementations of these methods are linear approximations to the frequency shift and thus offer only limited range of shifts up to ~ 0.65 of a linewidth before accumulating an error of greater than 10%. An equation which computes the fractional frequency shift which follows the non-linear resonator response is,

$$x(t) = -\frac{Q(t)\sin\theta_0}{2Q_r(I(t)\cos\theta_0 - A)}, \quad (10)$$

where the un-modulated phase on resonance is $\theta_0 = \arctan(Q/I)|_{f_0}$, Q_r is the total quality factor, and A is resonator depth. This equation is found by inverting the resonator forward transmission Eq. 21(see appendix A.2). All three approaches will be explored in a future study.

A highly desirable goal of the time-domain science is to produce maps with a cadence of at least one day. While the maps do not need to be fully processed the important transient information must be easily detectable. The initial deployment data rate will be around 1 Gb/s which provides a challenging downstream processing task. A 10 GbE connected computer with a carefully planned memory access strategy and processing threads will serve as the analysis and storage computer. We will aim for an approach similar to 66 for nearly real-time processing to produce quick maps nightly.

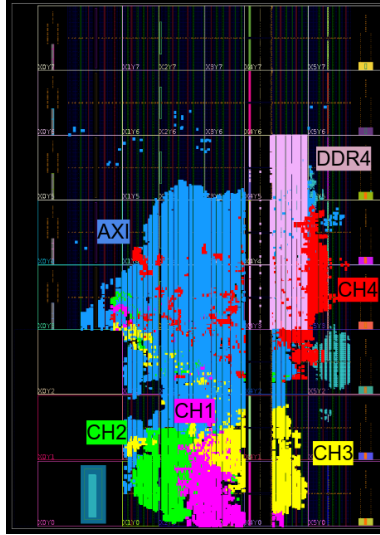


Figure 9. Resource utilization of the baseline design in device logic cell view. Implemented four x 1000 channel design on the Zynq UltraScale+ ZCU28DR - with the four independent channels highlighted along with the DDR4 memory and AXI interconnects.

4. IMPLEMENTATION AND RESOURCE UTILIZATION

An important consideration when developing any digital design for an FPGA is the resource utilization in comparison to the resources available. The four channel baseline design was synthesised and implemented on the gen 1 RFSoc providing the following utilization report: CLB LUTs 22%, CLB Regs 18%, DSPs 6%, Block RAM 17%, URAM 10 %. This is visually represented in Fig. 9 in a logic fabric view of the chip. Each channel is highlighted along with the AXI interconnects and DDR4 memory bank. Two things are immediately apparent from this visual representation: the AXI interconnects are taking a significant area of the fabric, and there is appears to be ample room to grow in the north west region of the fabric. The utilization report numbers support the visual assessment and provide encouraging proof that a doubling of the instantaneous bandwidth from 500 MHz to 1 GHz should be possible.

Upon closer examination into the resource utilization of a single channel we see that the PFB dominates the fabric area. Figure 10 gives the device fabric view of the four channel design with only a single channel highlighted in magenta and yellow. The yellow highlights solely the PFB resources and the magenta highlights the remaining parts of the channel. The utilization report of the PFB gives: 4303 CLB LUTs, 9844 CLB Registers, 675 CARRY8, 1407 CLB, 3375 LUTs as Logic, 928 LUTs as Memory, 27.5 Block RAM Tiles, and 52 DSPs. From the analysis of the digital crosstalk requirements described earlier in Sec. 2.2, the front end filterbank may not be necessary given the high number of accumulations in the fine channelization and expected resonator crosstalk level. This will allow for larger FFTs within the resource budget.

5. DEMONSTRATIONS

The baseline design was set up in RF loopback with an SMA cable connecting a D/A to it's corresponding A/D. One thousand tones spanning -250 to 250 MHz at baseband (pre-mixer) were generated and up-converted to 750 - 1250 MHz with the numerically controlled local oscillator (NCLO) within the digital mixer set to 1 GHz. On the receive side after being sampled by the A/D the waveform is down-converted to baseband by another NCLO set to 1 GHz. Each tone is assumed to be an independent detector channel and is demodulated and accumulated within the digital signal processing chain. The output of the last stage of the signal processing is captured and displayed in Fig. 11. All one thousand channels are shown and the plot is normalized to the maximum. A frequency dependent slope is seen in the magnitudes and a roll-off on both ends of the band. The roll-off is suspected to arise from the half-band up and down sampling filters frequency response within the RF

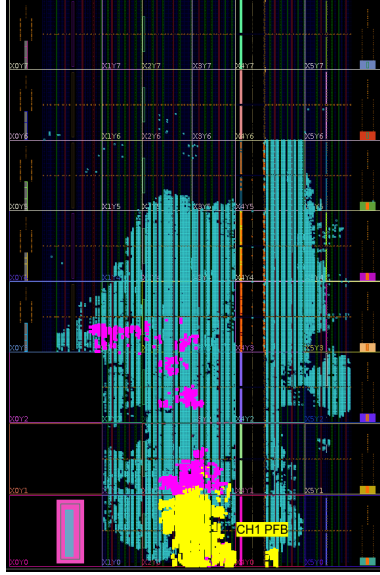


Figure 10. Device view of the resource utilization with only channel 1 highlighted in magenta and yellow. The yellow highlights the resources used solely for the polyphase filterbank (PFB). The remaining magenta elements are the rest of the resources used for channel 1. Clearly the fabric area covered by the PFB dominates the utilization of the channel.

data converters. Digital leveling can be achieved by applying the inverse transfer function to the amplitudes of the tones in the arbitrary waveform.

To characterize the dynamic range and phase noise a loopback measurement was made with a single chain of the design. The I&Q for each detector channel are streamed in UDP packets and captured for two minutes with a sample rate of ~ 500 Hz. The phase noise power spectral density is then calculated on the time-stream either by first calculating the phase time-stream with $\phi = \arctan(Q/I)$ then finding the power spectral density, or by first calculating the power spectral density of I&Q separately (S_{II} and S_{QQ}) then using the following equation,

$$S_{\phi\phi} = \frac{1}{2} \frac{S_{II} + S_{QQ}}{\bar{I}^2 + \bar{Q}^2}, \quad (11)$$

Where the sum of the power spectral densities are normalized by the mean magnitude squared. Figure 12 shows the loopback phase noise power spectral density in dBc/Hz for various numbers of tones in the arbitrary waveform and presents the median detector channel from each. A common mode present across each channel was removed with a single template produced with a principle component analysis. The inverse of the phase noise power spectral density is the maximum possible signal to noise or dynamic range achievable for that channel and specific arbitrary waveform. For 1000 tones this system will be detector noise limited for shifts of up to $\sim 3/4$ of a linewidth based on Fig. 2.

6. CONCLUSION

The RFSoc based readout for the Mod-Cam and Prime-Cam instruments was presented. The requirements were derived from expected detector parameters. The hardware, gateway, and software of the baseline design were described in detail. The implementation and resource utilization for the design proved that 4x 1000 channel design fit comfortably within the device fabric. This also revealed that there is space to increase the bandwidth for the 850 GHz instrument. We demonstrated the operation of the design in RF loopback showing that the digital mixers can replace analog IQ mixers and that the phase noise is low enough with 1000 tones to ensure detector noise limited performance for the anticipated operational range. In the near term, we expect to have an 850 GHz prototype array in our test cryostat at NRC Herzberg to inform the optimization of all aspects of the RFSoc based system. The first field deployment of the RFSoc readout will be with the Mod-Cam instrument in 2024.

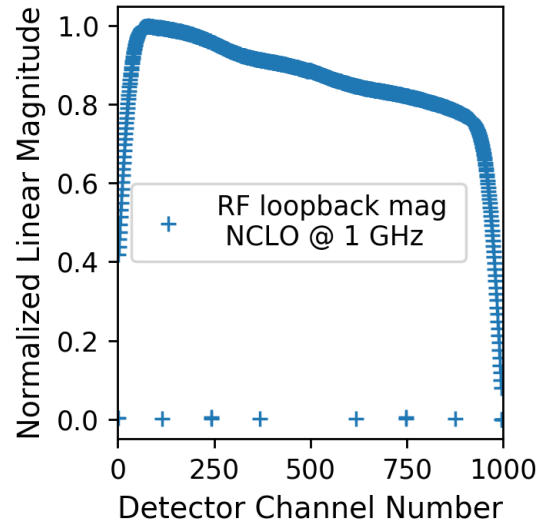


Figure 11. RF loopback measurement with the numerically controlled local oscillator (NCLO) set to 1GHz and a 1000 tone comb.

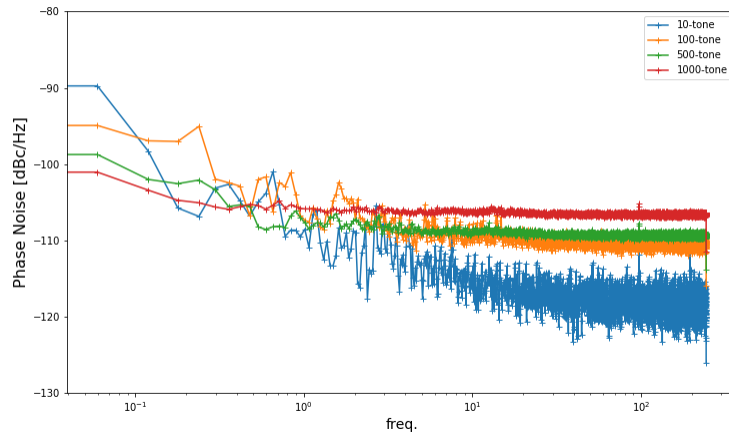


Figure 12. RF loopback phase noise measurement for various numbers of tones with a common mode removed.

APPENDIX A. DERIVATIONS

A.1 Equivalent Output Noise Temperature

Starting with the equation for the complex transmission of an LRC resonator,⁵⁸

$$S_{21}(f) = 1 - \frac{Q_r}{Q_c} \frac{1}{1 + j2Q_r(f - f_0)/f_0}, \quad (12)$$

Where f is frequency, f_0 is the resonant frequency, Q_r is the total quality factor, Q_c is the coupling quality factor. Rewriting the fractional frequency as $(f - f_0)/f_0 = x$ and splitting the above equation into real and imaginary components we get,

$$\text{Re}\{S_{21}\} = 1 - \frac{Q_r}{Q_c(1 + 4Q_r^2x^2)}, \quad (13)$$

and

$$\text{Im}\{S_{21}\} = -\frac{2Q_r^2x}{Q_c(1 + 4Q_r^2x^2)}. \quad (14)$$

Taking the derivative of each with respect to fractional frequency x ,

$$\frac{d\text{Re}\{S_{21}\}}{dx} = \frac{8Q_r^3x}{Q_c(1+4Q_r^2x^2)^2}, \quad (15)$$

$$\frac{d\text{Im}\{S_{21}\}}{dx} = \frac{2Q_r^2}{Q_c(1+4Q_r^2x^2)} - \frac{16Q_r^4x^2}{Q_c(1+4Q_r^2x^2)^2}. \quad (16)$$

In typical operation the measured output voltage depends on the probe tone input voltage and the forward transmission,

$$V_{out} = V_{in}S_{21}(x). \quad (17)$$

The absorption of optical photons will shift the resonant frequency modulating the transmission. Taking the derivative of the above equation to find the change in output voltage with respect to absorbed optical power or voltage responsivity,

$$\frac{dV_{out}}{dP} = V_{in} \frac{dS_{21}}{dP} = V_{in} \frac{dS_{21}}{dx} \frac{dx}{dP}. \quad (18)$$

Expanding the complex terms,

$$\frac{dV_{out}}{dP} = V_{in} \frac{dx}{dP} \left(\frac{d\text{Re}\{S_{21}\}}{dx} + j \frac{d\text{Im}\{S_{21}\}}{dx} \right). \quad (19)$$

Following⁵⁷ we can then calculate the noise temperature as,

$$T = \frac{(R \times NEP)^2}{kZ_0}, \quad (20)$$

where NEP is the detectors noise equivalent power, k is boltzmann's constant, Z_0 is the characteristic impedance, and $R = dV_{out}/dP$ is the voltage responsivity.

A.2 Fractional Frequency Shift by Inverse Method

The equation for the complex forward transmission of a shunt resonator is,

$$S_{21} = 1 - \frac{Q_r}{Q_c} \frac{1}{1 + j2Q_r(f - f_0)/f_0}, \quad (21)$$

Where Q_r is the total quality factor, Q_c is the coupling quality factor, f_0 is the unmodulated resonant frequency. The term $(f - f_0)/f_0$ is the fractional frequency shift commonly written as x . The fractional frequency shift x can be directly related to the power absorbed through measurements of the responsivity. Fixed tone readout systems estimate this value by measuring the instantaneous complex forward transmission at the unmodulated resonant frequency f_0 . These complex values are named the in-phase I and quadrature Q components of the transmission,

$$S_{21}(f_0) = \text{Re}\{S_{21}(f_0)\} + j\text{Im}\{S_{21}(f_0)\} = I(t) + jQ(t). \quad (22)$$

We seek an equation which gives the fractional frequency x with the measured I/Q signals as an input. This requires inverting Eq. 21 and using above relation to I/Q.

Equation 21 can be split into real and imaginary components as,

$$S_{21} = 1 - \frac{Q_r}{Q_c(1+4Q_r^2x^2)} + j \frac{2Q_r^2x}{Q_c(1+4Q_r^2x^2)}. \quad (23)$$

This makes it easier to see that subtracting 1 from the real term and dividing by the imaginary term simplifies the equation to,

$$\frac{\text{Re}\{S_{21}\} - 1}{\text{Im}\{S_{21}\}} = -\frac{1}{2Q_rx}. \quad (24)$$

Now using the relation from Eq. 22 and solving for x ,

$$x = -\frac{Q(t)}{2Q_r(I(t) - 1)}. \quad (25)$$

This equation assumes that a shift in resonant frequency is equivalent to a shift of stimulus tone frequency in the opposite direction. It's also an idealized symmetric resonator which has been normalized and phase rotated such that the imaginary component on resonance is zero.

In practice the resonator measurements have some arbitrary magnitude scaling and phase rotation angle. Including these effects the fractional frequency shift equation becomes,

$$x = -\frac{Q(t)\sin\theta_0}{2Q_r(I(t)\cos\theta_0 - A)}. \quad (26)$$

Where A is the resonator depth, θ_0 is the phase angle at the resonant frequency f_0 found from $\theta_0 = \arctan(Q/I)$.

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