High on/off ratio SiO_2-based memristors for neuromorphic computing: Understanding the switching mechanisms through theoretical and electrochemical aspects

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Keywords: memristor, switching mechanism, oxygen vacancy, finite element analysis, electrochemical impedance spectroscopy, neuromorphic computing

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Abstract

Memristors have emerged as promising elements for brain-inspired computing applications, yet the understanding of their switching mechanisms, particularly in valence change memristors, remains a topic of ongoing debate. We report on the CMOS-compatible SiO_2-based memristors, demonstrating a high on/off ratio ($> 10^5$). Particularly, this study aims to enhance the fundamental understanding of switching behaviors and mechanisms. Our approach involved an extensive investigation using finite element analysis to provide visual insights into the conductive path evolution in these memristors over the set/reset bias cycle. Electrochemical impedance spectroscopy experimentally validated the theoretical investigations by interpreting the switching behavior through the lens of the equivalent circuit. In addition, we evaluated synaptic characteristics and incorporated them into neural networks for image recognition tasks with MNIST and Fashion MNIST datasets. Our comprehensive exploration of both the underlying principles and potential applications is of practical relevance to studies that aim to realize and implement CMOS-compatible SiO_2-based memristors in neuromorphic computing.

INTRODUCTION

The silicon (Si) microelectronics research and industry promisingly consider memristors a promising contender in emerging memory technologies. This increasing interest is attributed to the potential performance advantages of memristors, including fast switching responses[1], high scalability[2], and the unique capability of updating multi-conductance levels[3]. These distinct characteristics of memristors position them as a compelling choice for implementing in-memory computing, offering a path to challenge and potentially revolutionize traditional Von Neumann architectures.

A wide range of oxide materials, from semiconductors to *high-k* materials, including InGaZnO[4], SiO_2[5, 6], HfO_2[7], TaO_x[8] have been reported to serve as switching layers in memristors. The majority of materials utilized in memristors are either expensive to grow or only partially compatible with the prevalent Si-based complementary metal-oxide semiconductor (CMOS) manufacturing process. Historically, SiO_2 has been one of the most extensively researched dielectric materials, largely due to its direct growth capability out of Si.[9] However, much of this research has been centered around the destructive and irreversible dielectric breakdown for traditional CMOS and very large-scale integration (VLSI) technologies.[10] Recently, a shift in focus has been noted within the memristor field, as SiO_2 has demonstrated reversible soft breakdown behaviors, also known as resistive switching.[5, 6] This, coupled with its full compatibility with current CMOS manufacturing, has prompted an increase in interest and research into the potential applications of SiO_2 within the realm of memristor technologies. Memristors based on SiO_2 have been investigated and reported with an achieved performance of on/off ratio of 10^2-10^4.[5, 11] Bilayer structure ($SrTiO_3$/SiO_2[12]) was demonstrated for realizing stable switching through engineering different ion transport rates in these two layers where the

role of SrTiO3 is to confine filament growth. Nanorods of SiO_2 were also investigated to lower the firing energy for an artificial neuron.[13] However, further advancement of SiO_2-based CMOS-compatible memristors is technologically limited due to issues such as large variation in SET/RESET voltages[14], unsatisfactory endurance and retention properties, and sensitivity to the moisture ambient[15]. Therefore, it is crucial to fundamentally understand SiO_2-based memristors' switching mechanisms, which in turn will provide insightful engineering criteria to address the challenging issues above. Thus far, the oxidation-reduction (redox)-based switching mechanisms have been suggested and categorized into two mechanisms, depending on the composition of the conductive filaments: electrochemical metallization mechanism (ECM) and vacancy-associated valence change mechanism (VCM). In an ECM device, Cu or Ag is widely chosen as an active electrode which can be partially oxidized and then reduced to form the metallic filaments.[16] On the other hand, the conductive path of VCM devices relies on the generation and accumulation of oxygen vacancies. [17] A phase change mechanism (PCM) has been also suggested as the third mechanism, where the switching process depends on the amorphous/crystallization transformation of the switching layer that is triggered by Joule heating.[18, 19] The evolution of conductive filaments in the ECM and PCM memristors have been evidenced through transmission electron microscope (TEM)[20], and these work enhanced understanding of the switching behavior of ECM and PCM memristors. [17] However, the direct visualization of conductive filaments in VCM based memristors are rarely reported due to the technical difficulties, for example in TEM characterizations, of low image contrast between oxygen-rich and -deficient regions in TEM characterizations, which makes the VCM switching mechanism remain controversial.[21, 22]

In this work, we selected SiO_2 as the switching element for CMOS-compatible memristor applications. To solely limit the contributing charged carriers to oxygen vacancies for the switching behavior, an inert metal Pd was employed as the top electrode. The dynamic evolution of oxygen vacancy conductive filaments in the SiO_2-based memristors was mechanistically visualized by a numerical solver, which delineates a selective growth process and the inhibition effect exerted on filaments nearby the established dominant paths. The equivalent circuit interpretation from non-destructive electrochemical impedance spectroscopy (EIS) measurements supplementarily corroborated our theoretical understanding about switching mechanism. Importantly, our SiO_2-based memristor can be considered as an electronics synapse in terms of structure, and furthermore, exhibited multi-conductance phenomena in response to pulse train stimuli. Given these synaptic characteristics, our SiO_2-based memristors were incorporated into a neural network for image processing tasks, benchmarking with MNIST and Fashion MNIST datasets. Our fundamental studies and concept validation may propel advances in CMOS-compatible SiO_2-based memristors, pushing the boundaries towards real-world neuromorphic computing applications.

RESULTS AND DISCUSSION

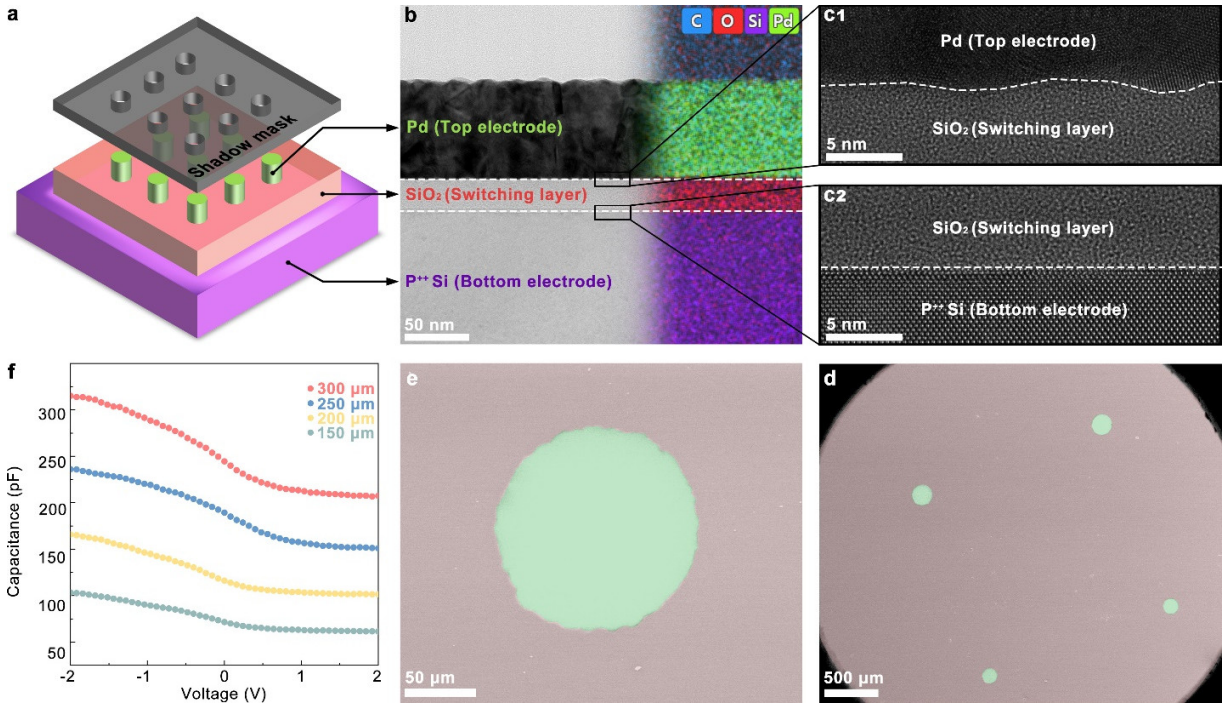

Figure 1. Pd/SiO_2/P^{++}Si memristors: (a) Schematic illustration of device structure of SiO_2 based memristor with Pd TE and heavily-doped Si BE. (b) A false-colored cross-sectional HAADF–TEM micrograph, and associated EDS elemental mapping of an Pd/SiO2/P^{++}Si memristor. (c) High resolution TEM images to reveal the morphology of (c1) the TE/SiO_2 interface, showing ~1 nm protrusions and (c2) the flat SiO_2/BE interface. (d) A false-colored SEM plan-view image of the top electrodes with diameters of 200 µm and 150 µm, and (e) An extended image for the typical size 150 µm. (f) C-V measurements at 1 MHz for 5 nm-thick SiO_2 based memristor with various TE sizes (300, 250, 200 and 150 µm).

Figure 1a is a schematic illustration of a SiO_2 based memristor in a vertical configuration. The top electrodes were defined using *in-situ* shadow masks during the fabrication, of which the circular pattern diameters vary from 150 to 300 µm with a 50 µm increment. A cross-sectional high-angle-annular dark-field (HAADF) TEM micrograph of the SiO_2 memristor is false colored and exhibited in Figure 1b. A vertical memristor structure consisting of top (Pd, ~100 nm) and bottom (heavily-doped Si) electrodes and switching layer (SiO_2, ~20 nm) between the electrodes was clearly identified. An associated energy-dispersive X-Ray spectroscopy (EDS) mapping

image in Figure 1b indicates the major elements of each layer of the memristor, indicating clear interface between layers without interdiffusion. In the high-resolution TEM images (Figure 1c), distinct morphological features are evident: the TE/SiO_2 interface exhibits protrusions approximately 1 nm in size (Figure 1c1), while the SiO_2/BE interface is characterized by a notably flat surface (Figure 1c2). A false-colored SEM image of the Pd top electrodes with diameters of 200 and 150 μm is displayed in Figure 1d and a magnified image of a 150 μm Pd top electrode is shown in Figure 1e. The typical vertical memristor structure is technically the same as that of a capacitor and particularly the characteristics of the high-resistance state are governed by the dielectric performance of the switching layer (SiO_2 in this study). To evaluate the dielectric property, as an initial figure of merit, of the switching layer and the devices, capacitance-voltage (CV) measurements were conducted on SiO_2-based memristors as a function of switching layer thicknesses and top electrode size within a voltage range from -2V to 2V under 1MHz. The CV results from the 5 nm SiO_2 switching layer are summarized in Figure 1f and those of other thicknesses, ranging from 10 nm to 30 nm can be found in Figure S1. Overall, the capacitance of 5nm SiO_2 based memristors is at 10^{-10} F level. With scaling down the top electrode dimension, the capacitances were decreasing in Figure 1f, which is aligned with the capacitance relation, $C = \varepsilon_0 \varepsilon_r \frac{A}{d}$,where C is capacitance, A is the electrode area, d is the distance between conductive plates, ε_0 is vacuum permittivity and ε_r is relative permittivity (also referred to as dielectric constant). From the C-V measurements, the capacitance densities of the SiO_2 switching layers with different TE sizes are comparable to each other, approximately 3.5-4.2 fF/μm^2. The relative permittivity extracted from the resulting sputtered SiO_2 is 3.3, which is close to the reference values 3.7-3.9.[23] The slightly lower value may be resulted from the room

temperature sputtering condition and mild annealing temperature (550 °C), compared with the reference values obtained from high temperature (1000-1200 °C) thermal oxidation.

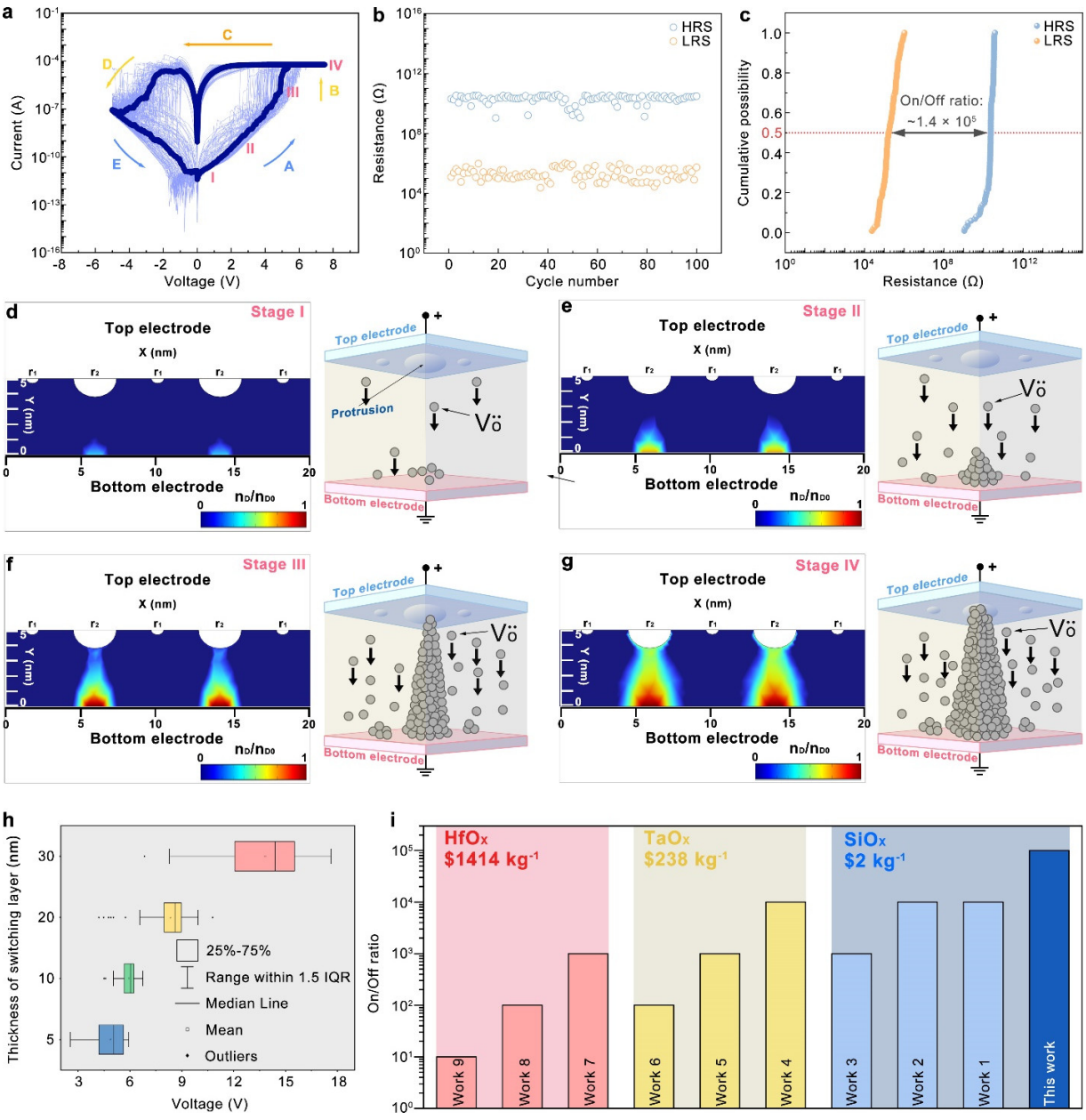

Figure 2. (a) I–V characteristics of the Pd/SiO_2 (5 nm)/P^{++}-Si memristor in semi-log scale, where arrows, labeled in alphabetical order, indicate HRS, SET, LRS, RESET, and HRS, respectively. (b) Endurance graph for 100 cycles, a high on/off ratio, $>10^5$ is observed, without damping. The resistance values at HRS and LRS are recorded at a read voltage of 0.3 V. (c) Statistical distribution of resistance at HRS and LRS, from which the on/off ratio is extracted to be $\sim 1.4\times10^5$ at a cumulative possibility of 50 %. The FEA visualization and schematic elaboration

for the evolution of conductive filaments at (d) stage I, where small positive bias for DC sweeping is initially introduced on TE of the device, positively charged oxygen vacancies ($Vo^{\bullet\bullet}$) are migrating towards BE; (e) stage II, where the magnitude of sweeping DC voltage is increasing, oxygen vacancies start accumulating at BE; (f) stage III, with voltage increasing continuously, the conductive filaments are growing; (g) stage IV, after a SET voltage applied, the conductive filaments are connecting the bottom and top electrodes, where the protrusion radii are r_1 = 0.3 nm, r_2 = 1.2 nm. (h) Statistical distribution SET voltages for different thicknesses of SiO_2 switching layers. (i) Comparison of the on/off ratio of the present study with those from the literature.

The electrical characteristics of SiO_2 based memristors were examined by cyclic DC sweeping. The electrical biases were always applied on palladium top electrode and the P^{++} Si bottom electrode was grounded. The sweeping bias ranged from -5 V to 7.5 V with a starting voltage of 0 V, and a compliance current (I_{cc}) was set at 60 μA during the positive sweeping. Figure 2a shows the current−voltage (I−V) property of a 5nm-SiO_2 switching layer memristor, including consecutive 100 cycles of DC sweeping curves with the same measurement parameters. The I-V sweeping curves appear as a butterfly shape which is a typical pattern for a bipolar memristor.[21] The bipolar switching resulted from the formation (with positive biases) and annihilation (with negative biases) of filament, caused by field induced oxygen vacancy migration with alternating opposite directions of bias application.[18] This is different from the unipolar switching which has been proposed, where the annihilation of the filament is achieved by Joule heating using a consistent bias direction.[24] When the bias increased from 0V to 7.5 V, abrupt current jumps were observed which indicates a conduction filamentary SET process, i.e., a transition from high resistance state (HRS) to low resistance state (LRS). And the transitions (turn on) mostly happened at a voltage ranging from 4V to 6V. The LRS was maintained during the sweeping from 7.5 V to 0V and subsequent 0V to negative bias. It should be noted that the turn-on voltage of the first cycle of DC sweeping was ~6V which was applied on the top electrode (Pd). From the SET voltage statistics distribution in Figure 2h (bottom for 5 nm thick SiO_2), it is on the

maximum side, but not too far from the medium/mean value of ~5 V. Thus, we can consider our device to be a near-forming free device, which is defined as the initial SET voltage of the device is similar to the subsequent SET voltages.[25] During the negative voltage sweeping, a current level drop was observed which means the cell was turned back to HRS, a RESET process was finished (i.e., off state). The current values at read voltage of 0.3 V for each sweeping cycle were extracted from the I-V curves, then converted to resistance values and plotted as resistance verse cycle number to yield the endurance performance of the device exhibited in Figure 2b. The results demonstrate that no deterioration in HRS and LRS during continuous cycling was observed, indicating reasonable endurance of the SiO_2-based memristor. A large memory window, i.e., on/off ratio, is clearly observed as high as $>10^5$. To characterize the on/off ratio more quantitatively, the cycle-to-cycle statistical distributions of HRS and LRS are demonstrated in Figure 2c. At the cumulative probability of 50%, the notable high on/off ratio is further validated as $\sim 1.4\times10^5$. The achieved high on/off ratios are attributed to the low off-state current and the high on-state current. The low off-state current behavior mainly depends on the intrinsic quality of the switching layer (i.e., dielectric property). As the capacitance-voltage characteristics are provided in Figure 1f, our sputter-processed SiO_2, followed by air annealing, demonstrates decent dielectric performance, comparable (or slightly less) to bulk and thermally grown SiO_2. Therefore, our SiO_2-based memristor achieved an off-sate current as low as on the order of 10^{-11} - 10^{-10} A. For the on-state behavior, various parameters are related to the overall on-state property, such as the intrinsic characteristics of the switching layer, thickness, and the transport behavior of the charged carriers (oxygen vacancy in this case), and hence the resulting conductivity of the filament. In addition to these intrinsic and processing parameters of the materials and device, a measurement parameter of the compliance current (I_{cc}) is also an

important factor in determining the on/off ratio, as it limits the maximum current flowing through the device. This not only prevents the device from experiencing a hard breakdown but is also proposed to control filament growth.[26] With I_{cc}= 60 μA in our study, the conduction filament, once formed, has sufficient conductivity (Figure S2) to achieve a relatively high on-current, thereby exhibiting resistive behavior. Furthermore, the regulated filament can be near-fully ruptured during the RESET process to get the low current again, contributing to the high on/off ratio.[27] In regard to the device-to-device variation, all the processing parameters and annealing environment are carefully controlled and monitored for the processing of our SiO_2 memristors, to minimize any processing variations and hence the possible performance variations. The performance of our SiO_2-based memristors slightly varies among the devices and particularly the on/off ratio is found to be reasonably consistent as shown in Figure S3, demonstrating 0.9-1.6 × 10^5. Additionally, the SET voltage exhibits very small device-to-device variation of 2.90% (Figure S4). To assess the stability of our device, the retention characteristics were evaluated with a read voltage 0.3 V at evaluated temperature 85 °C. As depicted in Figure S5, both the LRS and HRS show a prolonged retention time of 10^4 seconds. This evidence, in conjunction with previous endurance tests, underscores the reasonable reliability of our device. In order to enhance the fundamentals of the switching process through the evolution and rupture of an oxygen vacancy-based conduction filament as well as to complement the macroscale electrical and electrochemical measurements, we performed a series of FEA analysis as a function of applied bias. The physical modeling details are elaborated in Note S1, Supporting Information. It should be noted that the switching behavior the memristor in this study is governed by oxygen vacancies (i.e., VCM) due to the inert Pd (TE) and stably covalent-bonded Si (BE), which indicates that no electrode-related ions are involved in the conduction. A

Multiphysics-fields coupled model, which describes the diffusion and drift flux of the $V_O^{\bullet\bullet}$ at the nanoscale, was adopted to study the switching process of the memristor. Several protrusions at the top electrode with various radii (r_1 = 0.3 nm, r_2 =1.2 nm) were considered to reflect the roughness of the TE/SiO_2 interface (Figure 1c1). There is no chemical or structural difference between protrusions and top electrode Pd. In Figure 2d-g, the overall intensity of n_D/n_{D0} (concentration ratio of [$V_O^{\bullet\bullet}$] at current stage to [$V_O^{\bullet\bullet}$] at original stage) gradually increased from stage I to stage IV over the course of SET process, indicating the concentration of $V_O^{\bullet\bullet}$ was augmented in the turn-on process with increasing bias. Compared with the flat region and small protrusions on the top electrode, the protrusions with the larger radius have higher concentrations of $V_O^{\bullet\bullet}$, and exhibit a higher intensity of n_D/n_{D0}, which suggests that the $V_O^{\bullet\bullet}$ is preferentially concentrated at larger protrusions. This concentration difference can be explained by the variation in the electric field, induced by the intrinsic roughness of the TE/SiO_2 interface. The significantly enhanced localized electric field under the large protrusion, as confirmed in Figure S6, tends to attract more $V_O^{\bullet\bullet}$ to regions under the protrusions with larger radius.[28] Thus, our FEA analysis indicates that the selectively distributed $V_O^{\bullet\bullet}$ may limit the random growth of the conduction filaments. This provides an insight for engineering memristors that implementing well defined protrusions may mitigate the issue regarding performance variation of memristors. The bright regions under larger protrusions at stage IV became redder and wider compared with stage III, which implies that the formed conduction filament would grow thicker. Associated schematics at each stage that elaborate the SET process are also shown on the right of our simulation results. When a positive bias is applied to the Pd TE, oxygen ions (O^{2-}) are pulled away from the switching matrix by the external field, migrating towards the Pd TE.[29] This leads to the simultaneous generation of positively charged oxygen vacancies ($V_O^{\bullet\bullet}$). In general, this

process is often described by the motion of the corresponding oxygen vacancies, i.e., the positively charged oxygen vacancies migrate towards the grounding BE and subsequently accumulate there, forming a conductive filament that bridges the TE and BE.[30] Upon arriving at the Pd TE, the oxygen ions are oxidized to O_2 and accumulate around the TE/SiO_2 interface.[21, 31] To evaluate the effect of the thickness of SiO_2 layer, similar electrical characterizations were also carried out on 10 nm, 20 nm and 30 nm SiO_2 switching layer memristors. The I-V characteristics for these switching layer thicknesses can be found in Figure S7 (Supporting Information). It is observable that devices with thicker switching layers require a higher voltage for stable resistive switching. The SET voltages are statistically summarized in Figure 2h. A clear quantitative trend is confirmed, indicating that SET voltage increases with the thickness of the switching layer. The difference in SET voltage between the 5nm and 30nm SiO_2 devices is approximately 9 V. From a practical perspective, thinner SiO_2-based memristors offer higher energy efficiency. The models with associated thicknesses of the switching layer were simulated as well (Figure S8-10, Supporting Information). The calculated results are consistent with the model with the SiO_2 layer of 5 nm except for the turn-on voltage applied to the top electrode was increased which was led by the thicker SiO_2 layer in the models.

Figure 2i compares the on/off ratio of the present study with those available in the literature. For objective comparisons, other two widely-considered oxides of TaO_x (as Work 4[32], 5[33], and 6[34]) and HfO_x (as Work 7[35],8[36], and 9[37]) are also included in Figure 2i as well as SiO_x (as Work 1[38], 2[39], and 3[40]). The achieved on/off ratio of $>10^5$ from our SiO_2 memristors outperforms those ($\sim10^1$-10^4) of state-of-the-art HfO_x- and TaO_x-based memristors. In addition to the on/off performance, the unit price of these switching materials is also compared. Due to the abundance, SiO_2 is significantly cost-effective (100-700 times lower) than the other competitors.[41] In order

to make our comparison more comprehensive, we compared the endurance and retention in our work with those in other literature. The comparisons are presented in Table S1, where our device exhibits reasonable reliability, in terms of both endurance and retention, demonstrating on the order of 10^2 cycles and 10^4 s. The repeated DC sweeping at low voltage regime was also examined on SiO_2 based memristors and gradual switching was observed in Figure S11 which is a promising indicator for obtaining subsequent synaptic characteristics with pulse measurements.

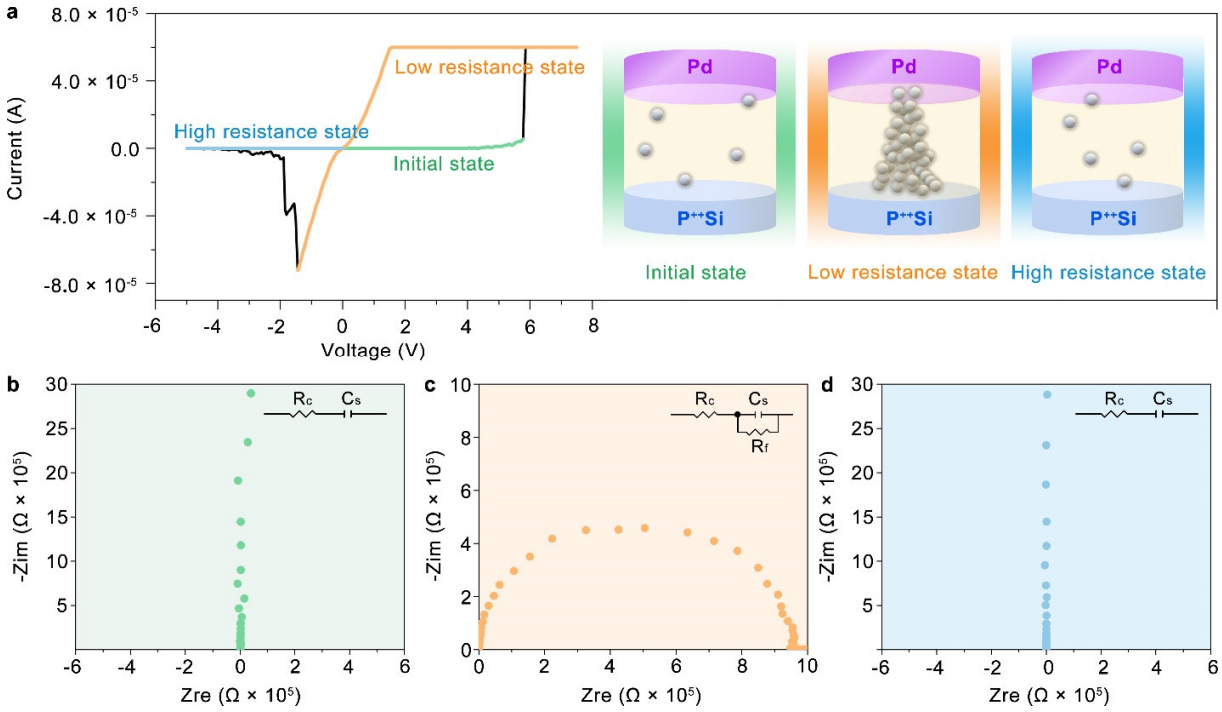

Figure 3. (a) A typical cycle of I-V characteristics from 5nm SiO_2-based memristors is shown in a linear-linear scale. The initial HRS, LRS (SET), and HRS (RESET) are colored with green, orange, and blue, sequentially. These three states are schematically explained on the right: the initial HRS of the device has a small number of intrinsic oxygen vacancies (White ball shapes). At LRS, an oxygen vacancy-based conductive filament is well established, connecting the TE and BE. At the HRS resulting from RESET, the conductive filament is dissolved, and fewer oxygen vacancies are present again. (b) A Nyquist plot from EIS measurements on initial HRS of SiO_2-based based memristors, of which the vertical line shape (parallel to the y-axis) indicates the pseudo-pure capacitive property. Based on the simulation, the equivalent circuit consists of a resistor in series with a capacitor, and it is displayed in the upper right corner. (c) A semicircle

shape appears in the Nyquist plot at LRS. Another resistor is paralleled with a capacitor in the simulated equivalent circuit. (d) The Nyquist plot at HRS after RESET becomes a straight-line shape again. The associated equivalent circuit is back to a series connection of one resistor and one capacitor.

EIS is instrumental to acquire a deeper understanding of the fundamental electrochemical mechanisms through the evaluation of impedance variations at various sinusoidal frequencies and resulting equivalent circuit interpretation.[42, 43] Since redox-based memristors' switching behaviors are relied on electrochemical reactions, this non-invasive EIS technique provides a unique way to characterize and perceive memristors' switching behavior.[43, 44] Thus, the EIS measurement was carried out on SiO_2 based memristors. To directly interpret the EIS results on an associated equivalent circuit model, the I-V characteristics of memristors (5 nm SiO_2) were rearranged on a linear-linear scale in Figure 3a. The green part of Figure 3a shows I-V characteristics in linear-linear scale for the initial high resistance state of memristor. The EIS measurement was employed on the memristor at this state. And the resulted Nyquist plot (left; green) in Figure 3b, exhibiting a straight line (parallel to the y-axis) supports the capacitive property of HRS of memristors. Based on the simulation, the equivalent circuit at this state consists of a resistor R_c at 10^2 Ω level and a capacitor C_s at 10^{-10} F level, connected in series. The resistance at this state of the resistor is attributed to contact resistance.[45] The capacitance value is aligned with our CV measurement from pristine devices (Figure 1f). And this capacitive property at "initial state" is conceptually explained in the right part of Figure 3a: the structure of a memristor at initial state is the same as that of a capacitor and there are few native oxygen vacancies in the SiO_2 switching layer. After turning on the memristor, i.e., at the state of Figure 3a in orange color period, an EIS measurement was repeated on the SiO_2-based memristor to

understand the on-state conduction behavior of the memristor. A clear semicircle in the Nyquist plot is observed in Figure 3c (middle; orange). Compared to the equivalent circuit at initial state, a new resistor (R_f) at 10^5 Ω level appears in the equivalent circuit at LRS, and it is connected to the capacitor in parallel. The new resistance value (~10^5 Ω) is aligned with the value measured in the I-V DC sweeping at LRS (Figure 2a-c). Therefore, the emerged resistor (R_f) in the equivalent circuit represents the filament(s) in the switching layer which was validated by the electric transport investigations in Figure S12 (i.e., Ohmic conduction mechanism at LRS). This EIS result complementarily supports the switching behavior suggested by the FEA analysis. At the same time, the majority portion of the memristor is still not connected with the conduction paths, thus, the capacitor component remains in the equivalent circuit. For simplicity, only one conductive path is illustrated in the schematic in Figure 3a to elucidate the LRS. A RESET process changed the LRS of memristor back to HRS, as shown in blue portion of I-V curve in Figure 3a. The device was turned off and showed the capacitor behavior with a negative bias, similarly as the previous HRS state. The EIS measurement in Figure 3d (right; blue) also verified the HRS of memristor where a vertically straight line appeared in the Nyquist plot again. The simulated equivalent circuit returns to a configuration of one resistor and one capacitor in series, with values at the same level as the initial state. This capacitive behavior at HRS (after RESET) indicates that the conduction path was almost completely dissolved (schematically described in Figure 3a right; blue), and the capacitor symbol describes the state of high resistance of the memristor. The annihilation of filaments can be ascribed to the back motion of oxygen ions under a reverse bias which in turn causes the recombination of oxygen ions and vacancies. Since the filament was regulated by compliance current, it can be near-fully ruptured during the RESET process. Thus, our EIS results on the capacitive properties at initial and after-RESET

HRS validate the near forming-free behavior of our memristors as well. Besides the above FEA and EIS investigations, the electric transport processes were analyzed in detail by replotting the I-V curve in Figure 3 to a log-log scale curve in Figure S12. The analysis reveals at HRS, the conduction mechanism follows typical Space-charge-limited conduction (SCLC).[17] And more importantly, at LRS, the conduction mechanism is determined as ohmic (slope of 1.36), providing additional evidence that our SiO_2-based memristors are governed by the filamentary conduction mechanism.[46]

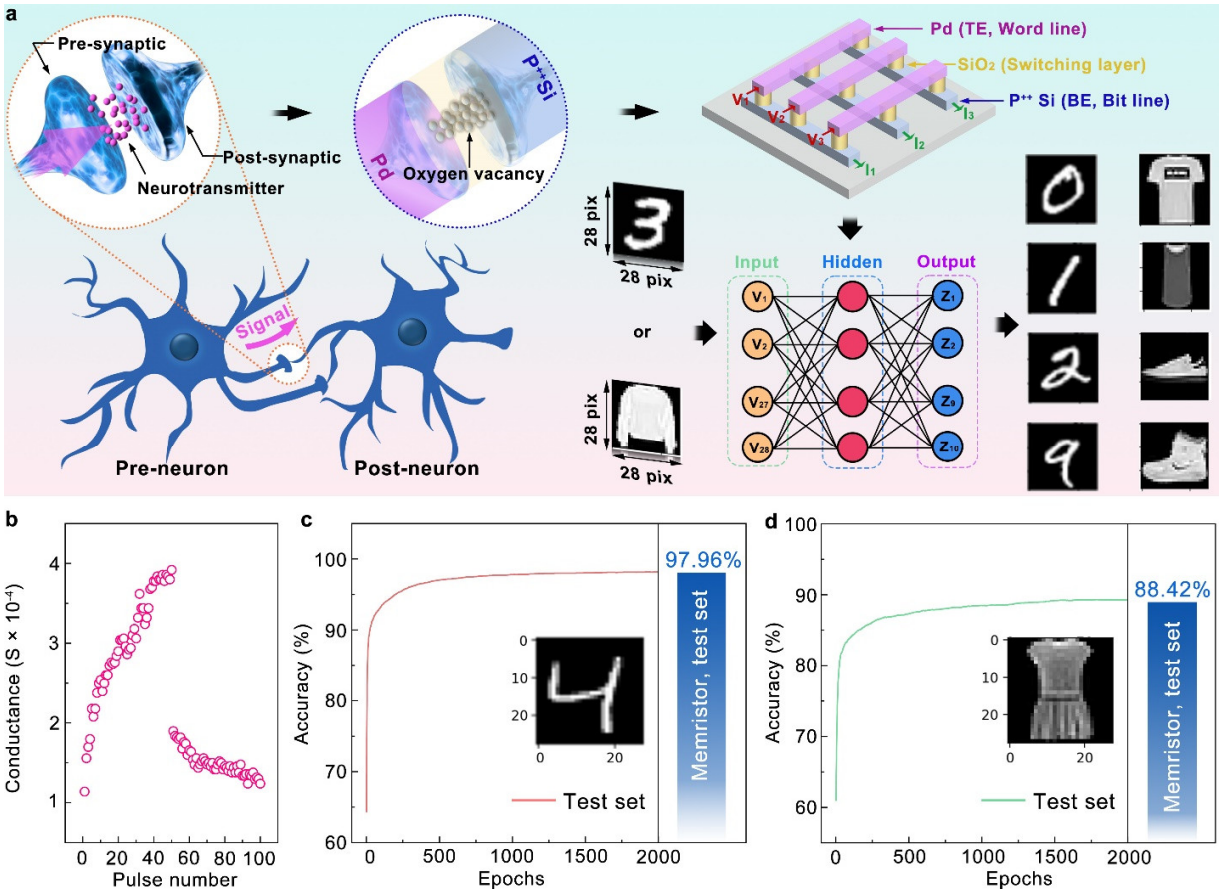

Figure 4. (a) The process for signal transportation between neurons. The structure and function of synapse in this process is illustrated in the dashed orange circle (left). In the dash blue circle (right), the synapse is schematically embedded into the SiO_2 based memristor to demonstrate the similarity between them. Next, a SiO_2 based memristive crossbar prototype is exhibited towards neuromorphic computing. Finally, a neural network for image recognition is explained with

instances from MNIST and fashion MNIST data sets (b) The synaptic characteristics evaluated from SiO_2 based memristors with 50 identical positive pulses and 50 identical negative pulses, demonstrating gradual variations of the conductance. The learning accuracy examinations with (c) MNIST and (d) fashion MNIST as a function of epochs.

As a two-terminal device, memristors, consisting of a switching layer and two electrodes in a simple sandwich structure closely resemble the structure of a chemical synapse in the brain. This similarity is demonstrated schematically in Figure 4a, particularly in the orange dash circle for synapse and blue dash circle for the memristor. The synaptic cleft corresponds to the switching layer of the memristor, while the pre-synapse and the post-synapse correspond to the top electrode and the bottom electrode of the memristor, respectively.

In the signal transmission process from one neuron to the next, as illustrated in Figure 4a, the action potential (i.e., pulse bias in memristor operation) is first transferred from the soma to the end of the neuron (i.e., the presynaptic neuron) via the axon.[47] Then, from the presynaptic neuron, synaptic weights are altered by the release of neurotransmitters. This neurotransmission process leads to the dynamic modulation of synaptic connection intensity. Our SiO_2-based memristor can mimic this synaptic behavior by tuning the conductance level with electrical pulses. The mechanism of updating weights for SiO_2-based memristor is similar to a chemical synapse, in which the oxygen vacancies function like neurotransmitters, forming a conductive path in the switching layer (i.e., connecting the top and bottom electrodes) and changing the conductance level of the device.[48] A proposed SiO_2-based memristor crossbar prototype is illustrated in the upper right corner of Figure 4. Such crossbar structure features two sets of wire electrodes, categorized as word lines (WLs) and bit lines (BLs). At each junction where these wires intersect, a resistive switching layer is present. Voltage pulses are fed through WLs then traverse through synaptic crossbar and converge at the BLs. The resulting output current is a

function of both the initial input voltages and the conductance properties of the memristors in crossbar, as described by Ohm's and Kirchhoff's laws.[49] We should note that the practical large-scale crossbar may experience disturbances caused by parasitic effects like series resistance and sneak path complications. The current flowing through the metal wires can cause a notable reduction in voltage, particularly affecting the cell at the greatest distance within the array. This phenomenon ultimately leads to what is commonly termed as the "IR drop" problem. This issue not only compromises the reliability of memory read operations but also reduces the accuracy of vector-matrix multiplication computations. Lowering the wire resistance or boosting the inherent resistance of the memristor can help mitigate this issue. Another parasitic issue sneak path refers to an unintended electrical pathway that allows current to flow through multiple memristors, rather than through the targeted cell for a particular operation.[50] Such sneak path issue may trigger operational malfunctions and excessive energy consumption.[51] To alleviate the sneak path issue, various strategies involve redesigning the basic units. For example, adding an access component to the single-memristor (1R) cell can create composite cells like one-transistor-one-memristor (1T1R) or one-switch-one-memristor (1S1R) to suppress the sneak current.[52] Neuromorphic computing capability of our SiO_2-based memristors was evaluated through pulse measurements with the pulse width of 5 ms and with continuous 50 positive pulses, followed by 50 negative pulses at the amplitude of 5 V for both positive and negative pulses. In Figure 4b, a prominent multi-conductance behavior is observed in the memristor, which mimics the information transportation between synapses. It should be noted that the resistance state is within the LRS regime during the pulse measurements (i.e., dynamic range) where the conduction filament experiences thickening (potentiation) and shrinkage (depression).[53] The asymmetric non-linearity factor (ANL) was calculated by using the following equation:

$$ANL = \frac{G_P\left(\frac{N}{2}\right) - G_D\left(\frac{N}{2}\right)}{G_{max} - G_{min}}$$

where G_{max}, G_{min}, $G_P(N/2)$ and $G_D(N/2)$ represent the conductance maximum, conductance minimum, median value of potentiation and medium value of depression, respectively.[54] As measured from synaptic behavior, our ANL was 0.52 which is comparable to those of other reports, typically ranging 0.3-0.54 [54, 55]

To demonstrate the neuromorphic computing performance of our memristor, we modeled a deep neural network (DNN) with 784 input neurons, 500 hidden neurons, and 10 output neurons based on our device. Further details on the simulation process are available in Note S2, Supporting Information. The DNN is employed to perform image recognition tasks on the MNIST and Fashion-MNIST datasets.[56] The computing structure of DNN is described in Figure 4a with examples of datasets. The input images are initially converted into 28x28 matrices with values ranging from 0 to 255. These matrices are then flattened into vectors of length 784 and fed into the DNN. The 10 output neurons correspond to 10 distinct classes, with the neuron exhibiting the highest value representing the recognized result. The DNN is initially trained on conventional hardware for 2000 epochs, attaining accuracy levels of 98.2% and 89.3% for the MNIST and Fashion-MNIST datasets, respectively. Subsequently, the trained weights are translated to conductance values based on our device's conductance changing curve. Given the finite number of conduction states, the learning accuracy becomes 98.0% and 88.4% for MNIST and Fashion-MNIST, respectively (Figure 4c and d). The marginal reduction (0.2% and 0.9%) in recognition accuracy validates the promise of our memristor for future applications in neural networks and neuromorphic computing.

CONCLUSIONS

We demonstrated high performance oxide-based memristors that are compatible with Si CMOS technology. Our SiO_2 memristors achieved a noteworthy on/off ratio as high as 1.4×10^5 with long-term stability and endurance. The oxygen vacancy-driven switching mechanisms were complementarily identified through theoretical and experimental investigations. A multi-physical field coupled model based finite element simulations systematically revealed the evolution of the conduction filaments as a function of applied bias where the roughness of TE/SiO_2 interface plays a significant role. The ~1 nm protrusion causes variations in the local electric field and hence selectively forms a conduction filament, preferably at the higher electric field locations. EIS analyses complement the theoretical switching mechanism investigation by identifying equivalent circuit components of the memristor at initial, SET, and RESET processes. Associated Nyquist plots ascertain pseudo single capacitor behavior at initial and RESET process, and a parallel structure of a capacitor and a resistor during the SET process. As a proof-of-concept, DNN was demonstrated with the parameters of our SiO_2 memristors. The demonstrated SiO_2-based memristors featuring notable high on/off ratio and reasonable reliability as well as low thermal budget processing may be of direct relevance to next-generation computing devices that require energy-efficient process and compatibility with current CMOS technology.

METHODS

The SiO_2 switching layer was deposited from a sintered ceramic SiO_2 target in a magnetron sputtering system on heavily-doped Si wafers (<0.003-0.005 Ωcm). Before the sputtering process, the deposition chamber was pumped down to a base pressure of under 9×10^{-7} Torr. Pure

Ar gas (15 sccm) was used as the sputter gas, leading to a working pressure of 1.7×10^{-3} Torr at an RF power of 150 W. Then, the deposited SiO_2 layer was annealed at 550 °C for 10 hours. A layer of palladium (Pd) was deposited as the top electrode (TE) on the annealed SiO_2/Si structure through a thermal evaporation system equipped with a 6 MHz oscillating quartz crystal sensor to monitor the growth rate and thickness. A shadow mask was utilized to define the shape and size of the TE during its fabrication. The thickness of the SiO_2 layer (5, 10, 20 and 30 nm) was verified by a Multi-Wavelength Ellipsometer (FilmSense FS-1) using an incident and detection angle of 65°. An FEI Themis Z TEM microscope equipped with an Energy Dispersive Spectroscopy (EDS) was employed to examine the structures and map elemental distribution in Pd/SiO_2/P^{++}Si memristors. The pattern of the top electrode was verified in plan-view images by an FEI Nova NanoSEM system.

DC current-voltage (I–V) sweeping evaluations of all SiO_2-based memristors were carried out using a semiconductor parameter analyzer (Agilent 4155B) connected to a probe station in a dark shield box. Capacitance-voltage (C-V) characteristics were performed with a precision LCR meter (Agilent 4284A). Electrochemical impedance spectroscopy (EIS) investigations were conducted in an electrochemical workstation (VersaSTAT3 Princeton). For the pulse measurement, the Agilent 33120A function arbitrary waveform generator provided the pulse profile, which could be conveniently designed by the Agilent IntuiLink Waveform Editor. A digital storage oscilloscope (Hantek DSO4254B) was utilized to monitor the pulse voltages, and the Agilent 4155B SMU was used to record the corresponding current. Physical Modeling details for finite element analysis can be found in Note S1 while detailed simulation for image processing is elaborated in Note S2 in the Supporting Information.

ASSOCIATED CONTENT

Supporting Information

CV measurements on devices with different thickness of SiO_2, retention characteristics on 5nm SiO_2 memristor, the electric field distribution within 5 nm SiO_2 switching layer at different stages, I-V DC sweeping characteristics of different thicknesses of SiO_2 switching layer, the oxygen vacancy evolution and the electric field distribution of memristor with 10 nm SiO_2 switching layer at different stages, gradual switching behavior of the 5nm SiO_2 memristor, physical modeling detail, and image processing detail.

AUTHOR INFORMATION

Author Contributions

F. Q. and Y. Z. contributed equally to this work. F.Q. and Y.Z.: Conceptualization, characterization for memristors' performance, finite element analysis, draft writing. Z. G.: Image processing simulation. C. K., J. P., and K. N.: TEM characterization. X. F.: Assistance with electrical measurements. T. P., H. P., K. Z., H. S., X. R., and S. L.: Conceptualization, methodology, supervision, funding acquisition, writing, review, and editing.

Notes

The authors declare no competing financial interest.

ACKNOWLEDGMENTS

This work was partially supported by National Science Foundation, Award number ECCS-1931088 and CBET-2207302. S.L. and H.W.S. acknowledge the support from the Improvement

of Measurement Standards and Technology for Mechanical Metrology (Grant No. 23011043) by KRISS. The authors would like to thank Dr. Kejie Zhao for providing electrochemical workstation.

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