I AM HONORED TO RECEIVE THIS year's IEEE Pioneer Award in Nanotechnology. I would like to use this opportunity to share three nanotechnology approaches we have developed and our vision on how these could contribute to the continued scaling of semiconductor technologies in 3D and by heterogeneous integration, with plenty of room all-around.

2022 IEEE NANOTECHNOLOGY PIONEER AWARD RECIPIENT

It is widely accepted that the Feynman Lecture delivered on Dec. 29th, 1959 at the annual American Physical Society meeting, "There is plenty of room at the

There Is Plenty of Room All-Around

Highlight of Semiconductor Nanotechnology Research in My Lab

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bottom," spurred the beginning of the nanotechnology field. In that lecture, Feynman brilliantly articulated that size matters – "When we get to the very, very small world—say circuits of seven atoms—we have a lot of new things that would happen that represent completely new opportunities for design. Atoms on a small scale behave like nothing on a large scale, for they satisfy the laws of quantum mechanics. So, as we go down and fiddle around with the atoms down there, we are working with different laws, and we can expect to do different things. We can manufacture in different ways. We can use, not just circuits, but some system involving the quantized energy levels, or the interactions of quantized spins, etc." His vision on how physics and engineering could move in the direction of shrinking in size eventually created nanotechnology – "an invitation to enter a new field of physics," as the subtitle of that famous lecture rightly noted.

For semiconductor nanotechnology, we must start with the discovery of transistors and how the transistors scaled in dimension and performance over the past half a century. In 1947, John Bardeen (1908–1991) and Walter Brattain (1902–1987) produced a semiconductor amplifier, named a "transistor," which was further developed by William Shockley (1910–1989); and the three of them were awarded the Nobel Prize in Physics in 1956. That first transistor was essentially made by hand, one at a time. The concept of the integrated circuit was not conceived until Jack Kilby (1923–2005) and Robert Noyce (1927–1990) independently came up with the conception of integration. In July 1958, Jack Kilby proposed a novel miniaturized electronic circuit with all components completely integrated into the body of the semiconductor (US Patent No. 3,138,743). Almost at the same time (Jan. 1959), Robert Noyce, from the then Fairchild Semiconductor (the precursor of Intel), also filed his patent (U.S. Patent 2,981,877) on the concept of multiple devices on a single piece of silicon (Si): the integrated circuit. Compared with Kilby's drawing, Noyce's planar transistor clearly depicted metal interconnect without flying wires. There is no doubt that it is these two giants who set the field of semiconductors onto the road of "reducing size,

weight, etc. as well as cost per active element." In 2000, the Nobel Physics Prize was awarded to Jack Kilby "for his part in the invention of the integrated circuit." With this integration scheme, Kilby envisioned that "there is no limit upon the complexity or configuration of circuits which can be made in this manner." Indeed, no other industry has advanced, and continues to reinvent itself, at the amazing rate of transistor technology predicted by Gordon Moore. The number of transistors per die doubles every two years approximately. The continuation of Moore's law has been enabled by many disruptive transformations at the materials, structures, and circuit levels, including strained Si at 90 nm node, high-k metal gate at 45 nm node, FinFET at 22 nm node; and continued aggressive scaling for integration is 3D in nature and heterogeneous by definition. At the same time, tremendous progress in optoelectronic, high-speed, and high-power electronic devices, have been enabled by compound semiconductor heterojunction growth and nanofabrication.

Inspired by the transformative impact so many pioneers in the field, my research lab, which started at University of Illinois about 16 years ago and recently relocated to the University of Texas, has been striving, in our own way, to address the ever-present need to reduce the size, weight, power, and cost (SWaP-C) of semiconductor devices. Our research objective is to create semiconductor nanostructures that enable new device concepts and new science discoveries, in a compatible and scalable fashion. Below, I highlight three nanotechnology platforms we have been developing and a few examples of the unique nanostructures enabled are shown in Figure 1.

MACETCH–NOT YOUR ORDINARY ETCHING

From transistors to lasers, semiconductor wafers go through many levels of lithography, deposition, and etching. In the fabrication of modern optoelectronic and electronic devices such as FinFETs, anisotropic etching is indispensable. Wet etch is inherently isotropic in most cases, and plasma-based dry etch, such as

reactive ion etching, is therefore required. Defying the isotropic nature of conventional wet etch, metal assisted chemical etching (MacEtch or MACE) is a near-room temperature, plasma-free, yet highly anisotropic etching method. MacEtch relies on a local catalysis and electron transfer effect to enable site-controlled semiconductor nanostructure fabrication. Unpresented aspect ratio (as high as 10,000:1) and an etch rate > 3μm/min have been reported. [1], [2], [3], [4], [5], [6], [7] This innovative etching method has profound impact on semiconductor fabrication, not only because of the readily achievable extraordinary aspect ratio, but also the inherent absence of ion-induced damage. The latter becomes increasingly critical as devices are aggressively scaled down, especially for compound semiconductors where high energy ion induced etching damage cannot be easily repaired without causing collateral loss.

We first reported MacEtch as a method to generate porous Si using a discontinuous layer of noble metal catalyst metal film under open circuit in 2000 in a solution of hydrofluoric acid (HF) and peroxide (H_2O_2). [8] The first related patent was filed in 2000 and granted in 2004 (U.S. Patent 6,790,785). Note that the acronym MacEtch or MACE was not used in the community until much later. Highly anisotropic etching was then achieved by patterning the metal catalyst film, using the self-assembled dendritic Ag network from the AgNO3 solution and various conventional lithographic methods. [9] The frontier of this technology continues to advance from investigating the fundamental mechanism, process parameters, properties, and applications, to extending its applicability to other semiconductors. Beyond Si, we have demonstrated MacEtch of Ge, [10] III-As, [11] III-P, [12], [13] III-N, [14] SiC, [15] and Ga_2O_3, [4], [16], [17], [18], as well as heterostructures. Metal catalysts, including the well-known noble metals such as Au, Ag, Pt, and CMOS-compatible Ru [19] and TiN [20], as well as metal stacks, have been proven to be effective for different structural or device requirements. Depending on the semiconductor doping type and level, metal catalyst-semiconductor barrier height,

[21] catalyst pattern (size, pitch, shape, and border), [22], [23] and etching solution composition and concentration, MacEtch can lead to different etching rates, topography, porosity, and morphology.

Apart from the competition with conventional chemical etch, there are mainly two rate-determining steps, [22] carrier generation (oxidation) and mass transport (dissolution of oxide). Self-anchored catalyst (*SAC-MacEtch*) overcomes the mass-transport limitation of large feature sizes and made it possible to etch over large areas and through deep trenches vertically, all the way through the entire wafer (> 500 μm) without detouring [24]. When either one of these two critical rate-determining steps cannot proceed where the metal-catalyst is, inverse-MacEtch (*i-MacEtch*) occurs, i.e., etching starts in the location where metal catalyst is absent. [12], [13] For wide and ultra-wide bandgap semiconductors, because of the limited carrier mobilities in these materials, it is necessary to use above bandgap photons (*hν*) to generate free electron-hole pairs and enhance MacEtch rate. [4], [14], [15], [16], [17], [18] *hν-MacEtch* is inherently *i-*MacEtch, because the UV light does not penetrate metal catalyst film; it is essentially an open-circuit photo-enhanced etching, but spatially defined by the metal catalyst. *I-MacEtch* enabled the demonstration of high performance, ultra-smooth and damage-free sidewalls in InP (see Figure 1(a)) and Ga_2O_3 finFETs. [12], [25] The additional degree of freedom, *hν* energy, allows selective etching based on the bandgap energy of the semiconductor. By adding ferromagnetic metal in the catalyst, magnetic-field guided MacEtch (*h-MacEtch*) [26], [27], [28] can enable better control of the etching direction, including arbitrary trajectories. Efforts to take MacEtch to vapor-phase have led to better control of the metal-Si interface and etching morphology and overcome stiction issues. [29], [30] We believe that programmable vapor-phase MacEtch (*VP-MacEtch, U.S. Patent 10,748,781*), where the flow of etchants can be independently controlled, will ultimately position the MacEtch technology towards true scalability and manufacturability.
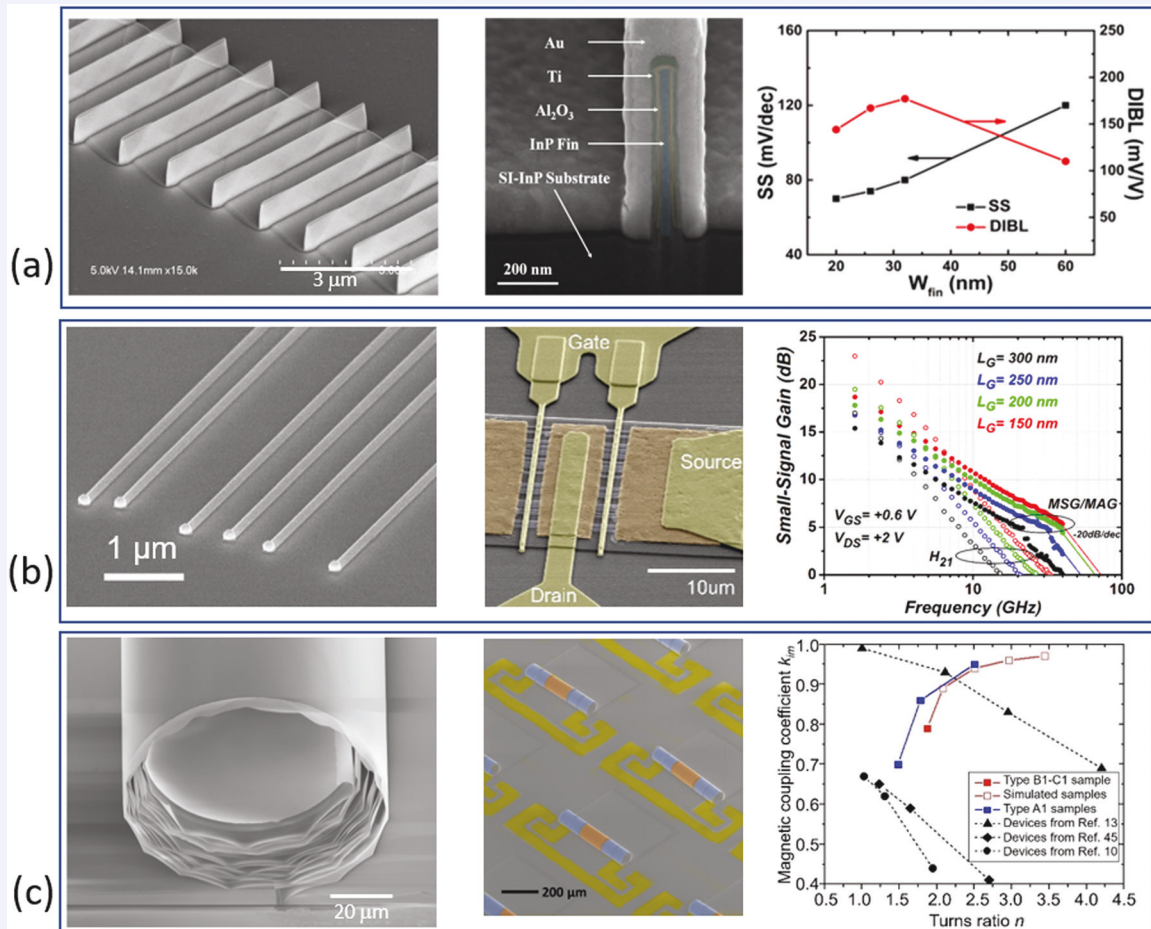

FIGURE 1 (a) From left to right: SEM image of a 50:1 aspect ratio InP fin array produced by MacEtch, the cross-section of a single fully fabricated FinFET, and the plot of subthreshold slope (SS) and drain-induced barrier lowering (DIBL) as a function of fin width [12]. (b) From left to right: SEM images of a planar GaAs nanowire array grown by Au-assisted VLS selective lateral epitaxy, a fully fabricated GaAs/AlGaAs planar nanowire double gate finger RF testing configuration, and the small signal gain as a function of frequency for various gate length (L_G) [32], [33]. (c) From left to right: SEM images of a single self-rolled-up nanomembrane (S-RuM) tubular inductor, an array of fully fabricated S-RuM L-C network, and the magnetic coupling coefficient of S-RuM transformers as a function of turns ratio. [41], [42], [43]. Adapted from [12], [32], [33], [41], [42], [43] with permission.

The simplicity, versatility, manufacturability, and the plasma-free, damage-free, and highly-anisotropic nature of the MacEtch process make it highly promising to supplement and enhance the well-known reactive ion etching methods for deep trenches or pillars with high aspect ratios, periodic or random arrays of ordered or random patterns, as well as shallow surface texturing. This technology is positioned to have disruptive lasting impact to various electronics, photonics, energy, quantum and biosensing applications.

MOCVD NANOEPITAXY FOR 3D HETEROGENEOUS INTEGRATION

For semiconductor technologies, advancement in epitaxial growth is one of the major factors responsible for the technology development momentum. Metal-organic chemical vapor deposition (**MOCVD**) represents the main-stream approach for the production of compound semiconductor lasers, high speed and high power transistors, LEDs, photodetectors, and high efficiency solar cells. Nanowire has long been regarded as a promising architecture for beyond Si finFET logic and high frequency III-V electronics, as well as next generation optoelectronic applications. The challenges have been the controllability and manufacturability. My lab's discovery of selective lateral epitaxy of planar III-V nanowire arrays via the metal-assisted vapor-liquid-solid (VLS) mechanism [31], [32] has transformed the long-standing perception of uncontrollability of self-assembled nanowires. On the fundamental side, this work opens up a new paradigm of crystal growth and consequently in situ lateral junction formation. Technologically, in-plane nanowire configuration is perfectly compatible with existing planar processing technology for industry. We have demonstrated chip-scale GaAs/AlGaAs nanowire high electron mobility transistors (HEMTs) with record DC and RF performance (Figure 1(b)), and a clear path to reach THz for high speed applications [33]. As transistor scaling continues, the FinFET inevitably evolves to the Gate-All-Around (GAA) configuration for even better static control and allows stacking transistors vertically. Our innovation in this space includes vertically stacked NWs with tunable size and doping levels for each level in the stack (U.S. Patent 20,140,353,574; licensed) as the high mobility GAA channel for low power and high linearity on-chip applications.

On the other hand, the holy grail of compound semiconductor technology is to integrate onto the mature Si platform, and the quintessential challenge of heterogeneous integration of III-V on Si and other foreign substrates is the lattice matching restriction. Through unconventional epitaxial growth modes including selective area, direct and van der Waals epitaxy, my lab has achieved site-controlled MOCVD growth of device quality III-V (GaAs, InAs, InGaAs, GaP, InAsP, GaAsP) nanowire arrays on Si [34], [35] and graphene [36], [37], as well as MoS_2 on GaN, [38], and uncovered new understanding of selective area nanoepitaxy and quasi-van der Waals epitaxy. These results could bring translational impact on nanoelectronics and nanophotonics, including III-V gate-all-around transistors and multi-junction tandem solar cells.

S-RUM NANOTECHNOLOGY FOR EXTREME MINIATURIZATION AND INTEGRATION

Combining bottom-up and top-down approaches, my group has established a 3D self-rolled-up membrane (**S-RuM**) nanotechnology platform for extreme miniaturization of passive electronic devices for radio frequency integrated circuits (RFICs) and beyond. The overarching physical principle of S-RuM nanotech is strain-driven spontaneous deformation of 2D membranes into 3D architectures [39]. Complex 3D structures formed by S-RuM enable advanced functionalities that are otherwise out of reach. S-RuM RF inductors have been demonstrated with a footprint that is 10 – 100 times smaller than the 2D counterpart [40]. By virtue of the small size and 3D confinement, energy loss to substrate and free space is minimized, leading to high frequency operation. Monolithic mTesla level magnetic induction was achieved at 10 MHz by geometric transformation of centimeter-long 2D nanomembranes into 140 µm diameter air-core microtubes (see Figure 3(c)), followed by post-rolling ferrofluid core-filling [41]. By stacking two S-RuM inductors in-plane or vertically to form transformers, near unity coupling coefficients and unconventional advantageous scaling trend with turns ratio have been achieved (Figure 3(c)) [42]. By combining multiple inductors and capacitors, all in one single lithography step monolithically before rolling, various L-C network (see Figure 3(c)) can be configured with unprecedented integration density and configurability [43]. To paraphrase Kilby on active device integrated circuits, there is practically no limit upon the complexity or configuration of L-C circuits, which can be made in the manner of S-RuM, and all with one single lithography step. Through global and local strain engineering, transmission lines (U.S. Patent 9,018,050) and antennas (U.S. Patent 9,224,809) with ultra-high frequency (RF, mm Wave, and THz) and bandwidth can also be enabled. S-RuM technology promises to break the constraints of size, weight, and performance (SWAP) of RFICs. The miniaturized form factor can also bring transformative impact to on-chip integration of passive components to power circuits, wearable and flexible IoT devices, microfluidics, and biomedical applications, including the demonstrated guiding and accelerating neuron cell growth for neural regeneration and DNA-based data storage [44], [45].

It is impossible to imagine a world without semiconductors. Through both bottom-up and top-down approaches, we have discovered or developed several portfolios of semiconductor nanotechnology for potential lasting impact to electronics, photonics, energy, and quantum systems, as well as human health. With continued innovation including heterogeneous integration and system-driven codesign approaches, there is plenty of room all-around to further scale semiconductor devices smaller, lighter, faster, more efficient, and less expensive. Our path to profoundly advance nanotechnology, inherently 3D, will continue, from epitaxial growth, fabrication, to devices, circuits, and systems.

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