A Review of Silicon Carbide CMOS Technology for Harsh Environments

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***Abstract*— A comprehensive overview of the advancements, challenges, and prospects of silicon carbide (SiC) complementary metal-oxide-semiconductor (CMOS) technology is presented. As the demand for high-performance and energy-efficient electronic devices continues to grow, SiC has emerged as a promising material due to its unique properties. The paper aims to provide a thorough understanding of the state-of-the-art developments in SiC CMOS technology. The paper delves into the key features of SiC and its compatibility with CMOS processing techniques. It highlights the challenges associated with SiC CMOS technology, such as substrate quality, interface states, and process integration. Examples of CMOS circuitry that have been successfully designed, fabricated, and tested are provided.**

***Index Terms*—Wide bandgap, silicon carbide, CMOS, integrated circuit, harsh environments.**

I. Introduction

SILICON (Si) has been the dominant player for decades in integrated circuits (ICs) to satisfy a tremendously wide range of needs for different applications since the 1950s. Si-based semiconductors can be processed virtually without defects and have excellent manufacturability. However, as has been well documented, the limits of Si are being approached since Si-based semiconductors have limited blocking voltage, limited thermal capability, limited efficiency, and operating frequency, etc. [1]. Due to several unavoidable physical constraints, Si-based semiconductors are not suitable for applications under harsh environments. Examples include extremely high-temperature, high-voltage, high-radiation, and corrosive gas environments in applications such as space exploration, nuclear reactors, automobile sectors, etc. as shown in Fig. 1. Instead of Si, wide bandgap semiconductor materials, known as third-generation semiconductors, are preferred for harsh environments. Among the wide bandgap materials, Silicon carbide (SiC) is the only wide bandgap material where complementary metal-oxide-semiconductor (CMOS) is not merely a promising possibility, but already an established platform with IC demonstrations and extreme-condition reliability studies [3].

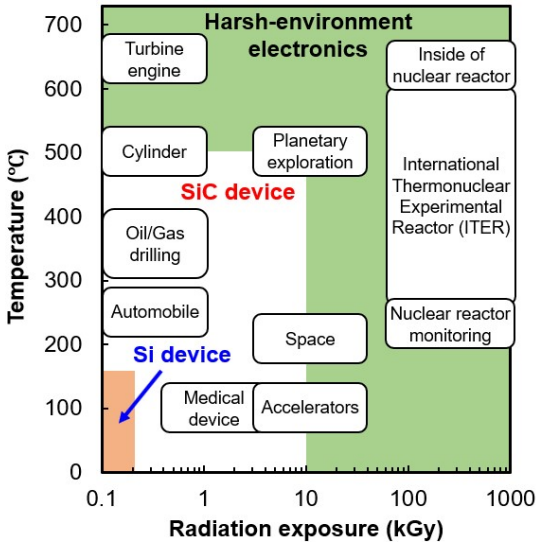

Fig. 1. Demand for harsh environment electronics [2].

A. SiC properties

SiC is the only compound of group IV elements comprised of Silicon (Si) and Carbon (C). Fig. 2 shows the temperature

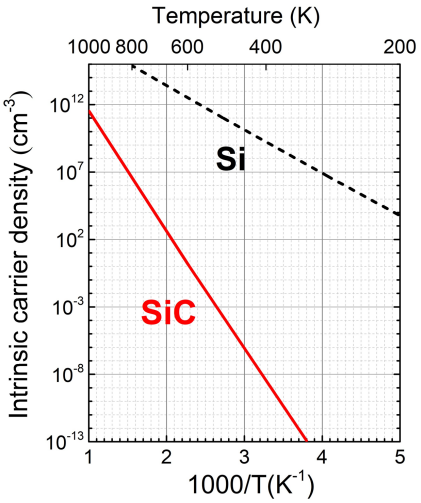

Fig. 2. Temperature dependence of the intrinsic carrier density for SiC and Si [4].

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TABLE I. MAJOR PHYSICAL PROPERTIES OF COMMON SIC POLYTYPES AT ROOM TEMPERATURE [2], [5], [6]

Parameters	Si	3C-SiC	4H-SiC	6H-SiC
Bandgap Eg (eV)	1.12	2.36	3.26	3.02
Band Structure	Indirect bandgap	Indirect bandgap	Indirect bandgap	Indirect bandgap
Intrinsic carrier concentration n_i (cm^{-3})	$1.5x10^{10}$	6.9	$8.2x10^{-9}$	$2.3x10^{-6}$
Breakdown field (MV/cm)	0.3	1.5	2.5-3	3
Electron mobility μ_e ($cm^2/V{\cdot}s$) *1	1450	1000	1020	450
Electron mobility μ_e ($cm^2/V{\cdot}s$) *2			1150	100
Hole mobility μ_p ($cm^2/V{\cdot}s$)	450	100	120	100
Dielectric constant ε	11.9	9.7	9.7	9.66
Electron saturation drift velocity V_{sat} ($x10^7$ cm/s)	1.0	2	2.2	1.9
Thermal conductivity K (W/cm·K)	1.5	5	4.9	4.9

*1 perpendicular to c-axis, *2 parallel to c-axis

dependence of the intrinsic carrier density for SiC and Si [4]. Due to the wide bandgap, SiC has an extremely low intrinsic carrier density (5×10^{-9} cm^{-3} at room temperature) whereas the density is about 1×10^{10} cm^{-3} in Si, enabling high-temperature operation of SiC electronic devices.

SiC has a wide range of crystalline structures known as polytypes varying in the stacking sequence of Si atoms and C atoms, leading to variations in electrical, thermal, optical, and mechanical properties. Among more than 200 polytypes [5], the commonly known and popular polytypes include: Cubic (3C-SiC) and hexagonal (4H- and 6H-SiC), which are being developed for device applications. Table I shows the physical properties of 3C-, 4H-, and 6H-SiC along with Si at room temperature. 3C-SiC is not stable at very high temperatures, which makes it difficult to grow large ingots at a reasonable growth rate compared to 4H-SiC and 6H-SiC. Thus, 4H-SiC and 6H-SiC polytypes are more popular. After the introduction of 4H-SiC wafers in 1994, 4H-SiC has become the dominant polytype over 6H-SiC used in research. This is due to the fact that the electron mobility along <1000> in 4H is about ten times higher than that in 6H as shown in Table I.

B. Essentiality of SiC IC technology

Despite having outstanding physical, chemical and electrical properties, SiC's low-voltage applications are less explored while most commercial efforts have targeted high-voltage discrete devices. The commercialization of SiC-related products will definitely benefit from the research and development of SiC-based integrated circuits (ICs) because specific electronic systems can be achieved to operate under harsh environments. From the IC technology development point of view, much more effort is ongoing. It is necessary to have a review of the status of IC technology development while there has been some review work published for SiC-based power devices [7], [8]. The following sections of this paper review the IC technology advancement, specifically the CMOS technology as SiC CMOS technology will be one of the most important technologies that will further drive the emergence of the world-wide SiC electronics industry. Device development, the applications of ICs, and monolithic integration development of high-voltage (HV) power devices and low-voltage (LV) components based on SiC CMOS technology are presented.

II. SiC IC DEVELOPMENT

Since the 1970s, SiC-based devices such as the MOSFET have been investigated, but the use of SiC was first suggested by Baliga in power devices in 1989 [9]. There has been strong momentum in SiC-related research and development. The first commercial SiC device (i.e., SiC Schottky diode) was introduced by Infineon in 2001 followed by the release of diodes by Cree and ST Microelectronics [10]. Since then, SiC has attracted a large interest in many research fields, such as power electronics, harsh environment sensing, high operation temperature circuits, and more. Cree (known as Wolfspeed after 2017) launched the industry's first SiC power MOSFET in 2011 [11]. Whereafter, many new players such as Rohm, STMicroelectronics, Infineon, Microsemi, and others announced discrete SiC power MOSFETs.

Although most commercial efforts have targeted high-voltage discrete devices as aforementioned, there is a desire for SiC ICs under harsh environments, especially when it comes to the application areas such as sensing and power circuits/energy conversion [12]. The challenges to develop SiC IC technologies are greater than expected. For example, an 8 nm channel length of commercial Si CMOS devices in modern ICs has been achieved with 2 nm technology node [13] whereas the channel length of SiC is still in the 1 µm range. SiC CMOS technology is still in its infancy, comparable to Si technology in the mid-1980s.

The development of SiC ICs traces to the early 1990s led by Cree [14] and Purdue [15] and was mainly based on NMOS, CMOS, JFET and BJT technologies. The SiC IC was developed based on NMOS technology, followed by CMOS. Taking account of technical drawbacks such as low channel mobility, gate oxide reliability, etc. JFET technology has been intensively investigated. The complicated gate driver remains a challenge. More recently, BJT IC technology has been proposed. However, the biggest weakness of BJTs is their low current gains. Table II lists the main IC technologies along with the

TABLE II. OVERVIEW OF SIC IC TECHNOLOGIES

Technology	Temperature limitation	Company/R&D institute	Ref.
NMOS	300°C	Purdue University, GE	[15]-[19]
CMOS	500°C	Cree, Purdue University, Raytheon, Hitachi, Fraunhofer	[14], [20]-[26]
JFET	800°C	NASA	[27]-[30]
BJT	600°C	Purdue University, KTH, GE	[31]-[34]

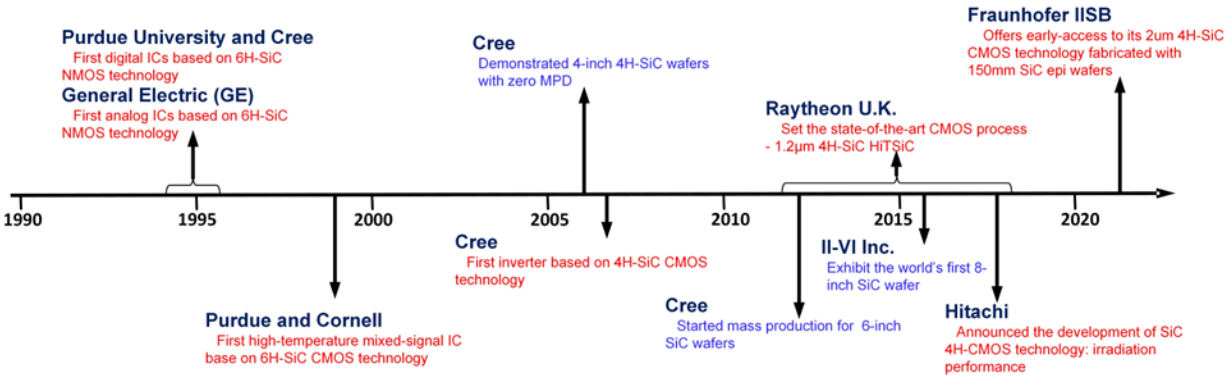

Fig. 3. SiC MOS technology development milestones.

temperature limitation and major players. It should be noted that in practice, the operating temperature of ICs is currently limited by the thermal stability of dielectrics and metallization used for the fabrication of these devices.

The authors' group has explored the advancement of SiC CMOS technology. Fig. 3 summarizes the key milestones in SiC MOS technologies. In 1994, Purdue University reported the first digital ICs such as inverters, NAND and NOR gates, RS flip-flops, etc. in 6H-SiC-based NMOS technology with n-channel enhancement-mode MOSFETs [15]. Shortly, the researchers at General Electric (GE) reported the first monolithic analog IC, i.e., operational amplifier and presented the operating waveforms at room temperature and over 300°C with 6H-SiC NMOS technology [19]. In 1999, investigators from Purdue and Cornell initially presented a high-temperature mixed-signal IC using 5 µm 6H-SiC CMOS technology [20]. As the crystal growth technology for 4H-SiC with higher carrier mobility advanced, research endeavors increasingly shifted the focus toward the utilization of 4H-SiC. Cree [26] demonstrated the first 4H-SiC CMOS inverter in 2006. During 2011-2013, Raytheon U. K. reported their 4H-SiC CMOS ICs with their 1.2 µm HiTSiC process, which employed two separately doped N- and P-wells on epi wafers and allowed operation on a single 15V supply at temperatures from room temperature to beyond 300°C [23], [35]-[36]. The researchers in the University of Arkansas took advantage of the HiTSiC process and demonstrated the first digital-to-analog converter (DAC) operational at 400°C [37] and other complex circuitry [38]. In 2017, Hitachi announced the development of SiC CMOS technology, emphasizing radiation-resistance, especially in the wake of the Fukushima disaster. The radiation performance of the transimpedance amplifier [39] and op-amp [25], [40] was reported. More recently, Fraunhofer IISB offers early access to its double-well 2 µm SiC CMOS technology. At this point, there is no mature SiC CMOS process for SiC IC commercial fabrication, and the accessible in-house SiC CMOS fabrication processes are scarce.

TABLE III. PROCESS TEMPERATURE RANGES FOR SI AND SIC

Process step	Si (°C)	SiC (°C)
Bulk growth	1400-1500	2200-2400
Epitaxial growth	600-800	1400-1600
Thermal oxidation	900-1200	1150-1250
Ion implantation	Room temp	600-800
Post-implantation annealing	1000-1200	1200-1800
Contact formation	400-600	800-1000

III. SiC CMOS Process

Though SiC CMOS is similar to Si because it allows thermal oxidation in the same way as Si, the difference in the processing temperature involved makes the SiC CMOS a non-self-aligned process. Thus, the source and drain regions must be processed before the gate stack is formed. Table III lists the temperature ranges for SiC and Si processes [12].

The overall fabrication process flow is briefly presented in Fig. 4. The attention of this section is focused on a few critical processes in SiC CMOS including the reported problems and the current level of technology, whose development is essential to improve the device and circuit performance.

A. Ion implantation and activation

Selective doping is an essential process for device fabrication. Ion implantation and diffusion are widely implemented to control the doping profiles of semiconductor devices. However, due to the low diffusion coefficients of dopants within SiC, the diffusion process would take a significant amount of time and is not realistic for achieving the desired doping profile [41]. This makes ion implantation one of the most important processes for the fabrication of SiC CMOS devices. Ion implantation based on SiC has been extensively

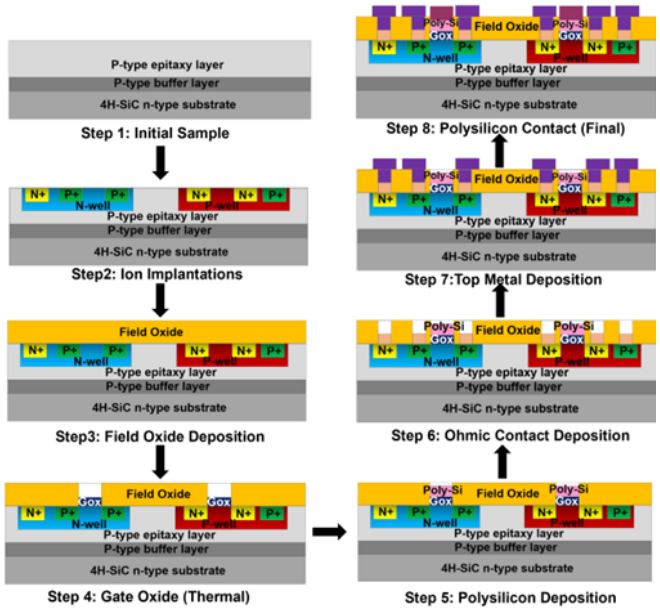

Fig. 4. Simplified SiC CMOS process flow.

TABLE IV. ION IMPLANTATION CONDITIONS AND RESULTS OF PUBLISHED SIC CMOS PROCESS

Ref.	Process layers	Ion implantation				Anneal			Results	
		Dopant	Total dose (cm^{-2})	Maximum energy (keV)	Temperature (ºC)	Temperature (ºC)	Time (min)	Condition	Peak doping (cm^{-3})	Junction depth (µm)
[22]	N-well	N	5.27E12	380	650	1550			1E17	0.7
[21]	P-well	B	3.5E14	380	650	1600	40		5E18	1
[66]	N+	N	3.4E15	190	650				1.2E20	0.3
	P+	Al	2E15	260	650				5E19	0.3
[67]	P+	Al	1.7E15	120	800	1500	30			
[26]	P-well	Al				1650			4E19	0.6
	N+	N							1E20	0.3
	P+	Al							2E19	0.5
[68]	P-well	Al	4E13	400	600	1700	2			
	N+	P	7.2E15		600					0.2
	P+	Al	6.6E15		600					0.2
[69]	N+	P				1600	5		2E20	0.2
	P+	Al							2E20	0.2
[70]	P-well	Al		350		1650	30	Carbon cap		
	N+									
	P+									
[71]	P-well	Al				1650	10	Carbon cap		
	N-well	N								
	N+	N								
	P+	Al								
[72]	P-well	Al	3.1E14	800	500	1700	20	Carbon cap	1E19	1.8
	N-well	P	2.05E13	900	500				1E18	1.4
	N+	P	2.5E15	220	500				1E20	0.2
	P+	Al	6.8E15	170	500				2E20	0.2

investigated, which includes the modeling [42]-[44], implant temperature [45]-[48], activation [49]-[59]surface roughness [44], [60]-[62], and defects [63]-[65]. Table IV summarizes the ion implantation conditions and results of published SiC CMOS process. In order to achieve a uniform doping profile, multiple-step ion implantations were carried out in these SiC CMOS processes. As shown in the table, nitrogen, phosphorus and aluminum are the most commonly used dopants for SiC CMOS devices. A total dose higher than 1E15 cm^{-2} is required for N+ and P+ regions. The peak doping concentrations of N+ and P+ regions are higher than 1E19 cm^{-3}, which achieves low contact and sheet resistances. The junction depths of N-well and P-well regions are usually around 1 µm, which requires a maximum implant energy of 350 to 400 keV. Meanwhile, ion implantation at elevated temperatures (i.e., >500ºC) is normally conducted to reduce the damage (e.g., surface roughness and defects) caused by the ion implantation. In addition, high-temperature activation is required to recover damage from the implant step and electrically activate the dopants in the SiC. Annealing temperatures higher than 1500ºC are usually employed for the activation. Carbon caps were implemented in some of the processes to reduce the surface roughness during the high-temperature anneal. Additionally, in order to improve the channel mobility of SiC NMOS devices, selective N-type implantation as a counter doping was performed to the P-type channel region [13], [73], [74].

B. Gate oxidation

A unique advantage of SiC among wide bandgap materials is that it can be thermally oxidized to give high-quality SiO_2, which can be utilized as a gate dielectric in MOS devices. This subsection describes the technological development of gate oxidation and the improvement of the quality, especially the interface, which is mainly related to the oxidation condition, surface roughness, post-annealing condition, etc.

Fig. 5 lists the three main gate oxide formation methods. To begin with, the thermal growth of SiO_2 on SiC is performed by dry or wet oxidation in an oxidation furnace. The wet oxidation process is faster than dry oxidation. During oxidation, the free C atoms remaining at the surface form C clusters at the interface, which greatly affect the electrical properties [76]. Surface treatment methodologies have been studied to improve the interface before oxidation. This includes the use of sacrificial oxide and SiC surface etching using H_2. H_2 etching has been shown to be effective in the preparation of a terminated surface that is ideal for future oxidation [77]. Sacrificial oxide is intended to remove the top rough layer of SiC and expose pure SiC for oxidation. This technique is used in silicon as surface preparation for thermal oxidation. Sacrificial oxide alone was only mildly effective in improving the interface as C clusters from sacrificial oxide growth may not be fully etched away by the sacrificial oxide removal [78]. As a result, it is proposed that a combination of both sacrificial oxide and H_2 etching can significantly improve the interface's smoothness [79], [80]. Post-oxidation anneal (POA) is necessary to reduce the fixed oxide charges and interface states. There has been considerable research to apply nitridation during the POA by using nitric oxide (NO), nitrous oxide (N_2O), ammonia (NH_3) and so on. The nitridation process is mature enough to be applied in the power MOSFETs, but the channel

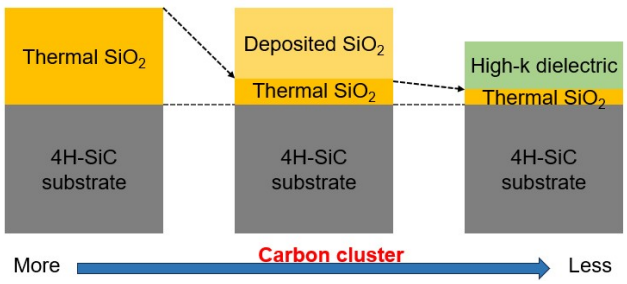

Fig. 5. Main gate oxide formation technologies [75].

TABLE V. SUMMARY OF INTERFACIAL CHARACTERISTICS AND CHANNEL MOBILITIES OF 4H-SIC MOS DEVICES FOR VARIOUS THERMAL OXIDATION PROCESSES

Oxidation	Optimal POA	Dit at E_C-E ($cm^{-2}eV^{-1}$)	Peak channel field-effect mobility ($cm^2/V•s$)	Ref.
Dry/Wet oxidation	Ar for 30mins	4-6x10^{12}@0.2eV	5-7	[83]
Wet oxidation	- NO, 1175℃ for 2h	N.A.	4-11 27-50	[84]
Dry oxidation	- NO, 1175℃ for 2h	2x10^{13}@0.1eV 2x10^{12}@0.1eV	<5 30	[85]
Dry oxidation	N_2O, 1200℃ for 3h	9x10^{11}@0.2eV	27	[86]
Dry oxidation	N_2, 1350℃ for 30mins	1x10^{12}@0.2eV	-	[87]
Dry oxidation	$POCl_3$, 1000℃	9x10^{10}	89	[81]
Dry oxidation	BN diffusion source, 950℃ for 10mins	9x10^{10}@0.2eV	102	[88]
CVD	N_2, 1250℃ for 60mins NO, 1250℃ for 60mins	2x10^{12}@0.2eV 1x10^{11}@0.2eV	-	[89]
PECVD	N_2O, 1300℃ for 60-360mins	3x10^{11}@0.2eV	30-52	[90]
Al_2O_3 MOCVD	-	5-8x10^{11}@0.2eV	200-300	[82]

mobility is still very low. Therefore, in addition to the nitridation method, other methods such as doped gate oxide and high-k dielectrics have been proposed. At NAIST in Japan, the gate oxide was doped with P in $POCl_3$ gas after the thermal oxidation growth, resulting in a peak channel mobility of 89 $cm^2/V·s$, which is much higher than the nitridation process [81]. Great efforts have also been made to explore high-k dielectrics such as Al_2O_3, MgO, HfO_2, etc. as potential alternatives to SiO_2 in the last two decades. In general, high-k dielectrics cannot be used alone. A thin oxide film should be formed before the deposition as shown in Fig. 5. A peak mobility of up to 300 $cm^2/V·s$ has been demonstrated in [82] using an Al_2O_3 film.

Table V lists the interface quality and channel mobility by different gate oxide formation processes. Good control of the MOS interface and accurate characterization remain big challenges. Despite the great efforts to improve interface quality, the interface state density of 4H-SiC is still far from a satisfactory level.

C. Ohmic contact formation

Simultaneous ohmic contacts – a contact of a single profile that is used for both n-type and p-type regions are preferred to lower the process budget. For SiC, there are few metals that pose as viable single-metal for creating ohmic contacts. The three most important factors involved in contact formation are resistivity, thermal stability, and compatibility with the rest of the process. For a low temperature CMOS process, the thermal stability and compatibility are less of a concern, so any ohmic contact which can achieve a low specific contact resistivity is suitable.

In terms of already-explored contact profiles, there are a few different routes which should be taken into consideration. A Ni-based contact is easy to form and works fairly well for n-type and p-type SiC. It yields a low resistivity with highly doped SiC, so this is the most commonly used metal for creating an ohmic contact [91].There are a few reasons which explain why Ni is suitable for contact formation with SiC. Firstly, Ni can react with SiC at temperatures between 600°C and 1000°C, allowing it to form phases (Ni_2Si and $Ni_{31}Si_{12}$) which are ohmic. Additionally, Ni is fairly easy to deposit, as compared to other comparable metals such as Mo or W. In terms of its performance, Ni can achieve specific contact resistivities in the range of ρ_c ~1E-6 $\Omega·cm^2$ with very highly doped SiC or minimum ρ_c ~1E-3 $\Omega·cm^2$ with highly doped SiC. Similarly to Ni-based contacts, another viable contact metal is Ti. In the case of Ti-based contacts, an ohmic contact can be formed directly with n-type SiC after deposition due to its low work function. It also has compatible phases with SiC including TiSi, TiC, Ti_5Si_3, $TiSi_2$, and the ternary Ti_3SiC_2 phase. This ternary phase can form an ohmic contact with ρ_c~1E-5 $\Omega·cm^2$ after annealing at temperatures above 900°C.

Both the Ni- and Ti-based contacts form low resistivity ohmic contacts with SiC after being annealed at sufficiently high temperatures, though these are rudimentary systems. Roccaforte et al. [92], [93] provides more comprehensive tables of Ni- and Ti-based contact systems for n-type and p-type SiC and their resulting resistivities. Excluding more exotic metals, such as Mo, Ta, Co, W, and others, some common contact profiles including Ni/Al, Ti/Al, Ni/Ti/Al, and Ti + Al/Ni.

In terms of non-exotic metal contact profiles, Ni-based profiles generally dominate in performance and simplicity. When it comes to thermal stability though, Ti is a better option for example. Out of the profiles included in Table VI, the Ni/Ti/Al profile achieves the highest performance.

TABLE VI. COMMON OHMIC CONTACT PROFILES AND PARAMETERS FOR SIC

Contact	Ratio/Thickness [nm]	Annealing	ρ_c [$\Omega \cdot cm^2$] (n+)	ρ_c [$\Omega \cdot cm^2$] (p+)	Ref.
Ni	200	1050°C – 10min	6E-6	1.5E-4	[94]
Ni/Al	5-6% Al	1000°C – 5min	1.8E-4	1.2E-2	[95]
Ti	100	1000°C – 15min	6.7E-5		[96]
Ti/Al	31% Ti	1000°C – 2min		2.5E-4	[97]
Ni/Ti/Al	80/30/80	950°C – 5min	7.8E-5	4.2E-5	[98]
Ti + Ni/Al	70 + 200/50	950°C -60s		2.3E-4	[93], [99]

IV. SiC Device Review

In this section, the performance of the SiC MOSFETs along with the resistors and capacitors as the basic and most important components are presented.

A. SiC MOSFETs

i. Basic Characteristics of SiC MOSFETs

While the material SiC may be highly reliable due to its high electric breakdown strength and negligible leakage currents at high temperature, SiC MOS devices are expected to be limited by the factors such as the quality of epitaxial layer, oxide growth process, etc. [100]. During the early stage of commercialization, the reliability of SiC devices did not achieve the requirements of their silicon equivalents. The reliability issue caused by the gate field (~V_{GS}) dominated failure and the drain field (~V_{DS}) dominated failure under harsh environments has not been completely broken through. In particular, gate oxide integrity (GOI) is the most important cause of the low reliability of SiC MOS devices [101]. There have been mature characterization methodology and stress techniques to investigate the reliability of MOS devices. Regarding the gate field related reliability, time-dependent dielectric breakdown (TDDB), bias-temperature instability (BTI) and hot carrier injection (HCI) are among the major assessments of long-term reliability of gate oxide [102], [103]. For the drain field related reliability, high-temperature reverse bias (HTRB) is commonly adopted with V_{DS} bias near avalanche. Neutron-induced single event burnout (SEB) on SiC MOSFETs is also one of the most important sources of device failures and needs to be resolved [104]. The neutron flux is on the order of 10 neutrons/cm^2/h (>10 MeV) according to the JEDEC Standard JESD89A [105]. Moreover, the high-temperature operating life (HTOL) reliability stress is also applied to devices to determine their intrinsic reliability as a lifetime test.

Among all the SiC CMOS technologies, Raytheon HiTSiC process is a high manufacturing readiness level CMOS technology, which achieves a good threshold voltage matching of n-channel and p-channel MOSFETs operating up to 400°C [106]. This process employs two separately doped n- and p-wells on n+ epi wafer as shown in Fig. 6(a) targeting 15 V operation. The MOSFET threshold voltage and channel mobility related to the interface traps density are among the most important parameters to evaluate the CMOS process. Fig. 6(b) presents the typical characteristics of an n-channel and a p-channel MOSFET with gate width of 20 µm and gate length of 2 µm at room temperature fabricated by Raytheon HiTSiC process. The extracted field-effect mobility is 25 cm^2/V·s and 6.8 cm^2/V·s for n-channel and p-channel MOSFET, respectively. Moreover, the characteristics of MOSFETs at high temperature up to 400°C were measured [107]. Figs. 7(a) and 7(b) show the extracted threshold voltage of n-channel and p-channel MOSFETs decreases monotonically as the temperature rises. The transconductance in Figs. 7(c) and 7(d) shows a slight increase with temperature increased, before falling as the temperature rises above 200°C. The reduction observed at high temperature is potentially linked to the lower bulk mobility due to increased phonon scattering. The field-effect mobility does not vary a lot according to the transconductance in Fig. 7 (c) and 7(d).

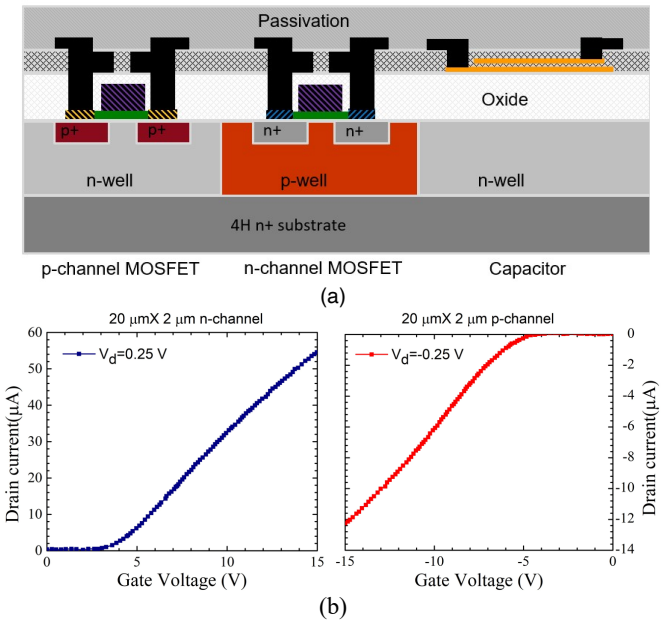

Fig. 6. (a) Cross section of Raytheon's HiTSiC process as in [107], (b) Id–Vg characteristics of a n-channel and a p-channel MOSFET with 20 µm x 2 µm at room temperature (reproduced from [107]).

Table VII presents a summary of the n-channel and p-channel MOSFETs reported by various groups including the information of gate oxide thickness, results of threshold voltage, the field-effect mobility, and the range of temperature. In general, the p-channel MOSFET has a relatively larger threshold voltage than n-channel due to lower field-effect mobility and the use of n-type polysilicon as the gate.

Besides the device performance research at high temperature, it is also essential to evaluate the device performance under high-radiation environment. Over the past decade, the total

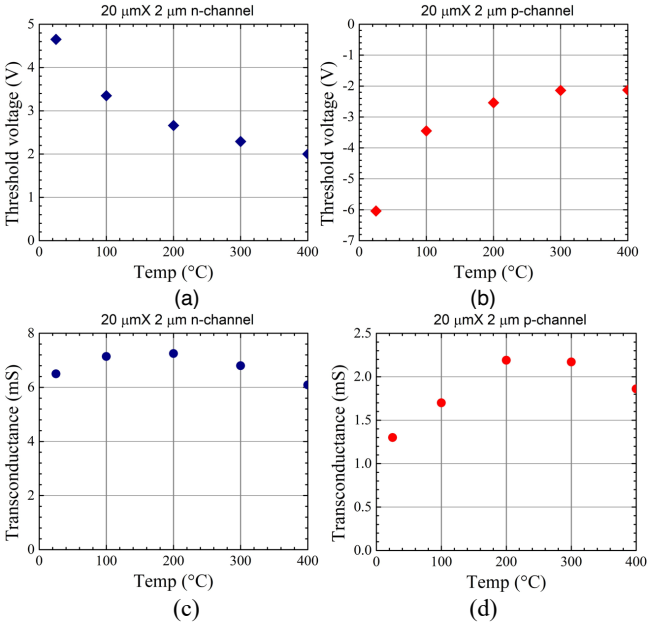

Fig. 7. Extracted threshold voltage for (a) n-channel MOSFET, (b) p-channel MOSFET; peak transconductance for (c) n-channel MOSFET, (d) p-channel MOSFET (reproduced from [107]).

TABLE VII. PERFORMANCE SUMMARY OF 4H-SIC MOSFETS

Company/R&D institute	Device	Gate oxide thickness (nm)	Threshold voltage (long-channel) at room temperature (V)	Peak channel field-effect mobility ($cm^2/V•s$)	Maximum characterization temperature (℃)	Ref.
IBM-CNM	NMOS	-	11	12	-	[16]
	PMOS		-2	2.3		
Raytheon U.K.	NMOS	40	4.1	25	400	[107]
	PMOS		-5.8	6.8		
GE	NMOS	50	~ 4.5	20	500	[108]
	PMOS		-	-		
Hitachi	NMOS	50	5.0	15	-	[25]
	PMOS		-10.0	5.2		
	NMOS	12.5	3.8	-	500	[109]
	PMOS		-2.9	-		
	NMOS	8	2.6	5.0	N.A.	[39]
	PMOS		-2.3	2.6		
Fraunhofer	NMOS	30	1.4	21	400	[110]
	PMOS		-3.6	10.2		
University at Albany, OSU&NCSU	NMOS	50	5.6	20	200	[111]
	PMOS		-8.5	9.5		

ionizing dose (TID) radiation hardness of commercial Si CMOS technologies has been evolving rapidly, while the exploration of SiC CMOS under TID radiation remains an area that requires further investigation. Regarding 4H-SiC CMOS technology, Masunaga, et al. [39] reported the degradation of threshold voltage and mobility of fabricated n-channel and p-channel MOSFETs. The threshold voltage of n-channel and p-channel MOSFETs were shifted in the negative direction as shown in Figs. 8(a) and 8(b), respectively. The drain leakage current increased with increasing integral dose especially for n-channel device, the leakage current exceeded 1 µA at 2.2 MGy. The dependence of the field-effect mobility on the integral doses for both types of MOSFETs in Fig. 8(c) shows that the mobility hardly changes below 2.2 MGy. This paper comes to the conclusions: (1) a thin gate oxide would help to reduce the threshold voltage shift by irradiation; (2) the incorporation of an oxynitride protective layer at the SiC/SiO_2 interface effectively mitigates the degradation of mobility induced by gamma radiation.

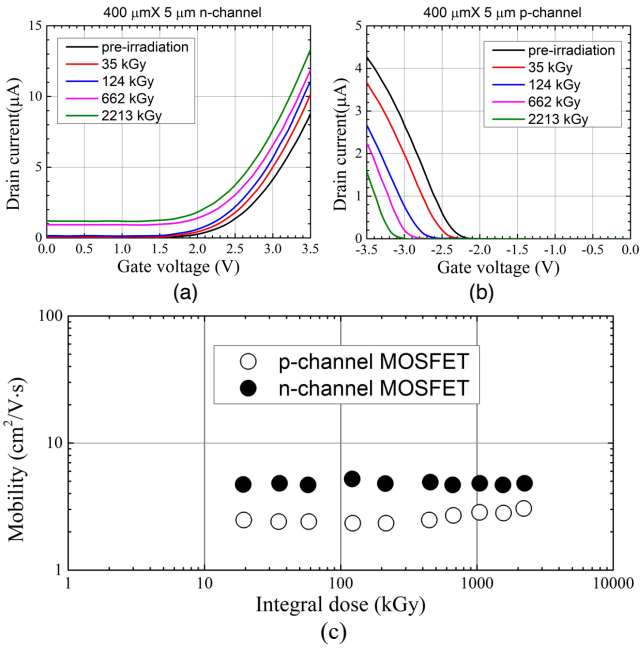

Fig. 8. Id-Vg curves with different integral doses for (a) n-channel MOSFET, (b) p-channel MOSFET; (c) dependence of field-effect mobility on the integral dose for the n-channel and p-channel at 1 kGy/h (reproduced from [39]).

When developing the CMOS IC technology, it is necessary to match n- and p- channel device characteristics such as the threshold voltage, drain current, especially for the inverter. In [112], an inverter with relatively good mathcing design was reported with operating temperature up to 200℃. As shown in Fig. 9, the switching voltage is found to be (9.2 ± 0.7) V. The benefits of SiC devices and ICs over Si counterparts under harsh enviroments are not fully realized until reliable and efficient devices and ICs are achieved. In summary, SiC MOS devices still have tough barriers to overcome. The main obstacles have been the low channel mobility related to the high interface trap density at the SiC/SiO_2 interface and the high resistance of the P-type ohmic contact. The research focus

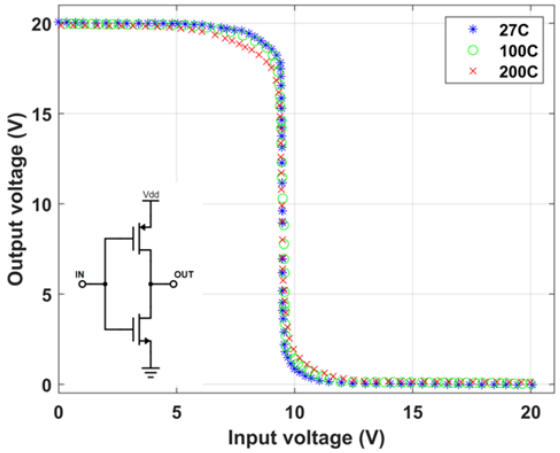

Fig. 9. Measured voltage transfer characteristics of the SiC CMOS inverter at different temperatures. The NMOS size is 20 µm x 6 µm and the PMOS size is 80 µm x 6 µm. The supply voltage of the process is 20 V (reproduced from [112]).

would be the channel region doping design, optimization of oxide formation (such as thickness, and POA condition) and ohmic contact with low resistance. There are tradeoffs among the expected parameters during the MOSFET device design. A CMOS device design window of process parameters (such as channel doping, gate oxide thickness, channel length) vs. device performance parameters (such as threshold voltage, short-channel effect, turn-on current and so on) used in Si CMOS [113] can be considered and developed to obtain the suitable ranges of the process parameters. Overall, the design and optimization of SiC CMOS devices still need further investigation.

ii. Modeling

Accurate compact models are among the most critical steps in realizing ICs. Currently, there are few robust models developed for lateral SiC MOSFETs. A compact model appropriate for n-channel SiC MOS devices was proposed by Kashyap et al. [114]. A novel parameter extraction approach was presented in their work to improve the modeling of the subthreshold section. The small-signal (transconductance, output resistance) and capacitance properties were not optimized in the article, however. Additionally, the SiC MOSFET's body effect, sometimes referred to as the back gate effect, which differs dramatically from that of a Si device, is not modeled. Modeling of impacts linked to interface states and geometry scaling are also not provided. A more thorough compact model of SiC n-channel MOSFETs was published by Mudholkar and Mantooth [115]. The main disadvantage of this approach is that iterative techniques are needed to solve the surface potential equation (which uses the flat band voltage formula), which increases simulation time and makes convergence challenging.

Although BSIM3v3 [116] has been used to design numerous MOS transistors, SiC MOSFET DC properties cannot be accurately modeled by BSIM3v3. These are some of the important causes for this deficiency.

a) There is no opportunity to submit SiC material properties as inputs because BSIM3v3 was created exclusively for Si technology. This leads to erroneous readings for material-dependent metrics such surface potential during strong inversion, intrinsic carrier concentration, flat band voltage, etc.

b) In BSIM3v3, there is no enhanced mobility model that can take Coulomb scattering effects (induced by interface trapped charge) into account. This impact is more pronounced when body bias is present in the area of low current where the device is beginning to undergo a significant inversion. Therefore, reliable modeling of Id-Vg characteristics with body bias is not possible. The disparity between SiC NMOS modeling transfer characteristics and BSIM3v3 is shown in Figs. 10(a) and 10(b). The inaccuracy is minimal at zero body bias for drain currents larger than 1 μA. Nevertheless, the RMS error is also significant at body bias of 3 V (67%) and 6 V (233%).

The soft transition from the subthreshold to the strong inversion area is not modeled by any formulation in BSIM3v3. The challenge BSIM3v3 encountered when simulating this behavior of SiC MOSFETs can be seen in Figs. 10(c) and 10(d). Even at zero body bias, the mismatch might reach 10% at the beginning of the saturation area [118].

Although BSIM465 [117] has a mobility model for a non-SiO_2 gate oxide and non-Si substrate, the main drawback is that it cannot simulate the body effect. Figs. 11(a)-11(d) demonstrate the challenges BSIM465 encounters while simulating the transfer properties in SiC NMOS [118]. RMS errors for BSIM465 are greater than 40% at nonzero body bias despite being quite small when body bias is zero. The BSIM4 model's inversion charge expression and a modified version of the drain current equation represent the physical strategy for simulating the impact of interface states on the device characteristics.

Lower transconductance of SiC MOSFETs on the 4H-SiC polytype in contrast with 6H-SiC results from significant entrapment of inversion electrons because of more density of traps at the oxide-semiconductor interface. In both polytypes, density of traps exhibits an increase towards the conduction band edge. It has been noted that artificial peaks in density of traps near valance band edge (in a p-type semiconductor) can be observed through Gray-Brown analysis when the trap's capture cross-section experiences rapid variations with energy [119]. For n-type SiC MOSFETs, the unit area interface trapped charge can be estimated as [118], under the sheet charge layer assumption

$$Q_{it,nMOS}(\Phi_S) = q\int_{E_i}^{E_F} f(E)D_{it}(E)dE$$

$$= q\left\{D_{it,mid}\Phi_S + D_{it,edge}\sigma_{it}exp\left(\frac{E_i-E_C}{\sigma_{it}}\right)\left[exp\left(\frac{\Phi_S}{\sigma_{it}}\right)-1\right]\right\} \quad (1)$$

Similarly for p-type SiC MOSFETs

$$Q_{it,pMOS}(\Phi_S) =$$

$$q\left\{D_{it,mid}\Phi_S + D_{it,edge}\sigma_{it}exp\left(\frac{E_v-E_i}{\sigma_{it}}\right)\left[exp\left(\frac{\Phi_S}{\sigma_{it}}\right)-1\right]\right\} \quad (2)$$

where Φ_S refers to the surface potential, σ_{it} is a parameter that represents the tail of the density of states (DOS), E_C is the conduction band energy, E_v is the valence band energy, E_i is the intrinsic Fermi level, $D_{it,edge}$ and $D_{it,mid}$ are the conduction band edge and mid-gap DOS (typically a fixed number), respectively. The challenges in integrating component (1) into the BSIM4 core model stem from significant differences in the charge expression's relationship with surface potential compared to established inversion charge relationships [118]. This inconsistency prevents the use of existing effective gate-to-source voltage expression, V_{gsteff}, for drain current calculation. Consequently, new equations and parameter extraction methods are needed, but incorporating them conflicts with BSIM4's proven features. While implicit equations relating inversion and interface trapped charges can be formulated, their reliance on numerical methods makes them unsuitable for compact modeling. Adding interface trapped charge to intrinsic current and charge equations increases model complexity and simulation time, while the resulting intricate and implicit equations often lead to convergence issues in compact models.

The transformation of the BSIM4 model into BSIM4SiC published by Shamim et al. [118] follows a systematic approach to incorporate the influences of interface trapped charges. In the initial step, the SiC MOSFET is modeled using HSPICE BSIM465, and any unaccounted features are identified. Moving

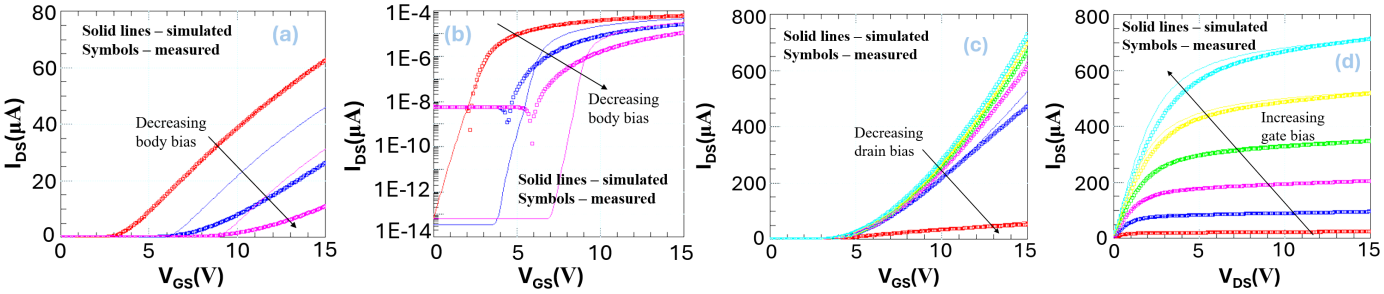

Fig. 10. The transfer characteristics of (a) strong inversion region, (b) subthreshold region simulated with different body bias, (c) strong inversion with different drain bias and (d) output characteristics simulated with BSIM3v3 (reproduced from [118]).

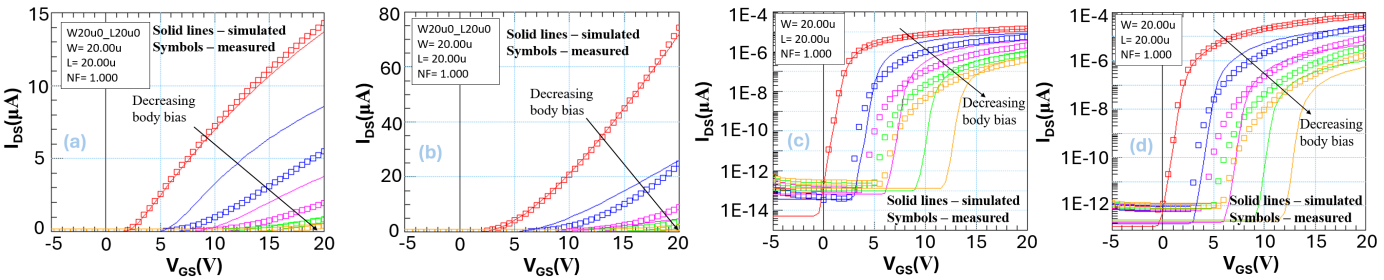

Fig. 11. The transfer characteristics of (a) strong inversion region with V_{ds}=0.5V, (b) strong inversion region with V_{ds}=15V, (c) subthreshold region V_{ds}=0.5V, and (d) subthreshold region V_{ds}=15V simulated with different body bias, simulated with BSIM465 (reproduced from [118]).

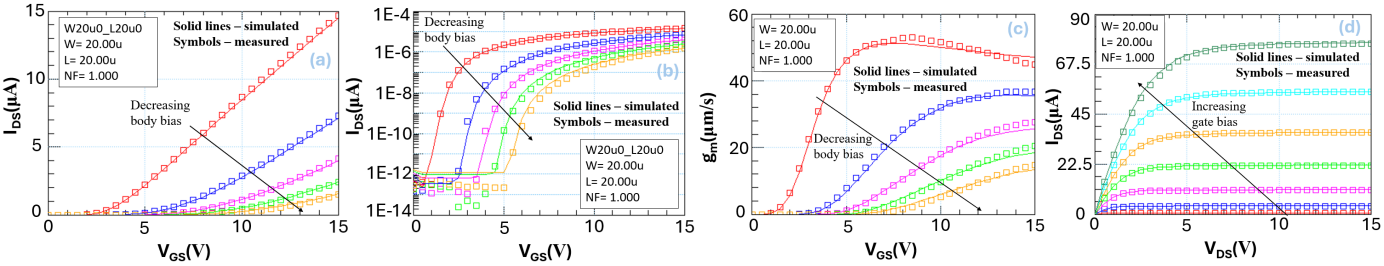

Fig. 12. The transfer characteristics of (a) strong inversion region with V_{ds}=0.5V, (b) subthreshold region simulated with V_{ds}=0.5V, (c) transconductance with different drain bias and (d) output characteristics simulated with BSIM4SiC (reproduced from [118]).

on to step two, a thorough examination of the physical phenomena causing these unmodeled features is conducted. For instance, the reduction in mobility at low vertical fields is attributed to Coulomb scattering, whereas at high vertical fields, it stems from surface roughness scattering. In step three, an assessment is made to determine whether BSIM4 already contains model formulations that address these relevant physical phenomena. For example, BSIM470 incorporates an advanced mobility model that considers the impact of Coulomb scattering on mobility reduction. Step four involves the modification of the BSIM470 model to integrate these effects. This can be achieved by either adjusting existing equations or introducing new ones. For instance, in the revised mobility equation, components related to body bias are introduced to simulate mobility reduction with varying body bias. Lastly, in step five, a new parameter extraction sequence is developed. This is necessary because the traditional sequence is no longer suitable after the original code has been updated [118]. The model fit results with the BSIM4SiC model are demonstrated in Figs. 12(a)-12(d). Not only the transfer characteristics curves in strong inversion and subthreshold, but also the transconductance and output characteristics curves have shown good match with the experimental results. Recently, a modified threshold voltage extraction method is also implemented to improve the threshold voltage measurement, especially considering the high temperature operation [120].

In summary, developing compact models for SiC MOSFETs based on the device physics is time consuming and challenging but needed for the circuit and system designers.

B. SiC passive components-resistors and capacitors

Finding discrete resistors and capacitors that operate reliably under harsh environments especially above 300°C poses a challenge. Developing integrated resistors and capacitors offers local matching or temperature tracking and can reduce packaging complexity and size [121]. Here we briefly present the resistor and capacitor options in SiC CMOS technology.

The common options of on-chip resistors mainly have: N-well, P-well, N+ and P+ implanted resistors which are created through the process of ion implantation. The resistance values first decrease when ionization increases with increasing temperature [12]. However, at a certain point, the mobility decreases as the scattering increases and the values may have a negative temperature coefficient especially for the N-type resistors as reported in [106]. The sheet resistance of N+ regions from room temperature to 400°C by extracting the data of Van Der Pauw test structures increases due to increased phonon scattering.

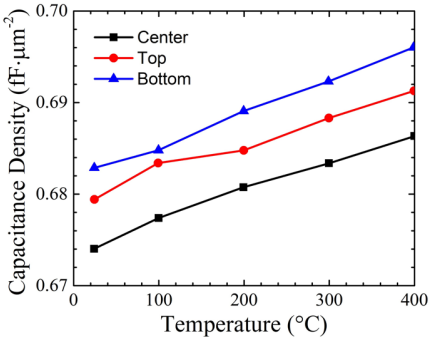

Fig. 13. Capacitance versus temperature over 3 sites on a wafer (reproduced from [106]).

The capacitor is arguably the most complex and difficult component to fabricate, especially for high-temperature applications. The lack of high-temperature capacitors limits the SiC IC development especially when it comes to the ones with high capacitance. The most common architecture is the sandwich-like structure that a dielectric is between two plates. The operation concerns at high temperature are mainly related with the leakage current, defects and the dielectric constant [122]. There is a tradeoff between the leakage current and the thickness of the dielectric. MOS capacitor using the same MOSFET gate oxide layer is the easiest structure for on-chip integration. The small dielectric constant of the gate oxide determines that a large area is needed for a high capacitance value capacitor. Raytheon U.K. designed an integrated capacitor as shown in Fig. 7(a) by using the polysilicon gate layer and a second layer of polysilicon deposited over a thin dielectric layer, resulting in a capacitance density (i.e., capacitance per unit area) of approximately 0.7fF•μm^{-2} [106]. The capacitance variation from room temperature to 400°C is less than 2% as shown in Fig. 13.

V. SiC Integrated Circuit Review

SiC IC technology aims to integrate elements to form analog and digital circuit functions. As the SiC CMOS IC technology advances, various groups have reported the development of ICs for diverse applications. The University of Arkansas and Ozark Integrated Circuits have been conducting research and development of on-chip SiC systems for high temperature operation using the 1.2 μm HiTSiC process of Raytheon U.K. [123]. Circuits such as an 8-bit DAC and ADC were demonstrated for the first time from 25°C to 400°C [124]. With the same process, a gate driver shown in Fig. 14 was fabricated and packaged for the characterization over a wide temperature range. This gate driver was capable of driving a power MOSFET at temperatures exceeding 500°C without significant degradation [125]. In addition, over 15 types of integrated circuits including ring oscillator [126], linear voltage regulator [127], voltage and current references [128], PWM generator [129], and an RS-485 transceiver [130] were developed. These circuits were designed for operation at a 15 V supply voltage. The CMOS ring oscillators achieved a maximum operating frequency of approximately 12 MHz at room temperature and increased to approximately 32 MHz at 400°C [126]. The ring oscillator operated continuously for 24 hours at 470°C. At that point, the circuit continued oscillating but no longer responded to changes in the input enable signal. The group concluded that

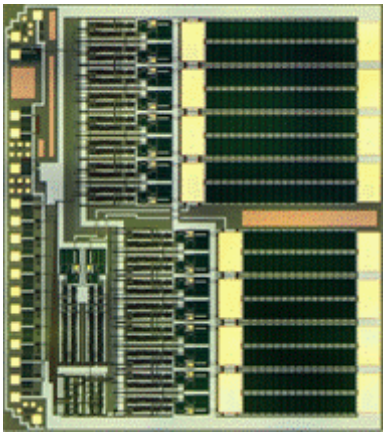
Fig. 14. SiC CMOS gate driver- dimensions: 5.0 mm x 4.5 mm [125].

enhancing the packaging system is essential for the long-term functionality of these circuits, as most failures were linked to packaging rather than circuitry. A two-stage operational amplifier (op-amp) was tested from room temperature up to 400°C [131]. Throughout this range, the measured DC gain of the op-amp fluctuates between 60.6 and 64 dB, while the unity gain bandwidth (UGBW) varies between 3.2 and 2.3 MHz. Moreover, the phase margin exhibited a maximum of 69° and a minimum of 36°. The measured results of the three-stage comparator indicate that the propagation delay varies depending on the overdrive voltage applied to it [131]. At lower overdrive voltages, such as 0.25 V at 25°C, the propagation delays were significantly higher, reaching 500 ns. When an overdrive voltage of 2 V was employed, the propagation delay of the comparator was reduced from 220 ns at 25°C to 123 ns at 550°C. To acquire a foundational understanding of thermal cycling dynamics, the linear regulator was tested for 30 hours at 300°C [127]. A 1.33% fluctuation in output voltage suggests consistent performance throughout the test. However, this investigation did not aim to draw any long-term reliability conclusions. Further research into the long-term reliability of SiC CMOS is necessary as the fabrication processes continue to mature. The University of Arkansas team also collaborated with Fraunhofer IISB to develop a 4H-SiC CMOS process and designed several ICs in that process [132]-[134]. This section will review SiC ICs designed for analog, mixed-signal, RF, digital, and hybrid power modules applications.

A. Analog, Mixed-signal & RF ICs

SiC's wide bandgap and superior thermal conductivity enable it to function at significantly higher temperatures for various critical applications such as hybrid vehicles, diesel engines, deep earth drilling, and aviation/aerospace needs [129]. These applications demand power conversion and voltage regulation at elevated temperatures, alongside essential sensing and monitoring systems for protection, data acquisition, and on-site control. To meet these requirements, there is an increasing demand for integrated circuits specifically designed to interface with high-temperature sensors. A signal conditioning system coupled with a sensing node designed for high-temperature environments can actively monitor crucial parameters like temperature within industrial machinery, such as gas turbines. Real-time monitoring aids industries in accurately scheduling maintenance for expensive equipment. SiC circuits, operational

at higher temperatures without requiring additional cooling systems or thermal isolation, hold the potential to significantly lower system costs and size while simultaneously enhancing operational reliability. NPN transistor-based ICs were fabricated in the in-house SiC low-voltage bipolar technology and exhibited functionality above 450°C [135]-[138]. The main limitation of the SiC bipolar process is excess standby power consumption because the process does not have a complimentary PNP device. Several integrated circuits were documented using a 4H-SiC all-NMOS process [139]-[143]. However, the absence of PMOS devices posed challenges for designing complex circuitry. With the advancement in SiC CMOS technology, several sensor ICs have been reported in SiC CMOS technology [144]-[146]. To establish high-voltage high-temperature power conversion and regulation systems, data acquisition and transmission systems, several analog and mixed-signal circuits have been reported in the SiC CMOS process [37], [124]-[128], [130], [131], [147]-[149].

B. Digital ICs

Implementing digital controls in the proximity of power devices in high-temperature environments can reduce critical delays and enhance overall system stability. Silicon carbide demonstrates the ability to create the necessary components for a digital microprocessor, like combinational and sequential logic cells, as well as static random-access memory (SRAM). Despite SiC circuits' resilience to high temperatures, they can still be affected by timing issues caused by extreme temperatures. To mitigate these problems, one approach is to avoid global clocked control and opt for an asynchronous circuit architecture employing a local handshaking scheme. A complex digital integrated circuit design methodology employing both synchronous and asynchronous logic and several digital ICs have been demonstrated in the SiC CMOS process for extreme environment system applications [38], [126], [129], [150]-[154]. In the architecture of any complex system, a pivotal element is the microprocessor. A microprocessor brings intelligence and programmability to diverse applications. In the context of planetary exploration, this implies the ability to adapt instruments on the spot to address unexpected challenges, such as changes in the environment or hardware malfunctions. Microcontrollers, which integrate data converters and various mixed-signal components with a versatile processor and memory, prove highly beneficial for intelligent systems. SiC CMOS technology will be a good fit to design these complex circuitries that can be used for Venus as well as terrestrial applications. Recently, high-temperature functional SRAM has been designed in SiC CMOS technology to integrate with electronic systems and enable data storage in harsh environments[112], [132].

C. Hybrid Power Modules

The motivation behind designing ICs in wide bandgap SiC stems from harnessing SiC's properties to create a system compatible with SiC power devices such as power FETs and insulated gate bipolar transistors. These devices are increasingly popular in high voltage and power applications due to their exceptional features such as high switching speeds, minimal power loss, and superior breakdown voltages [155]. Integrating control, protection, and driver circuitry with the power device within the same technology process eliminates the need for additional cooling, protection, and passive components. Consequently, it optimizes power density by reducing board area, parasitic elements, wire routing lengths, power loss, and overall costs in high-voltage and high-power systems [143]. An integrated SiC CMOS gate driver was designed for power module integration with a power MOSFET [125]. An undervoltage lock-out (UVLO), which is a subcomponent of the protection circuitry of a gate driver was demonstrated in a 4H SiC-based process for use in a plug-in hybrid vehicle charger [156]. A digitally controlled pulse width modulation (PWM) generator was designed for boost converter application and was functional for over 50 hours at 300°C [129].

Table VIII summarizes several integrated circuits reported in SiC CMOS technology along with their prospective applications.

TABLE VIII. INTEGRATED CIRCUITS IN SIC CMOS TECHNOLOGY WITH APPLICATIONS

Integrated Circuits	Temperature	Applications	Ref.
Analog			
Voltage and Current references	540°C	Supporting circuits for high-temperature data acquisition systems	[128]
Op-amp, Comparator	400°C, 550°C	Power converter applications	[131]
Voltage regulator	400°C	Power management for SiC gate driver	[127]
Gate driver	Above 500°C	To drive SiC power MOSFET	[125]
Temperature sensor (CTAT)	200°C	Harsh environment sensor applications	[144]
UV image sensor	200°C	Image sensor system	[145]
Sun position sensor	-	Satellite attitude control	[146]
Mixed-Signal			
Data converters (ADC, DAC)	400°C	High-temperature data acquisition	[124]
Schmitt trigger	300°C	To offer protection against system noise.	[147]
Phase-locked loop (PLL)	150°C	High-temperature applications	[148]
RS-485 transceiver	400°C	High-temperature data acquisition and transmission system	[130]
Digital			
NCL counter, Boolean FSM, DAC controller	Above 300°C	To monitor high-temperature diesel engine environments	[38]
Ring oscillator, clock generator, 8-bit register	500°C	Venus surface application	[126]
PWM generator	400°C	Motor control and switching converter applications	[129]
SRAM	300°C	To enable data storage at high temperature	[132]

VI. Monolithic Integration Development

Many LV ICs based on all-SiC platform have been successfully realized and reported in recent years. Meanwhile, various types of discrete SiC power devices have been well developed and commercialized. The monolithic integration of SiC CMOS and SiC power devices has become an attractive trend because it will definitely benefit some applications, especially for the high-frequency operation due to its reduced parasitic effects. However, so far, there are few practices of the integration of the LV ICs with high-voltage power components on the same chip.

In [157], the possibility of 4H-SiC CMOS integration with a HV vertical double-implanted MOS (DMOS) is experimentally validated. The body effect on the behaviors of PMOS and CMOS inverter induced by the high substrate voltage has been observed. In order to mitigate the body effect, the PMOS must be isolated from the n-type substrate which serves as the drain of the HV MOSFET. Thus in 2022, this institute presented the first integration of a 10 V CMOS logic circuit, 20 V gate driver, and 600 V VDMOSFET with junction isolation considered [158], [159]. The AIST group demonstrated the first monolithic SiC power IC integrating a 1.2 kV-class vertical NMOSFET with a CMOS gate buffer in 2021 [13]. At the same time, the groups of University at Albany, NCSU, and OSU reported the monolithic integration of lateral HV NMOSFET with LV CMOS on a 6-inch 4H-SiC substrate fabricated at ADI which lacked the isolation [71]. They modified the epi stack such that the HV devices and circuits are completely isolated from their LV counterparts [111].

In short, isolation optimization between the HV power device and LV CMOS components has to be seriously taken into consideration for the monolithic integration development. Meanwhile, there are tradeoffs to choose a vertical or lateral design of a HV power device integrated with the LV CMOS. The biggest disadvantage for the integration technology with lateral HV MOSFET is that a blocking voltage over 1.2 kV is difficult to achieve, while for the technology with vertical architecture power MOSFET, the main costs are: 1) the noise caused by the vertical architecture of the power device affects the performance of CMOS circuitry; 2) a more complicated process flow is involved; 3) multiple power MOSFETs cannot be integrated on the same chip if they operate at different states.

VII. Summary

Recently, operations in harsh environments such as high temperature, high irradiation are required in certain fields such as automobiles, space exploration, nuclear reactors, etc. The need for semiconductor technology using wide bandgap materials that exceed the physical limits of Si is increasing. This paper describes the challenges and progress made toward the IC development based on SiC CMOS technology. A systematic review of SiC CMOS technology in terms of process development, device performance, IC applications, and monolithic development has been presented. Examples of CMOS circuitry that have been successfully designed, fabricated and tested are provided.

The development of SiC CMOS technologies is still in a nascent phase, and we are facing a lot of challenges including material defects, metallization, reliability issues and so on. However, SiC CMOS technology shows great potential in achieving application-specific ICs for extreme-environment electronics.

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