# An 82dB-SNDR Input-Driving-Relaxed Noise-Shaping SAR with Amplifier-Reused In-Loop Buffering and NTF Leakage Reshaping

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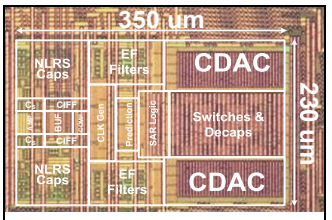
The noise-shaping successive-approximation register (NS-SAR) ADC is increasingly deemed as a promising digitizer architecture for high-resolution sensing and low-power wireless links. Many prior arts strove to attain superior energy efficiency by exploiting open-loop amplifiers and error-feedback (EF) structures [1]-[2]; but they are sensitive to PVT variations. While calibration can be employed to stabilize the open-loop amplifier [2], it consumes considerable power and area overhead. Another design challenge is the input driving of NS-SAR. As NS-SARs tend to target high-resolution with a relatively low oversampling ratio (OSR), the hardened kT/C noise requirement brings more stress to the input driver under the classic front-end sampling approach. Existing remedies include the buffer-in-loop (BIL) architecture [3]-[4] and kT/C noise cancellation [4]. However, BIL requires high supply voltage and incurs extra noise for the NS filter, whereas kT/C noise cancellation requires extra timing overhead.

This paper presents a 3rd-order NS-SAR design that effectively resolves both input driving and PVT robustness concerns. It highlights the use of an amplifier-reused in-loop buffering (AILB) scheme, which merges both input buffering and residue extraction into the comparator pre-amp. This scheme not only is free of high supply voltage and excess noise penalty, but also provides kT/C noise reduction inherently with no overhead. This work further features an NTF leakage reshaping (NLRS) technique that enables the NS to be insensitive to gain variation of the EF open-loop amplifier. The NLRS requires only a few switches and capacitors added on top of the AILB structure, which brings little impact on power efficiency.

Fig. 1 describes the proposed AILB scheme and compares it to the classic BIL approach. In AILB, during sampling, the CDAC no longer samples the input signal. Instead, it AC-couples the input signal to the pre-amp input, which drives the "offset capacitor" (now the actual sampling capacitor $C_S$) to track and sample the amplified signal. To avoid clipping the pre-amp under a large signal, the CDAC performs a preset operation prior to the sampling phase, where an approximated input voltage is generated using a digital predictor [5] and the pre-amp only needs to process the small incremental "prediction errors". During the SA conversion, with CDAC, noise shaping feedback, pre-amp and CS connected in series, the latch will see $G\cdot(V_{NS}+V_{DAC} - V_{IN})$, thus generating the decision the same way as conventional SAR. Like in BIL, the non-linearity of the pre-amp does not affect the result, and this allows the use of simple amplifier design. Note that during the first few MSB trials, the pre-amp may still saturate and corrupt the decision voltage. This can be solved by reusing the prediction result to skip a few MSBs. At the end of the conversion, an amplified version of the $V_{RES}$ is automatically available and can be transferred to the NS filter using a source follower (SF). The AILB scheme offers several merits: 1) It can be supplied with core voltage as the signal swing is small. 2) The AILB scheme can employ a current-reused amplifier (e.g. inverter-based amplifier) directly, unlike the BIL case where a level-shifter is needed to bias a push-pull buffer [4]. 3) The AILB inherently offers suppressed sampling kT/C noise without explicit cancellation. The CDAC preset noise is naturally cancelled due to the flipped polarity in CDAC and $C_S$. 4) This scheme incurs little noise penalty during VRES transfer since the SF noise is suppressed by the pre-amp gain.

As an amplified $V_{RES}$ is readily available at the SF output, it can be directly fed to a passive filter such as the FIR for EF structure. However, a key concern for EF-type NS implementation is the high sensitivity to coefficient drift. In this design, the main source of variation is the pre-amp gain. The gain error $\Delta$ will cause a leakage term $\Delta\cdot$FIR(z) in the NTF, which is not shaped and therefore degrades the NS quality. To overcome this issue, we propose the NLRS technique, as shown in Fig. 2. The NLRS is realized by adding negative feedback and positive feedback of the SF output back to the pre-amp input and SF input, respectively. Both feedbacks are implemented by charge sharing and capacitor stacking. In doing so, the effective $V_{RES}$ amplification becomes a 1st-order closed-loop filter, whose feedforward path consists of the pre-amp and an integrator formed by the positive-feedback SF. Such closed-loop signal flow desensitizes the impact of the pre-amp gain variation and defines the effective low-frequency residue gain by the charge sharing ratio of $C_{NLRS1/2}$ [6], leading to a robust $V_{RES}$ transfer. With NLRS, the leakage term due to gain error $\Delta$ will be reshaped to the 1st order (for 2nd-order EF) as shown in Fig. 2. Ping-pong capacitor pairs are used in light of the feedback needs to occur at the same time as $V_{RES}$ transfer. It is worth noting that while the NLRS shares similarities with the interstage gain error shaping of [6] in terms of fundamental concept, they differ in both usage context and implementation. The latter is a mixed-signal approach that requires extra DACs, whereas the NLRS is purely analog. The thermal noise contribution of the proposed NLRS is low, because the noise of the negative feedback ($1/G_D$) is canceled under the AILB operation, and the integrator noise gets attenuated like the SF noise.



Die micrograph.

Fig. 3 shows the circuit diagram of proposed NS-SAR incorporating both AILB and NLRS techniques. The 3rd-order NS is implemented with an EF-CIFF hybrid structure, where the EF path provides 2nd-order and the CIFF path provides 1st-order. The pre-amp design adopts an inverter-based amplifier with an explicit CMFB path. This allows the output common-mode voltage of the pre-amp stay near the ½ $V_{DD}$ over PVT variation, which further lowers the risk of pre-amp clipping under the impact of offset. The pre-amp also performs an auto-zeroing operation reusing the $C_{NLRS1}$ during the CDAC preset phase to further lower the offset. The pre-amp gain is chosen to be about 8 to provide sufficient kT/C noise suppression while keeping enough headroom for sampling the prediction error. The value of $C_S$ is chosen to be 300fF. The SF is duty-cycled to be activated only during $V_{RES}$ transfer. To cater for an OSR of 8, the digital prediction filter is chosen to be 3rd-order. Aligned-switching with detect-and-skip (DAS) is applied to the first 4 MSBs during preset and bit-trial to reduce CDAC reference power consumption.

The NS-SAR prototype is fabricated in 65nm CMOS and occupies an active area of 0.075mm$^2$. Operating at 8 MSPS and 1.2-V supply, the ADC consumes 126.8uW (breakdown in Fig. 4). The DAC mismatch is calibrated offline using least-mean-square (LMS) method. The measured output spectrum is shown in Fig.4 and the ADC achieved 82dB SNDR and 95.7dB SFDR over 500-kHz BW, respectively. The spurs occurring in the out-of-band region are caused by the memory effect in the mismatch transfer function that are not captured by the calibration algorithm. The measured dynamic range is 83.2dB. Fig. 5 shows measurement results for verifying the robustness, where the measured SNDR across 8 samples shows variation <1dB. The SNDR vs. different input frequency indicates the prediction works across the entire signal band. To verify the NLRS's effectiveness, we tune the pre-amp bias current to induce gain change and compare the SNDR under NLRS on/off. We also measured the SNDR sensitivity under different input $V_{CM}$, and it shows negligible SNDR change over 10% of VCM variation, indicating a better $V_{CM}$ tolerance over prior BIL design [4]. Fig.6 summarizes the performance and compares it with state-of-the-arts. The proposed design achieves 178.0dB FoMs and 12.4fJ/c-s FoMw respectively. Along with the competitive energy efficiency, this work further addresses the practical needs of input driving relaxation and robustness with new techniques that are simple and effective.

**Acknowledgement:**

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**References:**

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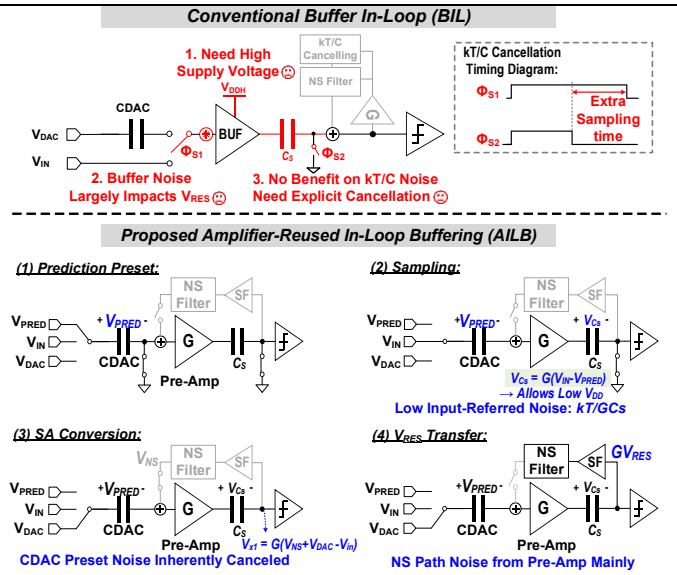


Fig. 1. Operation of the proposed AILB scheme and comparison with the classic BIL scheme.

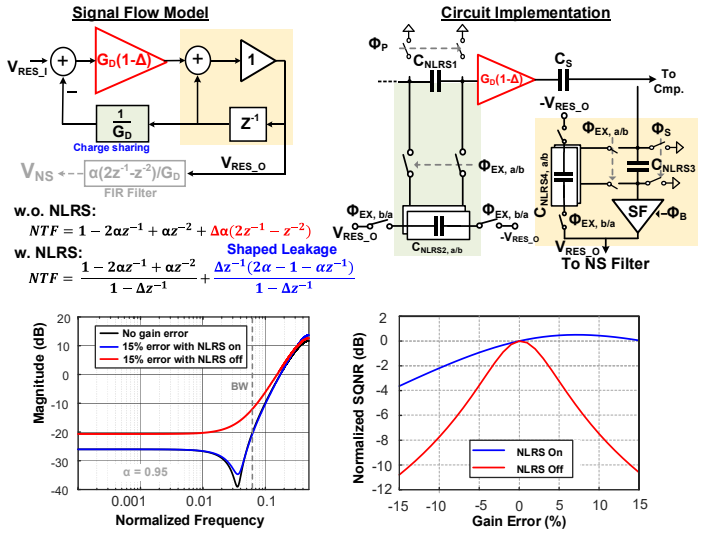


Fig. 2. Signal flow model and implementation of the proposed NLRS technique, with simulated NTF and SQNR comparison.

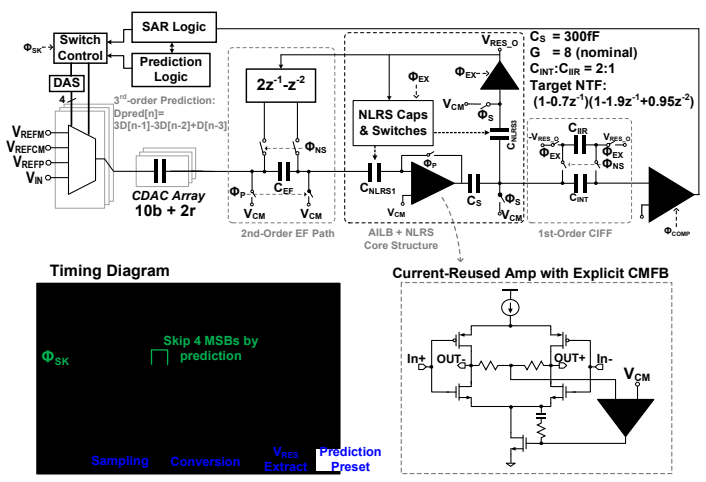


Fig. 3. Simplified schematic (shown as single-ended) and timing diagram of the proposed NS-SAR ADC.

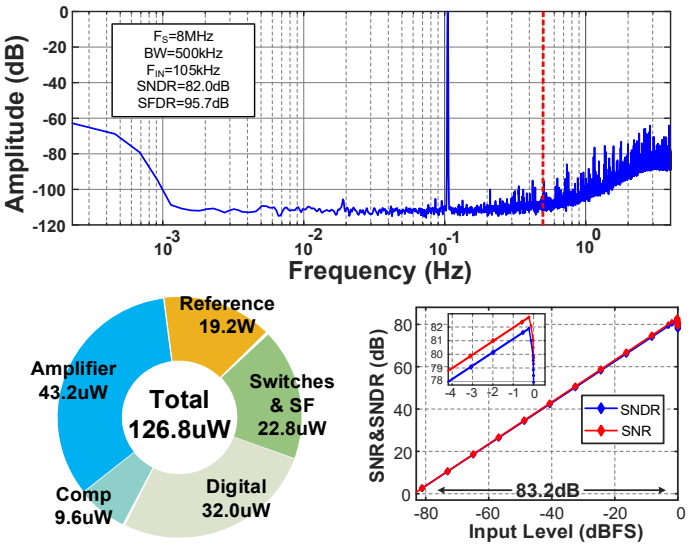


Fig. 4. Measured output spectrum (35k-points), power breakdown and dynamic range.

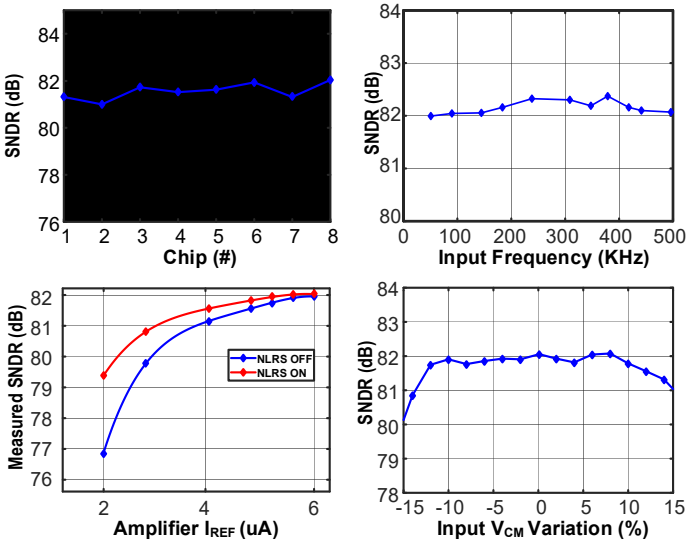


Fig. 5. Measured SNDR across multiple chips (TL), measured SNDR across different input frequency (TR), amplifier reference current (LL), and input VCM (LR).

| | ISSCC 20 X. Tang | ISSCC 20 L. Jie | CICC 19 T. Kim | ISSCC 22 T. Wang | ISSCC 23 M. Li | This Work |
|---|---|---|---|---|---|---|
| Process [nm] | 40 | 28 | 65 | 65 | 180 | 65 |
| NS Order | 2 | 4 | 2 | 4 | 0 | 3 |
| Residue Processing | Closed-Loop | Open-Loop | Passive | Open-Loop | N/A | Open-Loop |
| PVT Robust | ✓ | × | ✓ | × | × | ✓ |
| kT/C Noise Reduction | × | × | × | ✓ (Explicit) | × | ✓ (Intrinsic) |
| Input Buffered | × | × | ✓ | ✓ | ✓ | ✓ |
| Buffer Type | - | - | Source Follower | PPSF | FVF | Amplifier Reused |
| Supply [V] | 0.8/1.1 | 1 | 0.9/2.1 | 1.2/2 | 1.8/3.3 | 1.2 |
| Area [mm²] | 0.037 | 0.02 | 0.081 | 0.075 | 0.6 | 0.075 |
| Power [uW] | 107 | 120 | 2130# | 133.8# | 30410# | 126.8# |
| Fs [MS/s] | 10 | 2 | 80 | 5 | 12 | 8 |
| Bandwidth [kHz] | 625 | 100 | 2000 | 500 | 6000 | 500 |
| OSR | 8 | 10 | 40 | 5 | N/A | 8 |
| SNDR [dB] | 83.8 | 87.6 | 73.8 | 84.1 | 91.3 | 82 |
| DR [dB] | 85.5 | 89 | 77 | 84.9 | 94.1 | 83.2 |
| FoMs1* [dB] | 181.5 | 176.8 | 163.5# | 180.0# | 174.2 | 178.0# |
| FoMw** [fJ/step] | 6.8 | 30.8 | 133.0# | 10.2# | 84.4 | 12.4# |

* *FoMs1 = SNDR + 10*log10(BW/Power)*
** *FoMw = Power/(2^ENOB*2*BW)*
\# *Including Buffer Power*

Fig. 6. Performance summary and comparison with state-of-the-art high-resolution SAR ADCs.