Experimental Demonstration of Field-Free STT-Assisted SOT-MRAM (SAS-MRAM) with Four Bits per SOT Programming Line

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***Abstract*— SAS-MRAM has been proposed as a potential last-level cache SRAM replacement owing to its high speed (~1 ns), high cell density, and high endurance characteristics. Here, we report a first-of-its-kind experimental demonstration of simultaneous switching of 4 magnetic tunnel junctions (MTJs) with different polarity on the same spin-orbit torque (SOT) write line. We experimentally verify the novel SAS-MRAM writing scheme which overcomes the unique disturb modes found in the shared SOT line structure and enables simultaneous, field-free switching of multiple MTJs. The non-volatility of SAS-MRAM promises advantages in energy efficient computing applications such as edge AI over SRAM.**

***Index Terms*—Magnetoresistive random access memory, MRAM, spin-transfer torque, STT, spin-orbit torque, SOT, STT-assisted SOT, SAS, SAS-MRAM, field-free switching.**

I. Introduction

THE ever-growing demands of today's data-intensive computing ecosystem have necessitated radical innovations in memory system design. Spin-Orbit Torque Magnetoresistive Random Access Memory (SOT-MRAM) has emerged as one such nonvolatile memory technology which promises sub-ns switching speeds that could enable its use in SRAM-replacement applications (e.g., last layer cache and buffer memories), although several key challenges remain. The areal-density of conventional SOT-MRAM is constrained by its 2T1R bitcell design and the area footprint of the write transistor due to the switching current requirements resulting from the limited charge-to-spin conversion efficiency of today's SOT materials. Adding to that, an external magnetic field is often required to enable deterministic switching in certain favorable device configurations, such as those with in-plane *x*-type or perpendicular *z*-type magnetic tunnel junctions (MTJs), whereas field-free switching is preferred [1].

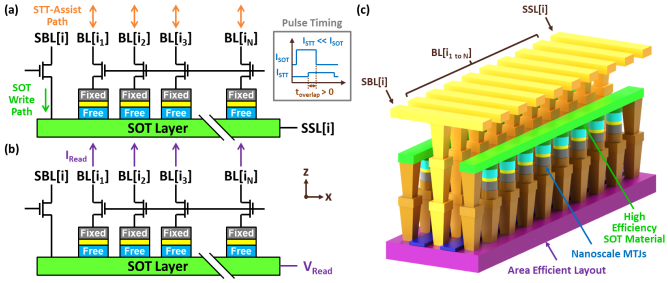

Fig. 1. Circuit schematic illustrating **(a)** writing and **(b)** reading in an *n*-bit SAS-MRAM device. **(c)** Conceptual sketch of *z*-type SAS-MRAM with SOT on top depicting 8 MTJs sharing the same SOT line and ultra-dense layout. SAS-MRAM can be constructed with both *x*- or *z*-type MTJs, where the MTJ access transistors can be as small as $6F^2$.

We seek to overcome these limitations by sharing the SOT line between multiple MTJs to amortize the area cost of the SOT drive transistor and leverage spin-transfer torque (STT) to enable deterministic, field-free switching. Sharing the SOT line between multiple MTJs has been explored in various contexts, and several techniques have been proposed to select individual MTJs on a shared SOT line, including voltage-based methods such as voltage-controlled magnetic anisotropy [2], [3], [4], [5], [6] or current-based techniques such as STT [7], [8]. Such approaches often require at least two SOT current pulses or other bit-serial writing techniques in order to write arbitrary data patterns to the device. In this work, we experimentally demonstrate a novel data writing scheme as shown in Fig. 1 [9] which enables bit-parallel, *simultaneous* switching of multiple MTJs with *different* polarity sharing the *same* SOT line, a first-of-its-kind experimental demonstration using a 4-MTJ STT-Assisted SOT (SAS) MRAM device as an example.

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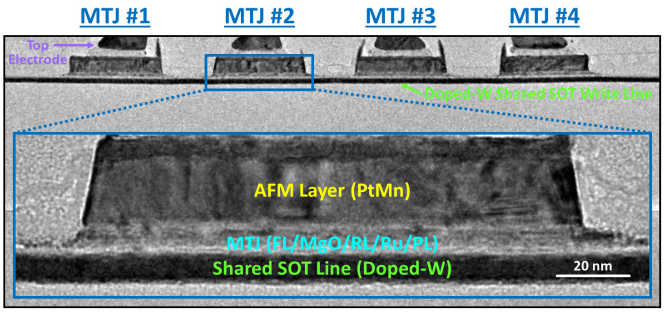

Fig. 2. Cross-section TEM of a SAS device with 4 MTJs sharing the same SOT line. The inset shows a close-up of a single MTJ.

II. SAS-MRAM: STT-Assisted SOT-MRAM

The interplay between SOT and STT has been leveraged to achieve various design goals ranging from 2-terminal SOT [10] to reduced switching current density in 3-terminal SOT devices [11], [12], [13], [14], [15], [16], [17]. SAS-MRAM (Fig. 1) offers a high-density cell design with n MTJs and (n + 1) transistors [9], where each MTJ current can be controlled independently and the SOT current is unidirectional and shared across all MTJs. SAS-MRAM can be routed using ~3 metal layers with an average footprint per MTJ as low as ~6F^2 per bit for bottom-pinned, z-type MTJs [18] when n is large (F is the minimum half pitch), as shown in Fig. 1(c). SAS-MRAM is also compatible with top-pinned MTJs (Fig. 2).

We introduce a novel, field-free writing technique which simultaneously switches all MTJs sharing the same SOT line and is compatible with both z-type and x-type MTJs (Fig. 1(a)) [9]: (a) first, a strong *unidirectional* SOT current is applied through the SOT line to orient each free layer midway between the parallel (P) and antiparallel (AP) states, which effectively neutralizes the anisotropy of all MTJs on the SOT line; (b) next, a small STT current is applied through each MTJ to break the symmetry between the P and AP states; (c) finally, the SOT current is released and each MTJ is allowed to relax to its programmed state. We refer to (a), (b) and (c) as the SOT-only, SOT+STT, and STT-only phases of writing, respectively. An example of this writing process showing ≤ 2 ns SAS switching and its associated micromagnetic switching trajectory is shown in Fig. 3(a), which is consistent with experimental demonstrations of ultrafast SOT-driven [13], [19] and STT-driven [20], [21], [22] switching in the ns and sub-ns regime.

This writing technique improves bit programmability and write bandwidth, and also helps overcome the write and read disturb modes found in the shared SOT line structure. More specifically, current that is injected into a MTJ to generate STT during the STT-only phase of writing must also flow through the SOT line due to Kirchoff's current law (KCL), which inadvertently generates a small SOT which could potentially disturb neighboring MTJs. In the limiting case, we must ensure that the sum of all currents injected into the MTJs is less than the SOT critical switching current ($I_{c,SOT}$) to avoid data corruption. We perform micromagnetic simulation with MuMax3 [23] to identify $I_{c,SOT}$ for device geometries similar to our fabricated devices (Fig. 3(b)). We show that the $I_{c,SOT}/I_{STT}$ ratio exceeds ~10 at technologically relevant MTJ widths, indicating robustness against this write disturb mode for $n \approx 4$ consistent with [24], which naturally increases with device scaling. At deeply scaled MTJ widths, $n \geq$ ~8 may be possible.

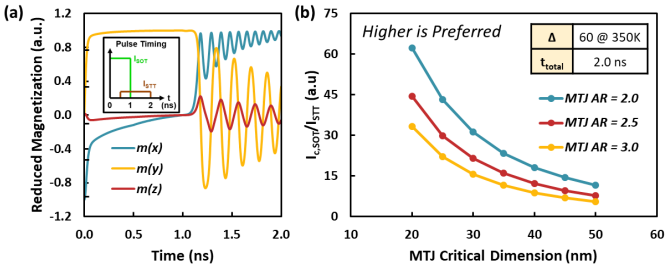

Fig. 3. **(a)** Average micromagnetic switching trajectory of a 150 × 50 nm^2 MTJ showing high speed (≤ 2 ns) SAS switching. J_{SOT} and J_{STT} are 184 and 2 MA/cm^2; θ_{SHA} is 0.6, which corresponds to that of doped-W. **(b)** Micromagnetic simulations of $I_{c,SOT}/I_{STT}$ at various MTJ critical dimensions. Device scaling naturally improves bit programmability.

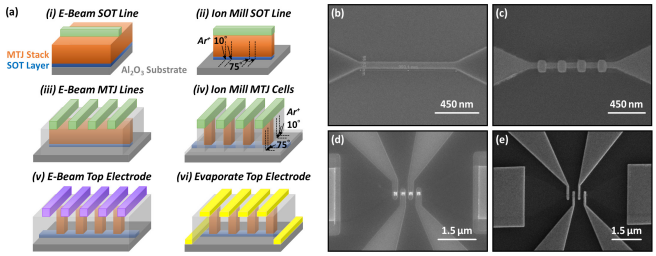

Fig. 4. **(a)** Schematic representation of the self-aligned fabrication process [26] used to fabricate SAS-MRAM devices. **(b, c, d, e)** SEM micrographs of SAS devices at various stages of fabrication, showing the SOT/MTJ patterning process in (b) and (c), and the top electrode patterning/deposition process in (d) and (e).

In addition, the $I_{c,SOT}/I_{STT}$ ratio can be further improved by adopting a z-type MTJ configuration which offers a smaller MTJ cross-sectional area (Fig. 1(c)). The $I_{c,SOT}/I_{STT}$ ratio may be used when evaluating write disturbance in the context of the SOT+STT phase of switching as well. Due to KCL, the current in the SOT line will deviate from its nominal value when STT current is injected into the device, where the relative deviation with respect to the SOT current may be expressed as [n / ($I_{c,SOT}/I_{STT}$)] in the worst case. At technologically relevant MTJ widths close to ~20 nm where the $I_{c,SOT}/I_{STT}$ ratio exceeds 40 (Fig. 3(b)), the deviation is less than 10% in a SAS-MRAM device with 4 MTJs; in other words, the SOT current may be driven 10% above $I_{c,SOT}$ to ensure that I_{SOT} exceeds $I_{c,SOT}$ for all MTJs. Incidentally, the read disturb figure-of-merit follows a similar formulation, where a higher $I_{c,SOT}/I_{Read}$ ratio is preferred. As $I_{Read} < I_{STT}$, the read disturb condition is naturally satisfied when the write disturb condition is satisfied.

III. Device Fabrication and Characterization

We begin fabrication with doped-W [19], [25] SOT-MTJ blanket films comprising of doped-W (7.2) / CoFeB (1.1 or 1.6) / MgO (1) / CoFeB (3.3) / Ru (1) / CoFeB (2.9) / PtMn (20) / Ta (4) / Ru (2) sputtered on a thermally oxidized Si substrate (thickness in nm), which is post-annealed under vacuum in a 1 T in-plane magnetic field at 360 °C for 20 minutes to pin the reference layer. Doped-W has been shown in the literature to achieve a high spin Hall angle of ~0.6, resistivity of ~160 µΩ·cm, and CMOS back end of line compatibility [19], [25]. We obtain a tunnel magnetoresistance ratio (TMR) of 140% and resistance area product of 12 Ω·µm^2 with the current in-plane tunneling test on MTJ blanket films.

We fabricate x-type SAS-MRAM using the self-aligned process [26] (Fig. 4(a)), targeting MTJ and SOT line widths of 30–60 nm, and SOT line lengths of 170–1100 nm depending on

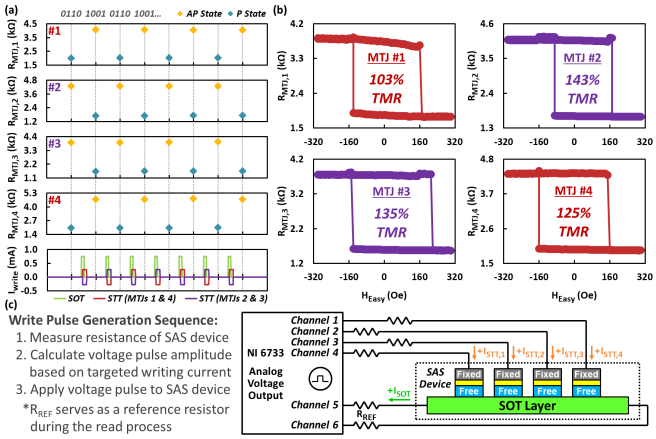

Fig. 5. **(a)** Field-free, current-induced SAS *simultaneous* switching of 4 MTJs on the *same* SOT line. The SOT current is *unidirectional*, which indicates that the polarity of the STT-assist current is breaking the symmetry between the P and AP states. I_{SOT} and I_{STT} are 0.74 and ±0.27/∓0.27 mA with a total pulse width of 4.2 μs (the fastest available in our measurement setup). Our micromagnetic simulations show that SAS switching can be ≤ 2 ns (Figs. 3(a,b)), consistent with sub-ns experimental demonstrations of both SOT-driven [13], [19] and STT-driven [20], [21] switching in the literature. **(b)** Corresponding field sweep loops showing excellent TMR. **(c)** Schematic representation of our measurement setup with the positive current direction indicated.

the number of MTJs. The self-aligned process improves device yields by relaxing the alignment tolerances in the vertical direction during fabrication. We first pattern and etch the SOT line geometry via e-beam lithography (EBL) and a two-step ion beam etching (IBE) process [27] immediately followed by passivation to protect the MTJ sidewall (Fig. 4(b)). Next, the MTJ geometry is defined using EBL and two-step IBE as before (Fig. 4(c)), where etch time control is used to terminate etching at the surface of the SOT line. Finally, the top electrode is patterned via lift-off (Fig. 4(d,e)). Fig. 2 shows a cross-section TEM view of a 4-MTJ SAS-MRAM device.

IV. Results and Discussion

Fig. 5(a) shows field-free *simultaneous* switching of 4 MTJs with *different* polarity sharing the *same* SOT line using our novel write method, a *first-of-its-kind* experimental demonstration. Importantly, the SOT current direction is the same for all write pulses, indicating that the STT-assist current is breaking the symmetry between the P and AP states. In addition, all 4 MTJs are switched in the same write operation with a single SOT current pulse as shown in Fig. 5(a), where an alternating binary data pattern of 4'b0110 and 4'b1001 is written into the device. The device does not switch when the SOT current is reduced, which shows that the switching is not driven by STT alone. The corresponding field sweep loops in Fig. 5(b) show excellent TMR exceeding 100% for all MTJs. The differences in TMR and coercivity may be attributed to geometric variations induced by the EBL exposure process.

We switch neighboring MTJs in opposite directions to show that adjacent free layers are not magnetically coupled to one another. To confirm that the stray field from neighboring MTJs does not play a role in multi-MTJ SAS switching, we perform SAS switching on a single-MTJ SAS device in Fig. 6 to exclude this possibility. Fig. 6 shows that excellent switching performance is maintained even in the case of a single-MTJ SAS device. While our experimental work focuses on *x*-type

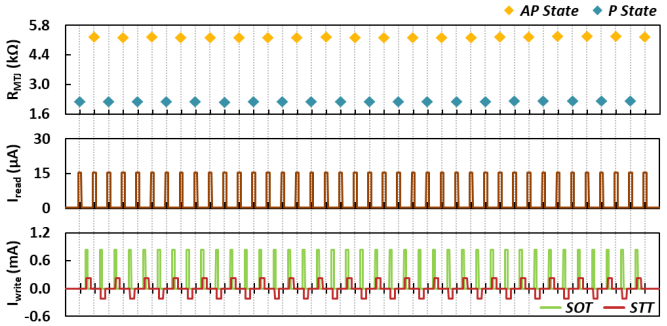

Fig. 6. Field-free, current-induced SAS switching was observed in an *x*-type, single-MTJ SAS device with dimensions of 102 × 57 nm^2. I_{SOT} and I_{STT} are 0.83 and ±0.22 mA, respectively, with a total pulse width of 4.2 μs (the fastest available in our measurement setup). The read current I_{read} is 15 μA, and the device has an excellent TMR of 141%.

MTJs, our SAS writing scheme is compatible with *z*-type MTJs as well, with both configurations offering various benefits. In particular, *z*-type MTJs enable higher $I_{c,SOT}/I_{STT}$ ratios and smaller MTJ access transistors, whereas *x*-type MTJs offer more flexibility in adjusting the free layer volume and the ability to leverage in-plane magneto-crystalline anisotropy [28] to enhance thermal stability. A more detailed treatment of the merits of *x*- and *z*- type SAS-MRAM may be found in [9, 29].

We note that the $I_{c,SOT}/I_{STT}$ ratio in our experimental demonstration (~3) is lower than expected (>10), owing to feature size enlargement of ~15 nm on each edge of the MTJ over the course of fabrication, resulting in a measured electrical area of ~60 × 110 nm^2, and limited STT efficiency in our MTJ stack. For this reason, we focus our current-induced switching experiments on the alternating data pattern shown in Fig. 5(a) to limit the current variation in the SOT line during switching. We expect to achieve better correlation between the designed and fabricated dimensions, and thus higher $I_{c,SOT}/I_{STT}$ ratios, by fine-tuning the etch process (e.g., etch angle optimization, etc.). Fig. 3(b) shows that the $I_{c,SOT}/I_{STT}$ ratio naturally improves with device scaling at MTJ critical dimensions well within the capabilities of MTJ manufacturing processes in industry. Our future work includes write error rate assessments and ultrafast switching measurements in the nanosecond regime on devices with optimized critical dimension and STT efficiency.

V. Conclusion

This paper demonstrates the feasibility of SAS-MRAM and verifies our novel writing method that enables simultaneous switching of multiple MTJs by overcoming the write and read disturb modes found in shared SOT line devices. We experimentally demonstrate *simultaneous* switching of 4 MTJs sharing the *same* SOT line. We believe that SAS-MRAM will pave a path towards a new class of high-density and high-speed on-chip nonvolatile memories, promising SRAM-like performance in last layer cache applications and more broadly in edge AI and energy-efficient computing.

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