Class AB Amplifier With Noise Reduction, Speed Boost, Gain Enhancement, and Ultra Low Power

Ali Far
ali.t.far@ieee.org

***Abstract* — This paper presents an approach that improves the cost-performance of an amplifier whose output noise (V_{ONOISE}) is lowered by narrow-banding filtering it, while slew rate (SR) and settling time (ts) are enhanced, when an imbalance is detected at the amplifier's input (V_{IN}) via a rail-to-rail (RR) minimum-current-selector (MCS). The contributions of the proposed circuit are (1) increasing the amplifier's gain without impeding its dynamic response by implementing a boot-strapped gain stage in a folded cascode transconductance amplifier, or FCTA (2) lowering V_{ONOISE} and enhancing the amplifier's dynamic response, with a smaller size suppression capacitor, or C_S, which lowers die cost and reduces the boost current consumption, or I_{DD} (3) enhancing the amplifier's SR and ts, lowering the dynamic I_{DD}, and improving the amplifier's power supply rejection, during the boost cycles, by utilizing a complementary MCS and a floating current summation, or FCS, circuits. Worst case simulations (WC), and Monte Carlo simulations (MC) simulations demonstrate the following: gain (Av) ~ 120dB, ts ~ 7µs to +/- 10mV with a rail-to-rail (RR) 1.5V step at V_{IN}, V_{ONOISE} at 1kHz ~ 9µV/√Hz, unity gain band-width (fu) ~5kHz, phase margin (PM) ~ 80 degrees, current consumption (I_{DD}) ~180nA, minimum operating V_{DD} ~1.2V, power supply rejection ratio (PSRR) ~ 94dB, common mode rejection ratio (CMRR) ~ 125dB. Approximate amplifier area is ~70 µm/side in 0.18µm digital CMOS.**

Keywords —**low noise, dynamic biasing, ultra low power, class AB, high speed, rail to rail, buffer amplifier, batteryless, slew rate boost, energy harvesting, smart dust, self powered, IoT.**

I. INTRODUCTION

All else equal, operating an amplifier in the subthreshold region at ultra low I_{DD} , generally increases V_{ONOISE}, slows the dynamic response (SR and τ_s), and reduces A_V [4-6]. The proposed embodiment of the (patent pending) method disclosed in [1-3], lowers the V_{ONOISE} of an amplifier by band passing it with an oversized suppression capacitor (C_s), while speeding up its τ_s by dynamically boosting the amplifier's bias current, when its V_{IN} is subjected to a large signal. Trading-off for higher operating V_{DD} requirement, the advantages of the proposed circuit over those proposed in [1-2] are: achieving nearly the same V_{ONOISE} and τ_s at ~1/3 I_{DD}, with ~ 50x more A_V, at ~1/60 of peak boost-on (transient) I_{DD}, with ~1/6th the die size (due in part to smaller C_s).

II. NOISE REDUCTION & DYNAMIC RESPONSE (BOTH SLEW RATE AND SETTLING TIME) BOOSTING

The proposed circuit is depicted in Fig. 1. For brevity, only the lower half of Fig. 1 is described here, given the symmetrical complementary nature of the upper and lower halves of the circuit.

TABLE I: SPECIFICATION COMPARISON

Typical Specs	[1][2]	This work	Figures
Area (µm²)	~180²	~70²	21
V_{ONOISE} @1kHz(µV/√Hz)	10	9	8
V_{DD} min (V) : with boost-on	0.9	1.2	16
V_{DD} min (V) : with boost-off	0.6	0.8	
I_{DD} (nA)	500	175	18,19
Peak Boost-on I_{DD} (µA)	520	8.5	2,3,4,5
Minimum R_L (Ω)	2K	10K	10, 15
Maximum C_L (pF)	1000	800	7
A_V (dB)	85	120	9,10
f_U (KHz)	20	5	9,10
φ_M (°)	75	85	9,10
|PSRR| (dB)	85/80	92	13,14
|CMRR| (dB)	125	94	11,12
V_{IN-pp} 1.5V pulse , $\tau_{S+/-}$ (µs)	5	6/7	2,3,4,5,6

This first section describes the RR buffer amplifier stage, containing a boot-strapped FCTA that increases the amplifier's gain. In the RR common source amplifier (CSA) section of the FCTA, the I_{Pa1} and I_{Pa2} differential currents (in concert with I_{Na10} and I_{Na12}) are steered onto N_{a11} and N_{a13}. Then, I_{Na11} and I_{Na13} are fed onto the FCTA high impedance high gain stage containing N_{a14} and N_{a16}, where VDS_{Na16} is boot-strapped through VGS_{Na17}. Qualitatively speaking, gain is enhanced here since VDS_{Na16} is held fairly constant (by VGS_{Na17}), irrespective of variations in the FCTA's gain stage output voltage (VD_{Na16}). Note that the boot-strapped topology, increases the minimum operating V_{DD} by an extra V_{GS}. Two floating constant current sources, containing N_{a15}, P_{a15} and N_{a18}, P_{a18}, provide the proper biasing for the boot-strapped gain stage (containing N_{a14}, N_{a16}, N_{a17}). The output FETs (N_{a24}, P_{a24}) and the boot-strapped gain stage quiescent currents (I_{qc}) are established by I_{Na23} and I_{Pa22}, which also bias $VGS_{Na19} + VGS_{Na20} + VGS_{Na21} = VGS_{Na18} + VGS_{Na17} + VGS_{Na24}$, in concert with their complementary symmetric counterparts, I_{Pa23} and I_{Na22} which bias $VGS_{Pa19} + VGS_{Pa20} + VGS_{Pa21} = VGS_{Pa18} + VGS_{Pa17} + VGS_{Pa24}$. A qualitative description of the transient signal flow of the boot-strapped gain stage is provided next.

During the transient rise of V_{OUT}, N_{a14} is fed the extra transient differential current that is steered through I_{Na11} and I_{Na13} causing $I_{Na14} \gg I_Q$ (for clarity, let's assume $I_Q = I_{qc}$, or equal quiescent currents in each of the FETs in the buffer amplifier stage, excluding N_{a24} and P_{a24}). Hence, during this transitory phase, I_{Na14}'s mirror $I_{Na16} \gg I_Q$ causes the decline in VDS_{Na16} and VGS_{Na17} (i.e., N_{a16} enters triode, and N_{a17} shuts off). As such, during the transient rising of V_{OUT} , the

978-1-5386-2311-4/18/$31.00 ©2018 IEEE

transient current through C_S is sourced by P_{a24} on one end and sunk on the other end (through N_{a16} in triode) and onto N_{a23} (scaled at 't.x') where $I_{Na23} = t \times I_Q$. The portion of I_{Na23} current, that was allocated to bias N_{a17} in steady state, is used here to speed up the transient response, given that N_{a17} is shut off. Note that during V_{OUT} transient rise, the capacitance at the output (N_{a24}'s gate) node is dominated by the roughly the Miller equivalent of Cg_{Na24}. When the N_{a15} and N_{a18} clamps kick in, the impedance at N_{a24}'s gate $\sim \propto f(1/g_m)$ of $N_{a14} - N_{a18}$ which are lowered by the extra available transient current ($g_m \propto 1/I$) with the rising V_{OUT} (and falling VG_{Na24}).

Conversely, during the transient falling of V_{OUT}, N_{a14} (and N_{a16}) are starved from current and are nearly off. Here, the floating current source (P_{a18}, N_{a18}) dominated by P_{a18} pulls up the gate of N_{a17} source follower. When $I_{Na14} = I_{Na16} \approx 0$, then I_{Na17} gets all of $\approx t \times I_Q$ that drives N_{a24} which speeds up the rise time for VG_{Na24}. Moreover, note N_{a17} and P_{a17} source followers decouple the impact of large sized output FET's Cg_{Na24} and Cg_{Pa24}, providing more independence for the amplifier's AC response to be dominated by C_S. Note also that increasing the gain and the output impedance of FCTA via the boot-strap stage, reduces the size of (oversized noise suppressing) C_S, which speeds up the SR ($C_S \propto 1/SR$). To accommodate RR span, P_{a3}, P_{a4} track P_{a1}, P_{a2} and turn off when V_{IN} is at or near V_{DD} . In order to avoid an I_{qc} imbalance in the FCTA boot-strap stage with V_{IN} near the rails, when P_{a7} is cut off from feeding N_{a10}, N_{a12} (through P_{a1}, P_{a2}), then P_{a6} is also cut off from adding current (through P_{a3}, P_{a4}) to N_{a8} which is mirrored onto N_{a10}, N_{a12}. Note also that in part, because the amplifier's speed is boosted rail-to-rail (RR), making its input stage's g_m constant RR does not justify the added cost and overhead.

This second section describes the RR MCS_P, which detects if V_{IN} is subjected to a large signal imbalance [5]. Un-equalized V_{IN} causes either of the drain currents $I_{Ns13} = I_{Ps10} = I_{Ps1}$ or $I_{Ns14} = I_{Ps6} = I_{Ps7} = I_{Ps11} = I_{Ps2}$ to be starved from current, which results in either of VGS_{Ps10} or VGS_{Ps11} to decline. Note that for MCS_P, the $VGS_{Ps11} + VGS_{Ps10} = VGS_{Ps9} + VGS_{Ps12}$. Thus, when $VGS_{Ps9} + VGS_{Ps12}$ declines enough, it causes P_{s9} to shut off. As such, I_{Ns19} pulls down on node S_p which initiates the 'boost-on' signal. The signal at S_p, via I_{Ns19} , drives the floating current summation (FCS_p) section, where $I_{Ns19} = I_{Pf1} = I_{Pf2}$. Similarly, on the complementary side of (FCS_n) when N_{s9} is off, then I_{Ps19} pulls up on S_n, which initiates a symmetric and complementary 'boost-on' signal as well (feeding $I_{Nf1} = I_{Nf2}$).

In steady state, when V_{IN} is equalized then $I_{Ps1} = I_{Ps2} = I_{Ps10} = I_{Ps11} = I_{Ps12} = I_{Ps8} = I_Q = I_{Ps9}$. By setting $I_{Ps9} > I_{Ns19}$, then a 'boost-off' signal is initiated at node $V_{Sp} \rightarrow V_{DD}$ that shuts off both P_{f1} and P_{f2}. Similarly, on the flip side (FCS_n) by setting $I_{Ns9} > I_{Ps19}$, it causes $V_{Sn} \rightarrow V_{SS}$, which initiates a symmetric 'boost-off' signal, and shuts off both N_{f1} and N_{f2}. Also, for FCS_N to span RR, P_{s3} and P_{s4} steer P_{s5} current away from P_{s1} and P_{s2} when V_{IN} gets near V_{DD}, causing $V_{Sp} \rightarrow V_{DD}$ and thus disabling FCS_N from falsely initiating a 'boost-on' signal. However, note that when V_{IN} is near V_{DD}, the complementary FCS_P containing P_{s3} and P_{s4} continues tracking large signal imbalances at V_{IN}, and remains equipped to initiate the 'boost on and off' signals.

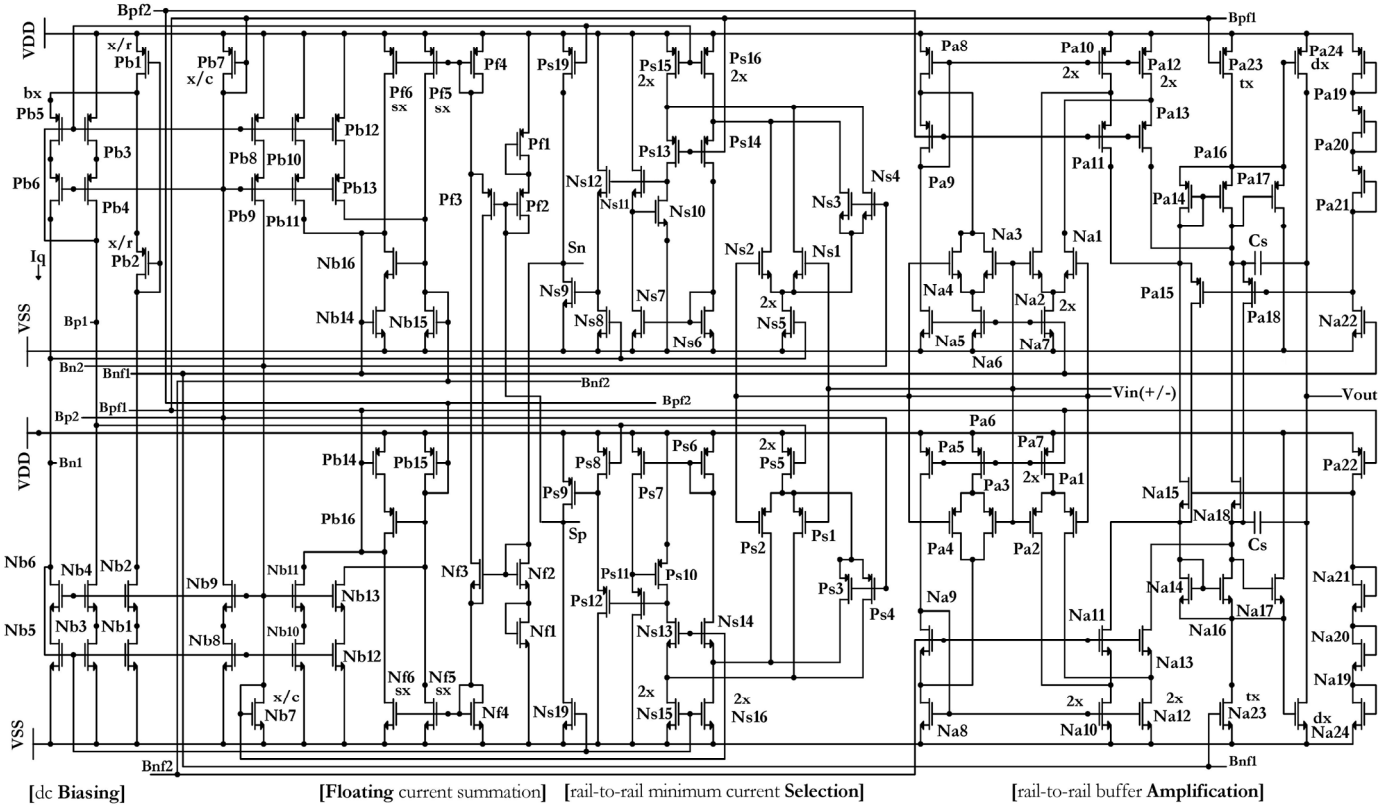

Figure 1. Buffer Amplifer Circuit Schematic Simplified (patents pending)

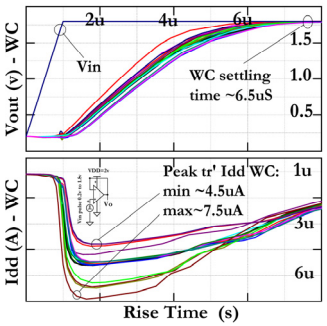

Fig. 2. Rising τ_s of V_{OUT} & I_{DD} (WC)

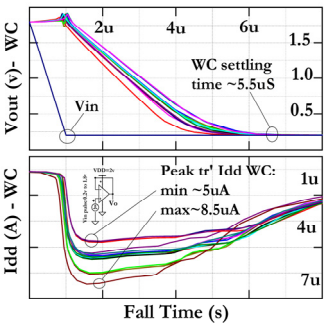

Fig. 3. Falling τ_s of V_{OUT} & I_{DD} (WC)

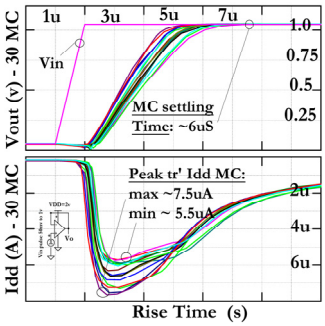

Fig. 4. Rising τ_s of V_{OUT} & I_{DD} (MC)

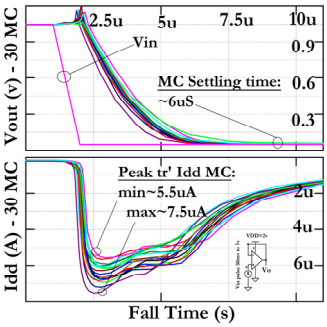

Fig. 5 Falling τ_s of V_{OUT} & I_{DD} (MC)

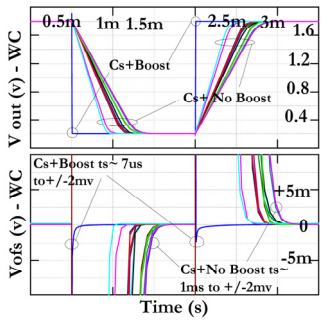

Fig. 6. τ_s of V_{OUT} with & without boost (WC)

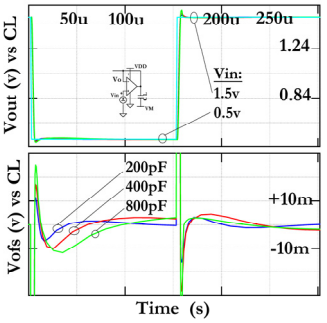

Fig. 7. τ_s vs. C_L

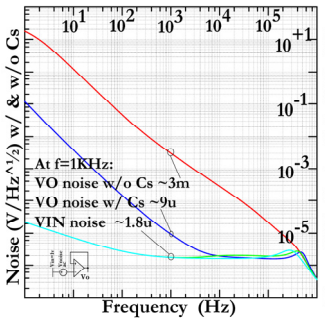

Fig. 8. V_{ONOISE} with & without C_S

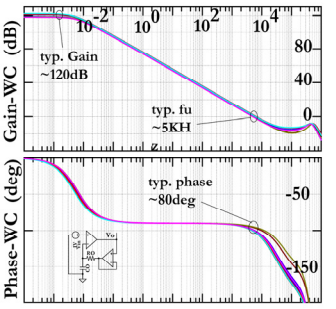

Fig. 9. AC Response (WC)

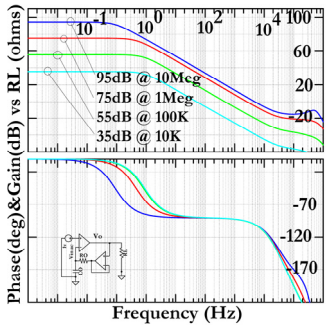

Fig. 10. AC response vs. R_L

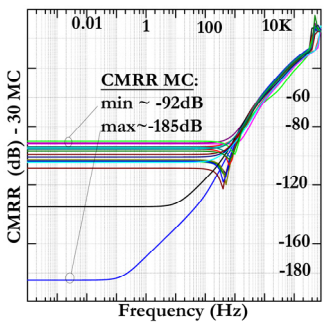

Fig. 11. CMRR (MC)

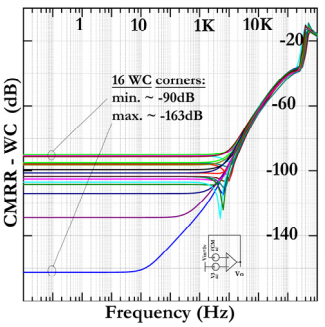

Fig. 12. CMRR (WC)

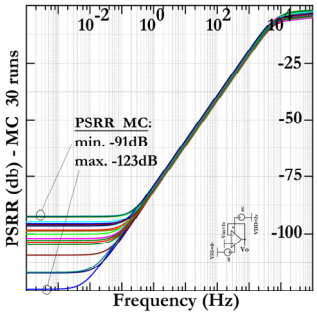

Fig. 13. PSRR V_{DD} (MC)

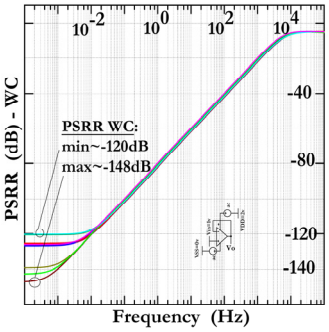

Fig. 14. PSRR V_{DD} (WC)

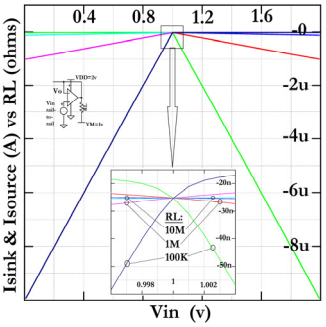

Fig. 15. I_{SINK}/I_{SOURCE} vs. R_L

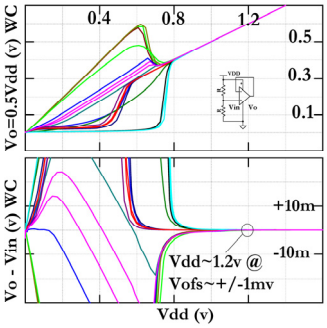

Fig. 16. V_{DD} vs. V_{OFFSET} (WC)

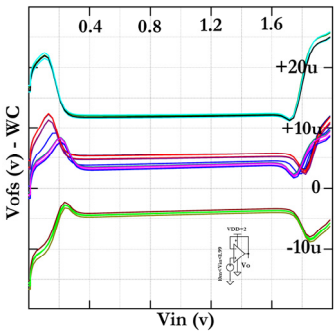

Fig. 17. V_{IN} vs. V_{OFFSET} (WC)

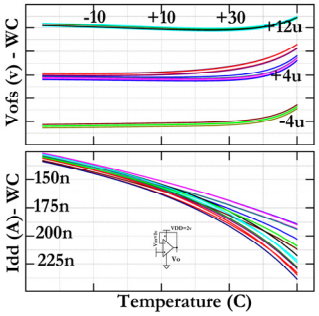

Fig. 18. V_{IN} vs. V_{OSF} vs. Temp (WC)

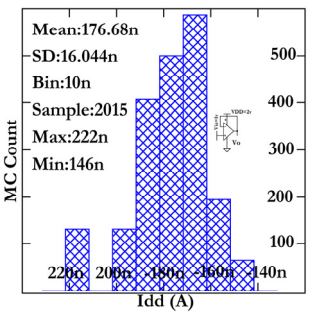

Fig. 19. I_{DD} (MC)

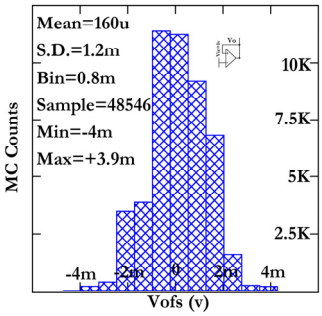

Fig. 20. V_{OFFSET} (MC)

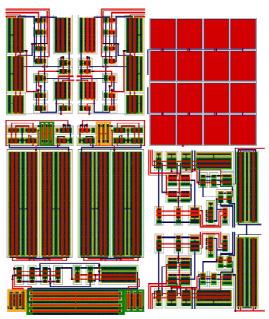

Fig. 21. Amplifier size ~(70µm)^2

This third section describes the FCS. In 'boost-on' phase, FCS generates a fast current spike for the main amplifier's bias network (N_{b14-16} and P_{b14-16}) to boost its SR. In 'boost-off phase when V_{IN} starts nearing equalization, then FCS provides a slow decaying current for the amplifier's bias network (starting at the peak of 'boost-on' dynamic current level), to enhance the amplifier's τ_s. With $VGS_{Pf1} + VGS_{Pf2} = VGS_{Pf3} + VGS_{Pf4}$, and $VGS_{Nf1} + VGS_{Nf2} = VGS_{Nf3} + VGS_{Nf4}$, then $I_{Pf3} + I_{Nf3} = I_{FCS}$ (floating current source) where I_{FCS} feeds each of P_{f4} and N_{f4} concurrently. Note that I_{FCS} is mirrored (onto N_{f5}, N_{f6}, and P_{f5}, P_{f6}) and scaled up by factor of 's' onto the central bias current network. In summary, when V_{IN} is imbalanced after it receives a large signal ('boost-on' phase), on the FCS_P side, N_{s19} turns on P_{f1}, P_{f2} which turn P_{f3}, P_{f4}, N_{f4} on while (symmetrically and) concurrently at the FCS_n side, P_{s19} turns on N_{f1}, N_{f2} which turn on N_{f3}, N_{f4}, P_{f4}. As such, FCS_n and FCS_p, collectively and symmetrically, feed the amplifier's bias network with a fast current spike to speed up SR. Conversely, when the 'boost-off' signal is initiated, P_{f4}, N_{f4} are cut off from current. As such, a decaying current (that continues feeding the amplifier's bias network) enhances τ_s, which is initiated by cutting off P_{f4}, N_{f4} where the current decay time constant is set by the impedance ($g_m \propto 1/I$) and the equivalent $C_{eqiv} \propto Cg_{Pf5} + Cg_{Pf6}$ and $Cg_{Nf5} + Cg_{Nf6}$.

III. Monte Carlo & Worst Case Simulations Summary

MOSIS equivalent models for BSIM3v3.1 for 0.18µm CMOS are applied for WC and MC simulations. Table I provides a specification comparison summary. Figure 2 is WC $\tau_{s+} \approx 6.5$ µS to ±10mV with V_{in} ↑1.6V step, transient $5\mu A > I_{DD_{t+}} > 7.5\mu A$. Figure 3 is WC $\tau_{s-} \approx 5.5$ µS to ±10mV with a V_{in} ↓1.6V step, transient $5\mu A > I_{DD_{t-}} > 8.5\mu A$. Figure 4 is MC $\tau_{s+} \approx 6$ µS to ±10mV with a V_{in} ↑0.95V step, transient $5.5\mu A > I_{DD_{t+}} > 7.5\mu A$. Figure 5 is MC $\tau_{s-} \approx 6$ µS to ±10mV with a V_{in} ↓0.95V step, transient $5.5\mu A > I_{dd_{t-}} > 7.5\mu A$. Figure 6 is WC τ_s (V_{in} ↓↑1.6V pulse) with the boost circuit on and without it. This indicates WC $\tau_s < 7\mu S$ to ±2mV with the boost enabled, or more that 60X improvement in τ_s, compared to WC $\tau_s < 1mS$ to ±2mV with the boost disabled. Figure 7 is τ_{s+} (< 25 µS ±10mV to with V_{in} ↓1V step) vs. C_L (200pF, 400pF, and 800pF). Note here that τ_{s-} is faster (V_{IN} ↑1V step), but that is due to the tail-end of 'boost-off' current still decaying in the amplifier's bias network. Figure 8 is the noise response, indicating $V_{ONOISE} \approx 9\mu V/\sqrt{Hz}$ at 1kHz with the noise reduction (band-pass) capacitor C_S vs. $V_{ONOISE} \approx 3mV/\sqrt{Hz}$ at 1kHz without C_S, which indicates more that 300X improvement in V_{ONOISE}. Figure 9 is WC AC response with $A_V \approx 120dB$, $f_u \approx 5kH$, $\varphi \approx 80°$. Figure 10 is typical AC response (gain at ~ 95dB, ~ 75dB, ~ 55dB, 35dB) vs. R_L (10MΩ, 1MΩ, 100KΩ , and 10kΩ, respectively). Figure 11 is MC -185dB < CMRR < -92dB. Figure 12 is WC -163dB < CMRR < - 90dB for V_{DD}. Figure 13 is MC -123dB < PSRR < -91dB for V_{DD}. Figure 14 is WC -148dB < PSRR < -120dB for V_{DD}. Figure 15 is the output $I_{sink\,\&\,source}$ vs. R_L: 10MΩ, 1MΩ, and 100kΩ vs. spanning $10mV > V_{IN} > 1.99V$. Fig. 16 is WC min. $V_{DD} > 1.2V$ by reading V_{OFFSET} (bias amplifier for I_{DD} =8µA to emulate transient current during 'boost-on') and ramping up V_{DD} with $V_{IN} = 1/2V_{DD}$. Note that in boost-off phase, WC I_{DD} min. is ~ 0.8V . Figure 17 is WC $-10\mu V < V_{OFFSET} < +30\mu V$ spanning $10mV < V_{IN} < +1.99V$. Figure 18 is WC V_{OFFSET} and I_{DD} vs. temperature (T) from −25℃ to +50℃. Figure 19 and 20 are MC I_{dd} (avg. 177nA), and MC V_{OFFSET} (avg. 160µV). Figure 21 is rough layout size ~$(70\mu m)^2$

Acknowledgment

My gratitude to Professor Shahriar Mirabbasi at University of British Columbia for his review and comments.

IV. Conclusion

Output noise of a rail-to-rail high-gain amplifier is lowered by band-pass filtering it with an oversized C_S, and when V_{IN} is imbalanced, the amplifier's speed is boosted. Accordingly, a dynamic current is injected into its bias during 'boost-on' to accelerate SR, as well as τ_s during 'boost-off' by slowly decaying its bias current back to steady state levels. FCTA gain is enhanced by a boot-strapped topology that leaves the dynamic response generally unimpeded. A MCS initiates the boost on-off signals, via feeding a FCS circuit that supplies the amplifier's dynamic operating current, symmetrically and RR.

References

[1] A. T. Far, "Ultra low power high-performance amplifier", U.S. patent pending Ser. No. 15/451,334

[2] A. Far," Low Noise Rail-To-Rail Amplifier Runs Fast at Ultra Low Currents And Targets Energy Harvesting," *2017 IEEE International Autumn Meeting on Power, Electronics and Computing (ROPEC),* Ixtapa, 2017,

[3] A. T. Far," Sub-1 Volt Class AB Amplifier With Low Noise, Ultra Low Power, High-Speed, Using Winner-Take-All," *2018 IEEE 9th Latin American Symposium on Circuits & Systems (LASCAS)*, Puerto Vallarta, 2018,

[4] Seevinck, E. *et al.*, "Universal Adaptive Biasing Principle for Micropower Amplifiers," in Solid-State Circuits Conference, 1984. ESSCIRC '84. Tenth European , vol., no., pp.59-62

[5] Y. Tsuruya *et al.*, "A nano-watt power CMOS amplifier with adaptive biasing for power-aware analog LSIs," ESSCIRC (ESSCIRC), 2012 Proceedings of the, Bordeaux, 2012, pp. 69-72.

[6] Allen P.E. , "Analog integrated circuit design", 1st. Ed., John Wiley & Sons, New York, 1997.

Ali Far received his B.S. in EECS from UC Berkeley; and MSEE, MBA, Juris Doctor in Law, and M.A. in Psychology, all from Santa Clara University. He is working on his M.A. in Philosophy at SFSU. He has more than 20 years of analog IC design experience in Silicon valley where he worked at Plantronics, PMI (ADI), MPS (MaxLinear), MVT (Creative Labs), and TelCom (Microchip) where he was Vice President of Design. He has 10 years of technology investment banking experience in Wall Street, where he worked at Prudential Securities, Galleon, and Spherix where he served as Technology Analyst. Ali has published a dozen papers in IEEE, has 14 patents and some pending in the area of analog ICs, and is currently researching ultra low power analog for energy harvesting.