Sub-1 Volt Class AB Amplifier With Low Noise, Ultra Low Power, High-Speed, Using Winner-Take-All

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***Abstract* — The proposed circuit utilizes a method to lower the output noise (V_{ONOISE}) of an amplifier by band-pass filtering it, while the amplifier's speed is increased by dynamically boosting its operating current when the amplifier's inputs (V_{IN}) receive a large transient signal. This amplifier uses a winner-take-all (WTA) circuit that detects un-equilibrium at V_{IN}, upon which the amplifier's bias current and its dynamic response are boosted. The WTA has a symmetric structure and operates in current mode that enhances the amplifier's dynamic response during boost on and off conditions, and facilitates operations at low power supply voltage (V_{DD}). The boost signals that WTA initiates, feed a summing and floating current source (FCS) that also have a complementary and symmetric structure, which accommodates rail-to-rail (RR) dynamic biasing and improves V_{DD} transient and noise rejection. Monte Carlo (MC) and worst case (WC) simulations are performed, indicating the following specifications as attainable: large-signal settling time (ts) ~ 1µs, current consumption (I_{DD}) ~ 85nA, V_{DD} under 1 volt (V), V_{ONOISE} at 1KHz ~ 75µV/√Hz, gain (Av) ~ 98dB, unity gain frequency (fu) ~ 70kHz, phase margin (PM) ~ 80 degrees, PSRR ~ 115dB, CMRR ~ 145dB. Amplifier rough area ~ 45µm/side in 0.18µm CMOS.**

Keywords — **sub 1 volt, subthreshold, batteryless, energy harvesting, smart dust, biometrics, wireless sensor array, self powered, winner-take-all, maximum-current-select, low noise, rail-to-rail, speed boost, dynamic biasing, ultra low power, high speed, class AB amplifier, low power supply, ultra low current.**

I. INTRODUCTION

In order to lower the noise at the output (V_{OUT}) of an ultra-low-power CMOS amplifier, the disclosure in [1] proposed a method to band-pass the amplifier (with a large capacitor , C_s) at its high-impedance node in order to filter out the output noise (V_{ONOISE}). Then, the operating current of this slowed (band-passed) amplifier is dynamically boosted such that its slew-rate (SR) and settling time (τ_s) are re-invigorated, when the V_{IN} is subjected to an un-equilibrium. To this end, a subthreshold input-output rail-to-rail (RR) standard folded cascode amplifier (FCTA) is proposed here utilizing a WTA (or a 'maximum'-current-selector) that detects when V_{IN} is un-equalized, and initiates boost on-off signals [1-3]. The proposed WTA runs in current mode and is triggered on 'maximum' current selection, which sharpens the boost on-off response time, around the cycles when V_{IN} is imbalanced. Boost on-off signals feed the boost currents onto the amplifier's summing and floating current source (FCS) stages, having a complementary structure like WTA, which accommodates RR dynamic biasing with improved power supply transient and noise rejection [4-6]. The amplifier's specifications are summarized in Table I.

TABLE I: SPECIFICATION COMPARISON

Typical Specs	[2]	This work	Figure
Area (µm²)	~180²	~45²	21
I_{DD} (nA)	500	86	2,3,6
Large signal $\tau_{S+/-}$ (µs)	5	1	12 to 20
Minimum V_{DD} (V) at boost on	0.9	1	6
V_{ONOISE} 1kHz (µV/√Hz)	10	75	7
|PSRR| (dB)	85/80	115	10
|CMRR| (dB)	125	145	11
Transient Peak I_{DD} (µA)	520	25	14 to 20
Min. R_L (kΩ)	2	100	9
Max. C_L (pF)	1000	100	13
A_V (dB)	85	98	8,9
f_U (kHz)	20	70	8,9
φ_M (°)	75	80	8,9

II. 'WINNER-TAKE-ALL' AND 'SUMMATION & FLOATING CURRENT SOURCE' CIRCUITS

Figure 1. is the schematic of the proposed circuit. The lower half RR 'winner-take-all' (WTA_N), or maximum-current-select ($MXCS_N$), in concert with the 'sum & float current source' (FCS_N) circuits are described, setting aside non-idealities (e.g., mismatch). The discussions on WTA_N and FCN_N also apply to their symmetric counterparts, WTA_P and FCN_P.

During steady-state phase (or 'boost-off' phase), V_{IN} is in balance. Here, the quiescent currents (I_Q) in P_{w1} and P_{w2} are equal, which feed N_{w4} and N_{w5} (i.e., inputs of WTA_N). Accordingly, $Vgs_{Nw7} = Vgs_{Nw8}$, and $I_{Nw7} = I_{Nw8}$. As such, $I_{Nw7} + I_{Nw8} = I_Q$ is fed onto P_{w9}. But here, in the steady state phase, P_{w9} is kept off by I_{Pw15} pulling up VGS_{Pw9} and reducing it. Thus, the 'boost-off' current is near zero with $I_{Pw17} = n \times I_{Pw9} \approx 0$. Also note that in steady state, with $I_{Pw9} = I_{Pw10} = 0$, then $I_{Pw16} = I_Q$ feeds N_{w6} that is mirrored onto $N_{w4,5}$ which receive the equalized I_{Pw1} and I_{Pw2}. Thus in 'boost-off' phase, only $I_{Pw18} = I_Q$ together with (the complementary side) $I_{Nw18} = I_Q$ supply current to the FCS_N. The I_{Pw18} feeds N_{f1} and N_{f2} with I_Q that biases N_{f3} while I_{Nw18} supplies I_Q to P_{f1} and P_{f2} that biases P_{f3}. Sum of the floating currents, $I_{Nf3} + I_{Pf3} = 2I_Q$, bias $N_{f4,5}$ and $P_{f4,5}$ that set steady-state current in FCTA's bias network, N_{f4-8} and P_{f4-8}.

When V_{in} is imbalanced, after receiving a large transient signal, then the WTA and FCS circuits process the 'boost-on' signal, which boosts FCTA's current and here is how. Let's take the WTA_N transient case when $I_{Pw1} \gg I_{Pw2}$ (e.g., $I_{Pw1} \approx 2I_Q$ and $I_{Pw2} \approx 0$) which lifts Vs_{Nw13} (shutting it off), causing I_{Pw11} to lift Vgs_{Nw7} and raise I_{Nw7}. Conversely, when $I_{Pw1} \gg I_{Pw2}$ in transient, then I_{Nw5} (through N_{w14}) lowers

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Vgs_{Nw8}, which reduces I_{Nw8}. The transient sum of $I_{Nw7} + I_{Nw8}$ is dominated here by N_{w7} that can spike to $\leq 3I_Q$, which provides P_{w9} with the scaled up (×n) boost current in P_{w17}. In the 'boost-on' transient phase: $I_{Pw15} + I_{Pw9} = I_{Nw7} + I_{Nw8} \leq 3I_Q$ (where $I_{Nw8} \approx 0$); $I_{Pw10} + I_{Pw16} = I_{Nw6} \leq 3I_Q$; and $I_{Pw1} + I_{Pw11,13} = I_{Nw4} \leq 3I_Q$. Thus, in 'boost-on' phase, with $I_{Pw1} \gg I_{Pw2}$ and considering $I_{Nw5} \approx I_{Nw6} \leq 3I_Q (> I_{Pw12,14} = I_Q)$, then N_{w14} pulls down on the Vg_{Nw8} and keeps N_{w8} off. As stated earlier, while in 'boost-on' phase, $I_{Pw11} = I_Q$ holds-up the voltage lift on Vg_{Nw7}. While 'boost-on' lasts, voltage lift on Vg_{Nw7} is sustained, considering $I_{Nw4} \leq 3I_Q$ and $I_{Pw1} \approx 2I_Q$ which causes $I_{Nw4} - I_{Pw1} = I_{Nw13} \leq I_Q$, when $I_{Pw11} = I_Q$. A similar current 'boost-on' mechanism would be in play for the complementary side WTA_P, which supplies the boosted current through FCS into the FCTA bias network. For the FCS_N half of the circuit, a transient 'boost-on' current spike $\leq [I_{Pw17} + I_{Pw18}] \sim [3(n \times I_Q) + I_Q]$ is channeled onto N_{f1} and N_{f2}. Similarly, on the FCS_p side, a complementary and symmetric transient 'boost-on' current spike $\leq [I_{Nw17} + I_{Nw18}] \sim [3(n \times I_Q) + I_Q]$ is channeled onto P_{f1} and P_{f2}. Therefore, a sum of currents $\leq [2I_Q\ (3n + 1)]$ would bias N_{f3} and P_{f3}, which establishes the 'boost-on' transient current for the FCTA bias network (N_{f4-8}, and P_{f4-8}). This boosted current (that is symmetric) feeds the FCTA's common source amplifier (CSA) stage (P_{a1-3}, N_{a1-3}), the common gate amplifier (CGA), the current mirror stage (N_{a4-7}, P_{a4-7}), as well as the FCTA's floating current source stage (N_{a8-9}, P_{a8-9}). The proposed embodiment, speeds up the dynamic response of band-passed amplifier (with the large C_S), and thus equipping the FCTA to low-pass the noise in steady-state, and have a fast dynamic response in the transient phases [1-2].

In summary, some of the merits of the proposed circuit are: First, the WTA operates as a 'maximum-current-selector' (MXCS) running in current mode, which helps speed. Second, and qualitatively speaking, the alternative approaches disclosed in [1-3] that utilizes minimum-current-circuit, triggers the 'boost on-off' signals upon appearance or disappearance of a 'minimum' current (i.e., smaller). The proposed circuit triggers the 'boost on-off' signal upon appearance or disappearance of a 'maximum' current (i.e., larger). As such, the proposed circuit, detects a V_{in} imbalance with larger currents, which is in part responsible for WTA enhanced response time compared to [1-2]. Third, the WTA 'boost-on' signal can be initiated rapidly, which boost the FCTA's slew rate faster, in compliance with the method proposed in [2-3]. This is because the spiked currents in N_{w7} or N_{w8} can pull down on diode connected P_{w9} faster due to the $Gate_{Pw9}$'s impedance declining while the transient current is rising ($1/g_m \propto 1/I$). Conversely, when the 'boost-off' phase is initiated, the current decay rate is slower than the current spike rate, which would enhance the FCAT's τ_S, again in accordance with the method proposed in [1-2]. This is because, upon arrival of steady state, bulk of the current $N_{w7,8}$ (in the case of WTA_N, for example) is supplied by P_{w15}, which diminishes the current in the diode connected P_{w9}, thus increasing its impedance $1/gm_{Pw9}$ as I_{Pw9} decays towards zero. Considering the scaled up (and the Miller equivalent) capacitance at the gate terminal of P_{w17} and the rising $1/gm_{Pw9}$ impedance,

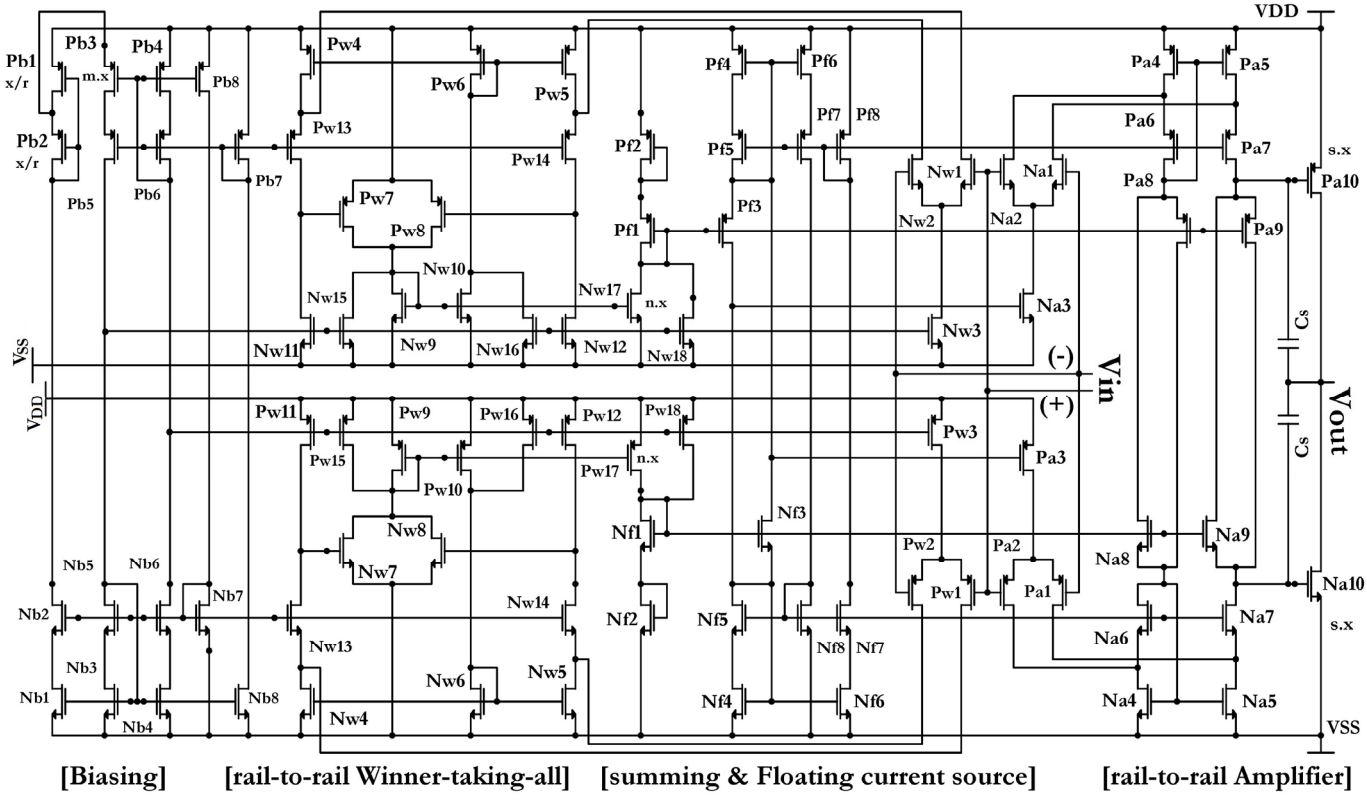

Figure 1. Amplifer Circuit schematic (patents pending[1])

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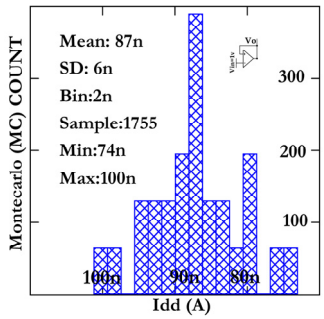

Fig. 2. Monte Carlo (MC) I_{DD}

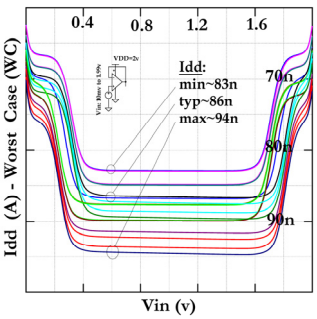

Fig. 3.Worst Case (WC) I_{DD} vs. V_{IN}

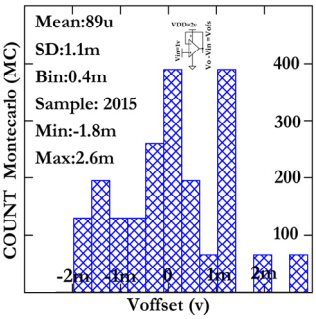

Fig. 4. MC input V_{OFS}

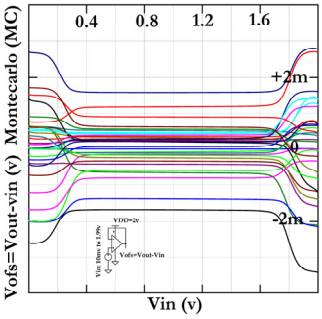

Fig. 5 MC input V_{OFS} vs. V_{IN}

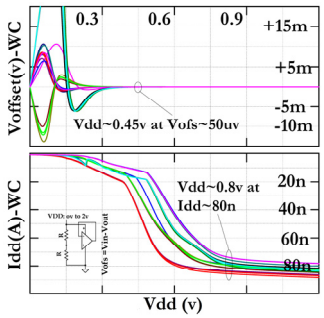

Fig. 6. WC min. V_{DD} vs. I_{DD} vs. V_{OFS}

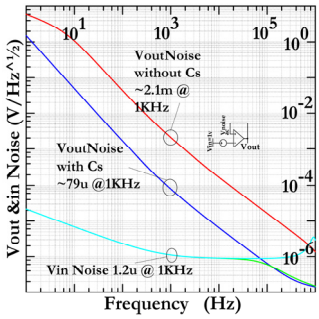

Fig. 7. V_{ONOISE} vs. C_S vs. No C_S

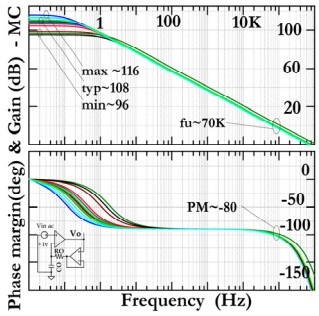

Fig. 8. MC Gain & Phase response

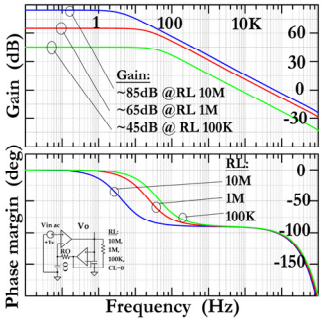

Fig. 9. Gain & Phase vs. R_L

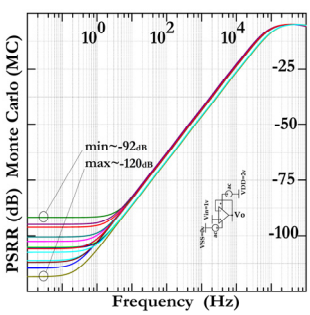

Fig. 10. MC PSRR response

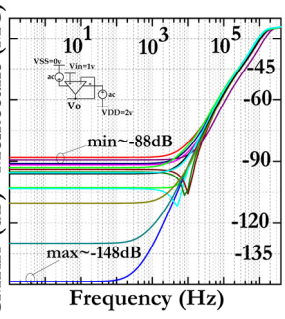

Fig. 11. MC CMRR response

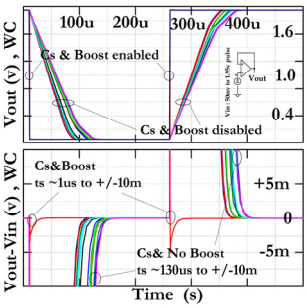

Fig. 12. WC speed with & without Boost

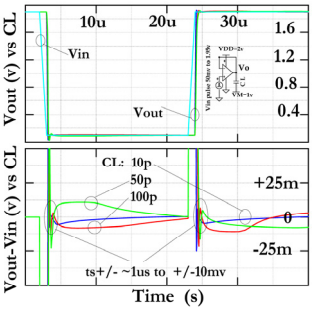

Fig. 13. Settling time (τ_s) vs. C_L

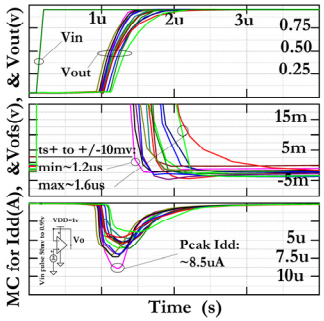

Fig. 14. MC τ_{s+} vs. V_{OFS} vs. I_{DD}@1v

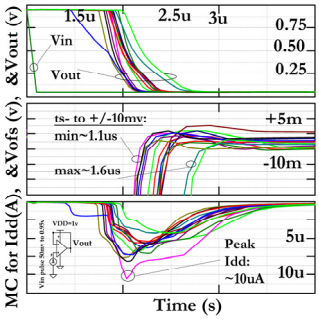

Fig. 15. MC τ_{s-} vs. V_{OFS} vs. I_{DD}@1v

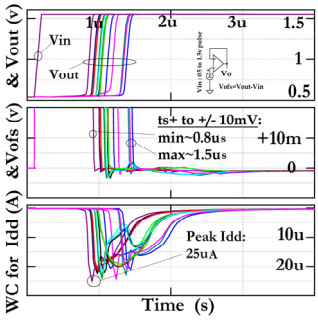

Fig. 16. WC τ_{s+} vs. V_{OFS} vs. I_{DD}@2v

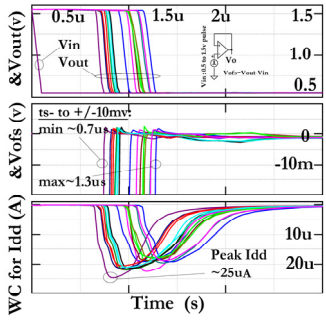

Fig. 17. WC τ_{s-} vs. V_{OFS} vs. I_{DD}@2v

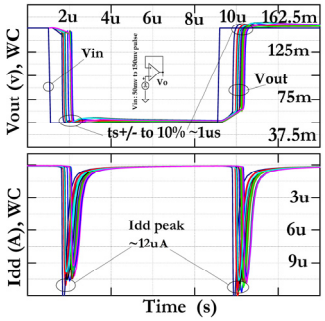

Fig. 18. WC $\tau_{s+/-}$ vs. I_{DD} @ $V_{in} \geq V_{SS}$

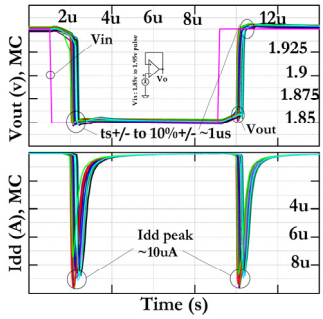

Fig. 19. MC $\tau_{s+/-}$ vs. I_{DD} @ $V_{IN} \leq V_{DD}$

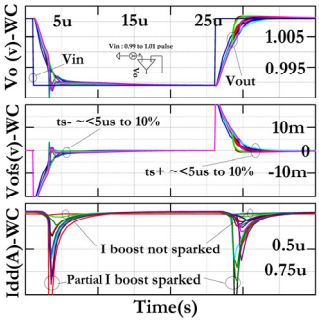

Fig. 20.MC τ_{s+}vs. V_{OFS} vs. I_{DD}@$V_{IN,small}$

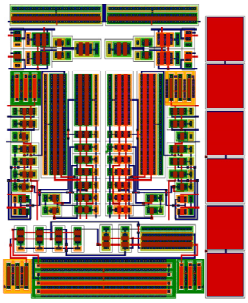

Fig. 21. cell size ~(45µm)²

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a slower decay current towards zero is initiated at the "boost-off' phase (providing the FCTA with more current above its quiescent $2I_Q$ while V_{out} is settling). Thus, τ_S is sped up. Fourth, FCS plus WTA operate rail-to-rail (RR). For example, when V_{IN} nears V_{DD} and P_{w1-3} shuts off, then $P_{w9,17}$ remain off, which inhibits WTA_N from initiating a false 'boost-on' current. Here, concurrently WTA_P continues monitoring V_{in} for imbalances even near V_{DD} and furnishing N_{w17} with the 'boost-on' current, through P_{f3} and onto N_{f4-5} and its complementary counter-part P_{f4-5}. Fifth, the proposed WTA can work with minimum V_{DD} of $V_{GS} + 2V_{DSon}$, thus not restricting FCTA's minimum V_{DD}. Sixth, there is flexibility to speed up SR and τ_S by raising WTA's I_Q through for example P_{w1-3} and P_{w11-12}. Seventh, the transient peak current is a multiple of $I_Q \propto f(\mu_P, V_T)$ where μ_P is PMOS mobility, and V_T is thermal voltage. As such, boost-on peak (band) current can be contained by design.

III. Simulations Results

WC and MC are performed utilizing equivalent device models in BSIM3v3.1 for MOSIS 0.18µm CMOS. Table I is specifications comparisons. Figure 2 is I_{DD} MC histogram $74\text{nA} < I_{DD} < 100\text{nA}$. Figure 3 is WC for I_{DD} vs. V_{IN} showing $83\text{nA} < I_{DD} < 94\text{nA}$, except for near the rails when one input pair (to FCTA and WTA) shuts off. Figure 4 is input offset voltage (V_{OFS}) MC histogram indicating $-1.8\text{mV} < V_{OFS} < +2.6\text{mV}$. Figure 5 is MC for input V_{OFS} vs. V_{IN}, where PMOS-NMOS mismatches, highlighted near the rails, would manifest as distortion. Figure 6 is WC for minimum V_{DD} ~ 0.8V via monitoring both input V_{OFS} and I_{DD}. Figure 7 demonstrates a 27 time improvement in output noise, Vo_{noise}, at $\sim 79\mu V/\sqrt{Hz}$ at 1KHz with the band-pass capacitor (C_S) versus $\sim 2.1\text{mV}/\sqrt{Hz}$ without C_S. Figure 8 is MC AC response denoting $96\text{dB} < \text{Gain} < 116\text{dB}$ with typical DC gain $A_V \approx 108\text{dB}$, $f_u \approx 70\text{kH}$, and $\varphi \approx 80°$. Figure 9 is AC response vs. R_L indicating A_V/R_L of 85dB/10MΩ, 65dB/1MΩ, and 45dB/0.1MΩ. Figure 10 is MC for PSRR showing $-92\text{dB} < \text{PSRR} < -120\text{dB}$. Figure 11 is MC for CMRR showing $-88\text{dB} < \text{CMRR} < -148\text{dB}$. Figure 12 is the WC τ_s to ±10mV, or $\tau_{s\mp}$, which depicts a 100X to 130X speed enhancement. Here, $100\mu\text{s} < \tau_{s\mp} < 130\mu\text{s}$ with the boost circuit disabled, and $\tau_{s\mp} \sim 1\mu\text{S}$ with boost circuit enabled. Figure 13 is $\tau_{s\mp} \sim 1\mu\text{s}$ vs. C_L $10\text{pF} < C_L < 100pF$ with a 50mV to 1.95V step at V_{IN-pp}. Figure 14 and 15 are MC, for $V_{DD} = 1\text{V}$, applying a 0.95V step at V_{IN-pp}, which indicates $1.2\mu\text{s} < \tau_{s\mp} < 1.6\mu s$, and dynamic (transient) $I_{DD-peak} < 10\mu A$, which vanishes in ~2µs. Figure 16 and 17 are WC, for $V_{DD} = 2\text{V}$, applying a 1V step at V_{IN-pp}, which shows $0.7\mu\text{s} < \tau_{s\mp} < 1.5\mu s$, and dynamic (transient) $I_{DD-peak} < 25\mu\text{A}$, which vanishes also in ~2µs. Figure 18 is WC $\tau_{s\mp} \sim 1\mu\text{s}$ after applying a 50mv→150mV step at V_{IN-pp}, indicating $I_{DD-peak} < 12\mu\text{A}$ dynamic boosting even near V_{SS}. Figure 19 is MC $\tau_{s\mp} \sim 1\mu\text{s}$ after applying a 1.85V→1.95V step at V_{IN-pp}, indicating dynamic $I_{DD-peak} < 10\mu A$ boosting also near V_{DD}. The transition zone (gray-zone) between application of a small signal applied at V_{IN} (i.e., no boost current spark or only a partial spark thus slower τ_s) vs. large signal applied at V_{IN}, which is captured in Figure 20. Here is WC $\tau_{s\mp} < 5\mu s$ after applying a 0.99V→1.01V step at V_{IN-pp}, with dynamic current $0 < I_{DD-peak} < 0.8\mu\text{A}$. Figure 21 is an approximate layout and the rough cell size is $\sim(45\mu\text{m})^2$.

IV. Conclusion

Prior art disclosed a method to dynamically increase the bias current and speed of a ultra low current amplifier, whose output noise is reduced by band-passing it (e.g., using a large C_S at the FCTA gain node). This embodiment improves the amplifier's performance by utilizing a rail-to-rail, low V_{DD}, WTA (or maximum-current-selector), that runs fast in current mode, to detect a V_{IN} imbalance upon which the amplifier's bias current and speed are boosted dynamically. The complementary and symmetric structure of the WTA and FCS facilitates rail-to-rail dynamic biasing and improves V_{DD} noise and jitter rejections.

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