Enhanced Gain, Low Voltage, Rail-To-Rail Buffer Amplifier Suitable For Energy Harvesting

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Abstract — **A CMOS subthreshold rail-to-rail input-output buffer amplifier suitable for energy harvesting applications is presented, having high gain (A_V) of ~ 130dB, consuming ultra low currents (I_{DD}) of ~ 150nA, and operating with low power supply voltage (V_{DD}) > ~ 0.8v. Contributions of this work are the synthesis of the following attributes: First, using a single transistor, the amplifier input stage's tail current is steered between the two PMOSFET input pairs, while one of the PMOSFET pairs is level shifted by a pair of NMOSFET source followers, which keeps the amplifier's input stage transconductance (gm) roughly constant while the inputs span rail-to-rail. Second, to boost folded cascode transconductance amplifier's (FCTA) A_V, the proposed plurality of regulated cascode (RGC) current mirrors (CM) utilize a small size auxiliary amplifier, containing the same type and un-scaled FETs as that of the cascoded CMs employed within the FCTA. As such, the boosting of A_V is less impeded by the otherwise higher impedance and high capacitance associated with scaled FETs, utilized in most prior art, in the RGC's auxiliary amplifier's signal path. Moreover, the RGC-CM utilizing the same FET, as that of the FCTA's CM, provides more consistency in FCTA's DC, AC, and dynamic response over process and operating condition variations. Third, a buffer driver containing a Minimum Current Selector (MCS) and an inverting current mirror amplifier (ICMA) controls the quiescent current of the inactive output transistors (FETs), while a complementary non-inverting current mirror (CNICM) curbs the current waste attributed to monitoring the FET's (external load) currents. The output buffer driver is inherently fast and can work at low V_{DD}, since it operates mainly in current mode. Montecarlo (MC) and worst case (WC) simulations indicate the following specifications are achievable: input voltage range rail to rail; output voltage range ~ 10mV from the rails; resistive load (R_L) 5K ohms capability; unity gain frequency (fu) ~ 200KHz and phase margin (PM) ~ 40 degrees; power supply rejection ratio (PSRR) ~ -90dB; common mode rejection ratio (CMRR) ~ -110dB; slew rate (SR) ~ 3V/ 10uS; settling time (ts) ~ 15uS; size ~130um/side.**

Keywords — **ultra low power, energy harvesting, self powered IC, transconductance, bioelectronics, amplifier, class AB, buffer, wireless sensor network, rail-to-rail, sink-source, enhanced gain, regulated cascode, auxiliary amplifier, high speed, fast, low power, low current, low voltage, subthreshold, RFID, IoT, wearable electronics, biometrics, sensor array, smart sensor array, smart dust, SSA, batteryless, resistorless, analog.**

I. Introduction

Class AB buffers utilizing folded cascode transconductance amplifiers (FCTA) are suitable for low voltage applications in lieu of their wide rail-to-rail input-output range and being structurally self-compensating, which is generously covered in the analog literature [1]-[27][29]. In ultra low power wireless batteryless applications the extra current, that can lift the gain of an amplifier, is a scarcity. As such, keeping the currents ultra low, while adopting a gain enhancement strategy is useful, where utilizing RGC-CM is an effective mean to boost a FCTA's gain [11-27]. The following additional capabilities of RGC-CM would be beneficial for energy harvesting applications: First, operating with low V_{DD}; second, having wide input-output voltage span; third, providing high PSRR and fast power up and down transient responses, keeping in mind potentially less tidy and jittery V_{DD} patterns in some power harvesting applications; and fourth, exhibiting consistent DC, AC, and transient performance over process and operating variations.

Considering the need, in for example wireless batteryless sensor networks, for an amplifier to drive resistive sensors, the following capabilities are also useful for an output buffer driver: First, operate with low V_{DD} at ultra low I_{DD}; second (to allow FCTA gain stage to dominate the frequency response) the buffer should have a much faster dynamic response than the FCTA; third, having wide input-output voltage span; and fourth, controlling the quiescent current in the inactive output FET driver while having high currents drive capability for the resistive sensor. This work aims to optimize the cost-performance trade-offs in providing a buffer amplifier (patent pending) with the attributes noted above.

TABLE I: Amplifier Typical Specification & Comparisons

Typical Specs	[1] Sim'	[4] SiO2	[6] SiO2	This Work Sim'	See Fig
FOM ($f_u \times L^2 / I_{DD}$)	11.1	2.8	2.3	43.2	
V_{DD} min (V)	2.5	1	1	0.8	2
I_{DD} (nA)	50E3	35E4	15E4	150	3,4
L_{CMOS} (µm)	0.18	0.35	0.35	0.18	
A=Area (µm)^2	94^2	230^2	315^2	130^2	22
Rails - ΔV_{IN}	0	0	0	0	7,8,16
Rails - ΔV_{OUT}	np	?0	np	10mv	7,8,16
SR+/- (V/µs)	11	2.7/5	0.17	0.3	18,19,20,21
$R_L(\Omega)$	np	np	1K	5K	9,10,19,21
t_S (µs) to 1%	0.1	np	np	20	18,19,20,21
f_u (MHz)	17.3	8	0.28	0.2	10,11,12
PM = φ (°)	67.7	60	np	40	10,11,12
PSRR+/- (dB)	93	45/40	np	90	13,14
$CMRR_{1Hz}$ (db)	86.5	75	np	110	15
A_v (db)	99.6	86	90	130	10,11,12
Noise $_{1KHz}$ (nV/$\sqrt{Hz}$)	np	903	np	1400	16

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II. Input And Bias Stage

Note that the entire buffer amplifier operates in the subthreshold region. The input stage of the proposed buffer amplifier depicted in Fig. 1 contains two pairs of PMOSFETs ($P_{i1} - P_{i2,3}$ and $P_{i4} - P_{i6,7}$), where one input pair ($P_{i4} - P_{i6,7}$) is DC level shifted by NMOSFET source followers ($N_{i1} - N_{i2}$) to accommodates rail-to-rail common mode input range [3][10-11][29]. Before the input voltage nears V_{DD}, and at a voltage pre-determined by P_{i9} and N_{i5}, a single PMOSFET (P_{i10}) is activated to steer the same tail current (P_{i8}) between the source summing junction of the two PMOSFET input pairs, $P_{i1} - P_{i2,3}$ and $P_{i4} - P_{i6,7}$ which keeps the input stage's g_m roughly constant throughout the rail-to-rail input span.

The bias stage is amply covered in prior art [28-29], and here is a brief description: It operates with a minimum $V_{DD} \geq V_{GS} + 2V_{DS}$. The $\Delta VGS_{Pb3,4} \approx \eta\, V_T \ln(8)$ is applied across the drain-source terminals of P_{b1} which is in the triode region. Hence, a bias current is generated: $I_B \propto f(\eta_{PMOS} \times \beta_{PMOS} \times V_T{}^2 \times K_b)$, where V_T is thermal voltage, β_{PMOS} is the FET's gain, and K_b is set by FET aspect ratio. Note that the amplifier's I_B is mostly a function of V_T and μ_{PMOS} which are more tightly controlled in fabrication compared to V_{TH}.

III. Gain Stage

Please see Fig. 1. As a general description, the common source amplifier (CSA) section, contained in the enhanced gain FCTA, feeds the $ID_{Pi1} + ID_{Pi4}$ onto the common gate amplifier's (CGA) section of the FCTA's gain stage, containing N_{g2} - N_{g1} [12-27]. Similarly, FCTA's CSA section feeds $ID_{Pi7,3} + ID_{Pi6,2}$ onto FCTA's CGAs containing $N_{g3,5}$ - $N_{g4,6}$. The outputs of CGAs (i.e., I_Ds of N_{g1} - N_{g2} and $N_{g3,5}$ - $N_{g4,6}$) are fed onto the current mirror containing P_{g1} - P_{g2} and $P_{g3,5}$ - $N_{g4,6}$, and summed at node(s) $Z_{N,P}$ which is the high-gain high-impedance output node of the FCTA.

Plurality of RGC-CM are utilized in the CGA section of FCTA to enhance its gain via the auxiliary amplifiers centered around NMOSFETs N_{z4} - N_{g2} and $N_{z15,16}$ - $N_{g4,6}$ and their complementary PMOSFET counterparts P_{z4} - P_{g2}, and $P_{z15,16}$ - $P_{g4,6}$. A brief description of the role of auxiliary amplifier, centered around $N_{z15,16}$ - $N_{g4,6}$, in RGC-CM is provided next, which is also applicable to the other RGC-CM's contained in the buffer amplifier. The basic idea of RGC current mirror (CM) is to raise the effective output impedance of a CM ($N_{g4,6}$) by using negative feedback of an auxiliary amplifier (formed by $N_{z15,16}$ - P_{z17}) with a gain ($G \propto gm_{Nz15,16} \times Ro_{Pz17} \propto V_A/V_T$ in subthreshold) to keep the $VDS_{Ng3,5}$ nearly constant, irrespective of variations at the CM's output voltage ($VD_{Ng4,6}$). As such, the output impedance at the drain terminal of the cascoded current source ($N_{g4,6}$) within the FCTA current mirror network is increased, which enhances the FCTA's gain.

To meet the DC span (rail-to-rail operations at low V_{DD}) objectives, the auxiliary amplifier's (centered around $N_{z15,16}$ - $N_{g4,6}$) input signal is shifted by $VGS_{Nz12,18}$ before it is applied to $N_{z15,16}$ whose drain terminal(s) regulate the $VG_{Ng4,6}$. Note that $VDS_{Ng3,5} = VGS_{Nz8} - VGS_{Nz10} + VGS_{Nz15,16} - VGS_{Nz12,18} \approx \eta_{NMOS} \times V_T \ln(32)$.

Excluding the contribution of output buffer driver to the overall buffer amplifier's gain and frequency response, note that the subthreshold FCTA's bandwidth is roughly $f_u \propto (I_B/V_T)/C_o$, and approximately $A_V \propto (V_A/V_T)^3$, where C_o is the effective capacitance at node(s) $Z_{n,p}$ that is dominated by the aggregate of the sink-source FET drivers C_{gate}[29].

For brevity, the same description as above applies to the other plurality of RGC-CMs (within the CGA section). Please note that single FET current sources are shown in the simplified Fig. 1, where the actual circuit contains cascoded FETs for CM's higher output impedance.

In summary, the benefits of the proposed enhanced gain FCTA stage: First, in setting $VDS_{Ng3,5}$ to widen the RGC-CM input-output voltage span, no FETs with long length (L) or wide width (W) are used in the auxiliary amplifications signal paths, except for scaling N_{z8} to establish a bias voltage. Being

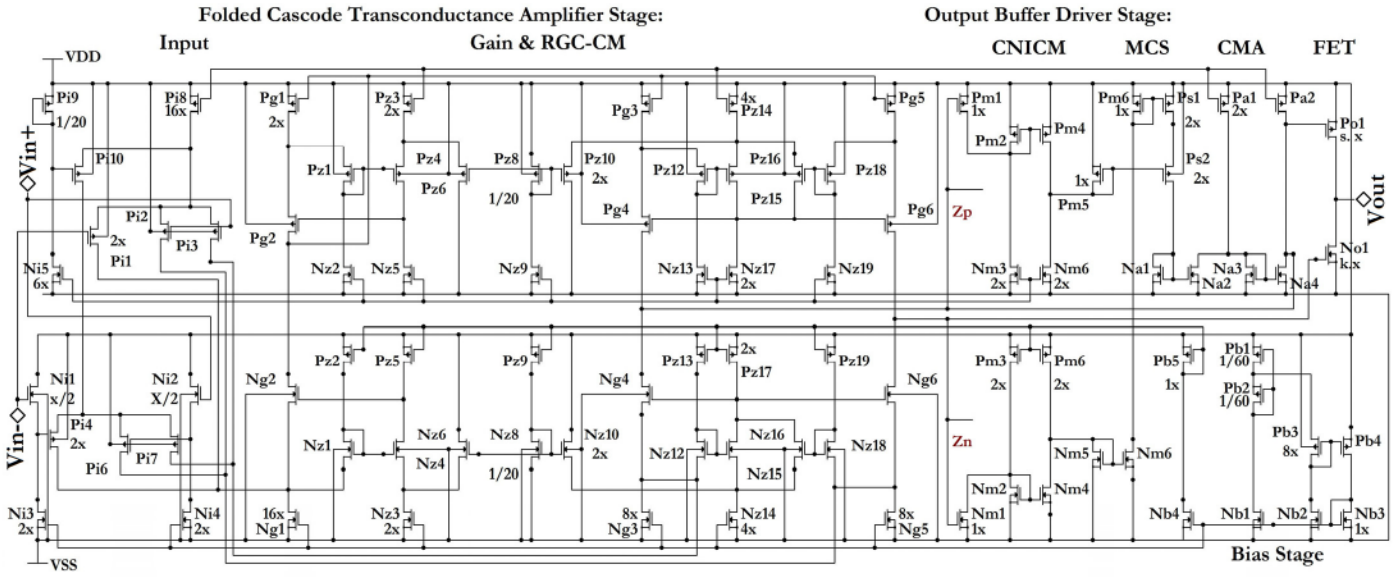

Figure 1. Simplified Amplifer Circuit (output buffer driver stage and RGC-CM patents pending)

mindful of offset and noise considerations, the auxiliary amplifier FETs (e.g., $N_{z12,18}$ and $N_{z15,16}$) can be sized closer to a minimum geometry for RGC-CM's faster speed, by avoiding low admittance or high capacitance FETs in the auxiliary amplifier's signal path. Second, the same type FETs are used in each of the auxiliary amplifiers and their associated cascoded FETs (in the FCTA's CGA current mirror network) whose device parameters match and track each other. Hence, the amplifier's DC, AC, and transient specifications exhibit more consistency over fabrication process, temperature, and power supply variations. Third, low power supply can be accommodated with the minimum $V_{DD} \geq V_{GS} + 2V_{DS}$. Fourth, as stated earlier, energy harvesting applications may require ICs with more rugged and stable transient responses. Availability of harvestable energy may be unpredictable. The V_{DD} patterns may be less orderly for reasons such as power off, power save, or for frequent switching from a magnetic to solar to kinetic power harvesting sources. Hence, the RGC-CM utilizing few FETs with no complicated AC loops, as is the case with the proposed design, could provide more rugged, predictable, and a more stable AC and transient responses.

IV. Output Buffer Driver

Please see Fig. 1. As an introductory description, the CNICM monitors and feeds the MCS, which provides the CMA with the smallest of the output driver FET (sink or source) currents. As such, the loop containing the output buffer driver's elements, including CNICM, MCS, and CMA, in concert with the FCTA controls the minimum operating current in the inactive sink or source FETs [1-10].

The CNICM's inputs (P_{m1}, N_{m1}) mirror and scales down the output FET's (P_{o1}, N_{o1}) sink-source currents, and curb them (P_{m5}, N_{m5}, P_{m6}) at $2I_B$ maximum before heading onto the inputs of MCS (P_{s1}, P_{s2}). During steady state, $I_{Pm5} \approx I_{Nm5} \approx I_B \rightarrow$ MCS's inputs are equalized $\rightarrow$ MCS's output select min $(I_{Pm5}, I_{Pm6}) \approx I_B \rightarrow I_B$ fed onto the input of CMA via N_{a1}. The current equilibrium is established at nodes Z_n and Z_p when in the FCTA: $(I_{Pg6} \approx I_{Ng6}) \approx (I_{Pg4} \approx I_{Ng4})$, and when in the CMA : $I_{Na4} \approx I_{Pa2} \approx I_B \rightarrow I_{Po1} \approx s \times I_B \approx I_{No1} \approx k \times I_B$.

When output FET is serving excess sink-source currents to an external load (R_L), but before steady-state, when either $(I_{Po1} \gg I_{No1})$ or $(I_{No1} \gg I_{Po1}) \rightarrow (I_{Pm5} \gg I_{Pm6})$ or $(I_{Pm6} \gg I_{Pm5}) \rightarrow$ min $(I_{Pm5}, I_{Pm6}) \approx 0$ or min $(I_{Pm5}, I_{Pm6}) \ll I_B \rightarrow$ before steady-state, there is unsustainable current imbalance at nodes Z_n and Z_p. To neutralize such current imbalance, the loop containing FCTA, MCS, and CMA, would regulate VG_{No1}, VG_{Na4}, and VG_{Po1} so that $I_{Pa2} \approx I_{Na4} \approx I_B$ and $(I_{Pg6} \approx I_{Ng6}) \approx (I_{Pg4} \approx I_{Ng4})$.

In the current sink mode, $I_{No1} \gg I_{Po1}$ and before steady-state $\rightarrow$ MCS selects the min $(I_{Pm5}, I_{Pm6}) \approx 0 \approx I_{Na1} \approx I_{Na2} \rightarrow I_{Na3} \approx I_{Na4} \approx 2I_B \rightarrow I_{Na4} > I_B$ and $I_{Na4} > I_{Pa2}$ that is unsustianble, which the loop regulates until steady-state is arrived by equalizing $I_{Pa2} \approx I_{Na4} \approx I_B$. Therefore, the loop regulates the inactive source FET current when $I_{Na1} \approx I_B \approx I_{Pm5} \approx I_{Pm1} \approx I_{Po1} \times 1/s$ while the active sink FET, N_{o1}, sinks the excess current needed for R_L.

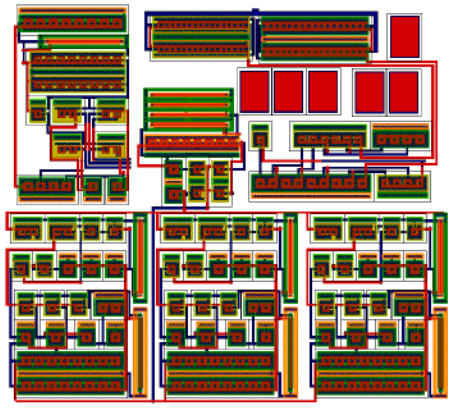

Fig. 2. Preliminary layout and rough area estimate ~ $130\mu m^2$

Similarly, in the current source mode, $I_{Po1} \gg I_{No1}$ and before steady-state $\rightarrow$ MCS selects the min $(I_{Pm5}, I_{Pm6}) \approx 0$ and the loop regulate node Z_n and Z_p by an infinitesimal lift in $(I_{Ng4} \approx I_{Ng6})$ above $(I_{Pg4} \approx I_{Pg6})$ which increases the Z_n and Z_p voltages tiny enough in order for N_{o1} (and its mirror N_{m1}, N_{m5}, and P_{m6}) turn back on enough so that steady-state current equilibrium is reached and $I_{Pa2} \approx I_{Na4} \approx I_B$. As such, the loop regulates the inactive sink FET current where $I_{Na1} \approx I_B \approx I_{Pm6} \approx I_{Nm6} \approx I_{Nm5} \approx I_{Nm1} \approx I_{No1} \times 1/k$ while the active source FET, P_{o1}, sources the excess current needed for R_L.

Here is a summary of the benefits of the proposed output buffer driver: First, it can work with low power supply minimum $V_{DD} \geq 2V_{DS} + V_{GS}$. Second, all elements of the output buffer driver namely CNICM, MCS, and CMA mostly operate in the current mode, which inherently makes the buffer's dynamic response fast. Third, it is low cost, given the low number of FET. Fourth, it can accommodate rail-to-rail input-output voltage span. Fifth, it can control the output FET's steady state quiescent current, and regulate the current in the inactive sink or source FET. Sixth, CNICM curbs the current that is otherwise wasted, while monitoring the FET's sink-source associated with variety of R_Ls.

V. Monte Carlo & Worst Case Simulations:

A set of performance specification comparisons, with selected prior arts, are provided in Tables I. The WC and MC simulations are performed based on BSIM3v3.1 MOSIS/TSMC equivalent 0.18μm CMOS device models. Fig. 2 is a rough layout area $(\sim 130\mu m)^2$. The amplifier simulations, which are illustrated in Fig. 3 through Fig. 26, are configured in unity gain, $V_{DD} = 2v$, Temperature (T) = 27°C, unless otherwise noted. Figure 3 is WC simulations showing minimum $V_{DD} \sim 0.8v$ measured by increasing V_{DD} until the steady state for Vin_{OFS} and I_{DD} is reached. Figure 4 is MC with average $I_{DD} \approx 149nA$. Figure 5 shows WC $I_{DD} \leq 195nA$ as a function of temperature $-35°C \leq T \leq +65°C$. Figure 6 is MC for $-4.6mv \leq Vin_{OFS} \leq +4.5mv$. Figure 7 shows WC $Vin_{OFS} \leq 300\mu V$ as a function of temperature $-35\,°C \leq T \leq +65°C$.

BUFFER AMPLIFIER'S SIMULATION SUMMARY

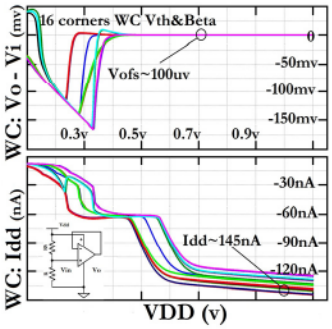

Fig. 3. WC Min' V_{DD} vs. I_{DD} & V_{OFS}

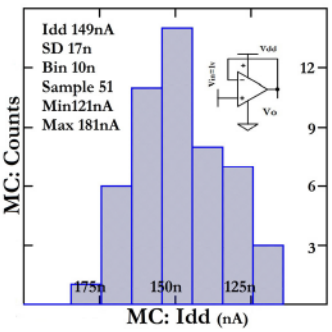

Fig. 4. MC I_{DD}

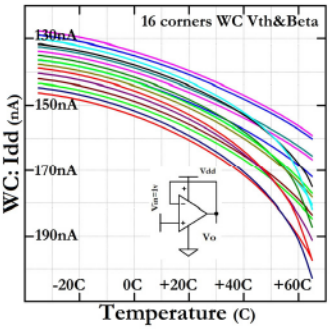

Fig. 5. WC I_{DD} vs. T

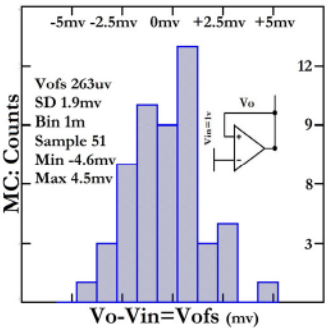

Fig. 6. MC V_{OFS}

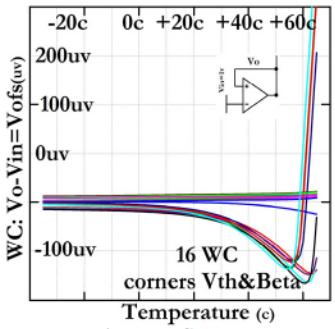

Fig. 7. WC V_{OFS} vs. T

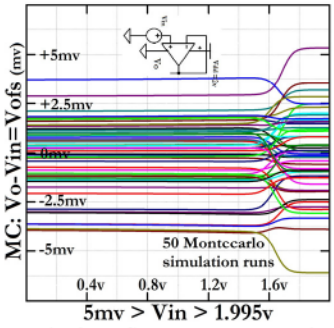

Fig. 8. WC V_{OFS} vs. V_{IN}, V_{DD}=2v

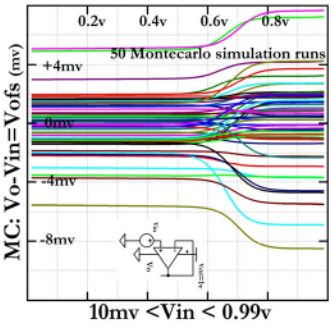

Fig. 9. MC V_{OFS} vs. V_{IN}, V_{DD}=1v

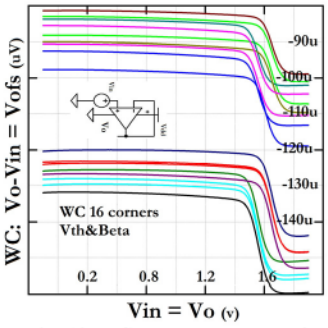

Fig. 10. WC V_{OFS} vs. V_{IN}, V_{DD}=2v

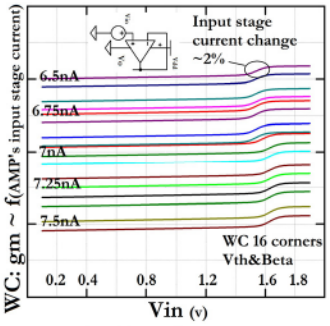

Fig. 11. WC gm vs V_{IN}

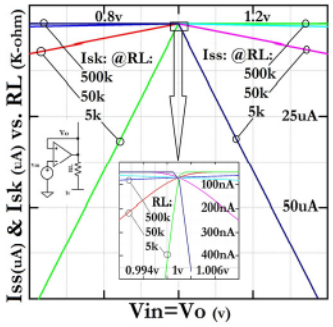

Fig. 12. V_{IN} vs. R_L ($I_{SINK-SOURCE}$)

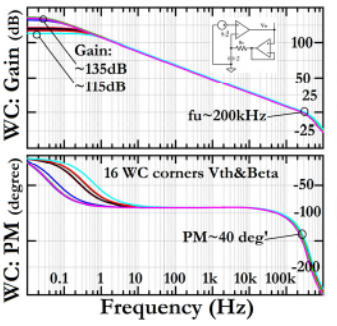

Fig. 13. WC AC reponse

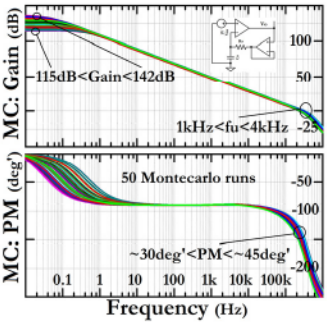

Fig. 14. MC AC reponse

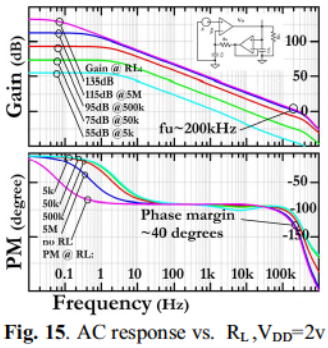

Fig. 15. AC response vs. R_L, V_{DD}=2v

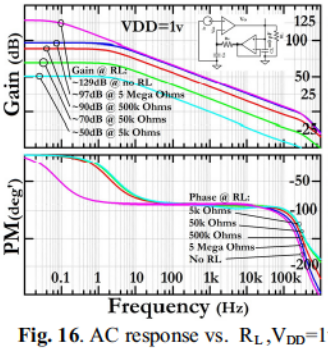

Fig. 16. AC response vs. R_L, V_{DD}=1v

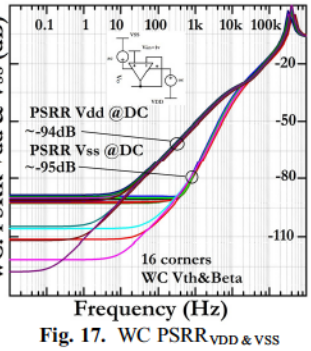

Fig. 17. WC $PSRR_{VDD\,\&\,VSS}$

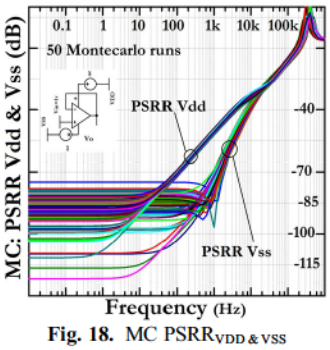

Fig. 18. MC $PSRR_{VDD\,\&\,VSS}$

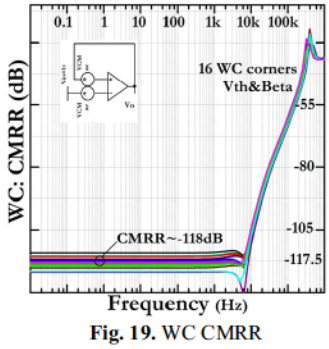

Fig. 19. WC CMRR

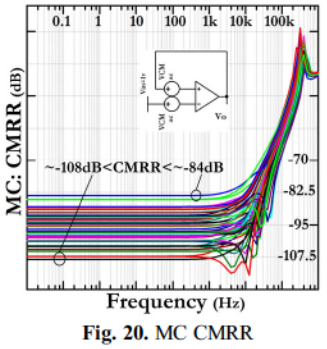

Fig. 20. MC CMRR

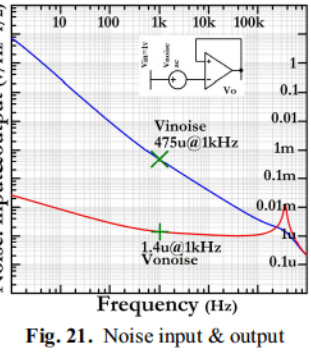

Fig. 21. Noise input & output

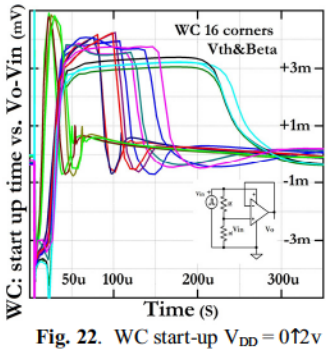

Fig. 22. WC start-up V_{DD} = 0↑2v

AMPLIFIER'S SIMULATION SUMMARY CONTINUED

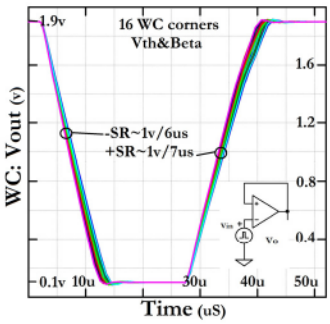

Fig. 23. WC τ_s & SR, V_{DD}=2v

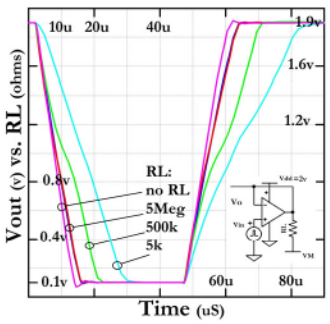

Fig. 24. τ_s & SR vs. R_L, V_{DD}=2v

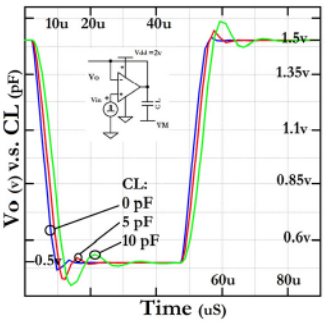

Fig. 25. τ_s & SR vs. C_L, V_{DD}=2v

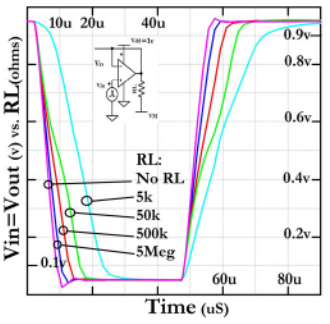

Fig. 26. τ_s & SR vs. R_L, V_{DD}=1v

Figure 8 is MC for Vin_{OFS} at $V_{DD} = 2v$ while spanning $5mv \leq V_{IN} = V_{OUT} \leq 1.995v$, results in $-6.5mv \leq Vin_{OFS} \leq +5mv$ due mostly to mismatch between the first PMOS versus the second PMOS+NMOS input pairs resulted when V_{IN} nears the rails. Figure 9, similar to Fig. 8, is the MC for Vin_{OFS} at $V_{DD} = 1v$ while spanning $10mv \leq V_{IN} = V_{OUT} \leq 0.99v$, which results in $-8mv \leq Vin_{OFS} \leq +8mv$. Figure 10 is WC for Vin_{OFS} with $V_{DD} = 2v$ where spanning $50mv \leq V_{IN} = V_{OUT} \leq 1.95mv$, results in $-160\mu v \leq Vin_{OFS} \leq -80\mu v$. Figure 11 is WC Δg_{mT} vs. V_{IN} indicating a ~ 2% variation in amplifier's input stage g_m as a function of the change in PMOSFET input pair's current versus $V_{IN} = V_{OUT}$ spanning rail-to-rail. Figure 12 is sink-source output FET current, I_{SINK} and I_{SOURCE} , as a function of external load R_L=5KΩ, 50KΩ, and 500KΩ versus $50mv \leq V_{IN} = V_{OUT} \leq 1.95mv$. Figure 13 is WC AC response which indicates $115dB < A_V < 135dB$ with unity gain frequency $f_u \approx 200kH$, and phase margin $\varphi \approx 40°$. Figure 16 is AC response as a function of R_L with $V_{DD} = 1v$. Figure 17 is WC PSRR indicating at DC: $-90dB < PSRR_{VDD} < -135db$ and $-92dB < PSRR_{VSS} < -130db$. Figure 18 is MC PSRR indicating at DC: $-80dB < PSRR_{VDD} < -110db$ and $-83dB < PSRR_{VSS} < -120db$. Figure 19 is WC CMRR indicating at DC: $-114dB < CMRR < -125db$. Figure 20 is MC CMRR indicating at DC: $-84dB < CMRR < -108db$. Figure 21 is typical $VO_{Noise} = 1.4\mu V/\sqrt{Hz}$ at 1kHz, $VI_{Noise} = 475\mu V/\sqrt{Hz}$ at 1kHz which is based on very preliminary noise models. Figure 22 is WC $t_{start-up} \leq 350\mu s$ with V_{DD} pulsed to 2V from 0 (and $V_{in} = 1/2V_{DD}$ and amplifier is in unity gain). Figure 23 is WC transient response (TR) for $V_{in} = V_O$ that is stepped to 1.9v from 0.1v which shows SR > ~1v / 7μS and τ_s < ~ 20 μS, with $V_{DD} = 2v$. Figure 24 is TR vs. R_L for $V_{in} = V_O$ stepped to 1.9v from 0.1v, for R_L = 5kΩ, 50kΩ, and 500kΩ , with $V_{DD} = 2v$. Figure 25 is TR vs. C_L for $V_{in} = V_O$ stepped to 1.5v from 0.5v, for C_L = 0pF, 5pF, and 10pF. Figure 26 is TR vs. R_L for $V_{DD} = 1v$ $V_{in} = V_O$ stepped to 950mv from 50mv, for R_L = 5KΩ, 50KΩ, 500kΩ, and 5MΩ.

VI. Specifications Risk From Simulation to Fabrication & Design Gaurd-bands

Given the ultra low currents, the transient injection could cause prolonged settling time within the amplifier's (high impedance) bias network. To guard band against such jitters, each of the biasing circuits for the input, gain, and output buffer driver stages are segregated. For conservatism, a power-on-reset (POR) function is added to the bias stage, although simulations indicate self start-up due to source-drain junction leakage currents. The PSRR and CMRR results in silicon are subject to substrate currents, FET parasitic leakages, and FET mismatches, which are not completely modeled in SPICE. The amplifier is optimized to drive resistive loads (e.g., use of resistors sensors in sensor array networks utilizing a power harvesting source) and it is not suited to drive capacitive loads. Also, cross-over distortion will be high at the output stage operating at ultra low currents. The input offset voltage mismatch between the PMOS and PMOS+NMOS paths will appear as distortion. Operating at ultra low currents elevates noise, and noise models are approximate. Amplifier's performance at high temperature will be degraded due to leakage, exacerbated by operating the amplifier at ultra low currents. FETs with small W and L mismatch more and are more noisy, while smaller FETs with smaller source-drain junction areas leak less. Smallest W/L used in this design is 3 times larger than minimum. Offset mismatch over temperatures is not modeled and not captured in the simulations. Metal mask options with compensation capacitors near $Z_{n,p}$ and V_{out}, and extra dummy FETs (e.g., larger N_{o1} and P_{o1}) will be provided in layout as a back-up plan for stability and extra output current drive capability.

VII. Conclusion

A rail-to-rail input-output buffer amplifier is presented that consumes 150nA of current, operates with low V_{DD} ~ 0.8v, has gain of 130dB, and can drive a 5KΩ load while accurately controlling the inactive sink-source FET currents. The input stage uses two pairs of PMOSFETs, with one pair that is DC level shifted using a NMOSFET source follower to facilitate input rail-to-rail span, while a single FET steers the tail current between the two PMOSFET to keep the amplifier's input transconductance stable during rail-to-rail input span. The gain

stage utilizes a simple regulated cascode current mirror topology, that uses the same type FETs as the folded cascode amplifier's current mirrors, to enhance its gain, accommodate rail-to-rail performance at low V_{DD} , and to provide consistent AC and DC performance over the span of process and operating variations. The output stage runs mostly in current mode that help the speed at low V_{DD}, with input-output rail-to-rail span, and capable of curbing current waste associated with monitoring the output stage FET driver currents.

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Ali Far received the B.S. in EECS from UC Berkeley in 1983. He got his MSEE in 1986, MBA. in 1989, Juris Doctor in Law in 1997, and M.A. in Psychology in 2010, all from Santa Clara University. He is working on his M.A. in Philosophy at SFSU. He joined Plantronics in 1982 as an Audio Engineer. Between 1983 to 1985 he was a data converter Design Engineer with PMI (now part of ADI). From 1985 to 1992, he worked at MPS (now part of MaxLinear) as Design and Marketing Manager working on converters, S/Hs, high-speed amplifiers, and regulators. Then, Ali joined MVT (now part of Creative Labs) as Director of Design, making multi-media chips. Between 1994 to 1997, he worked at TelCom (now part of Microchip) as VP of Design, where he developed converters, high-power regulators, and power management chips. In 1998, Ali joined Prudential Securities, as a Semiconductor Analyst and Vice President covering investments in the analog industry. Between 2000 to 2006, he worked at Galleon, where he was an Analyst and Managing Director covering technology equities broadly, including semiconductors, storage, wireless, and networking sectors. In 2008, he founded Spherix where he worked as an Analyst and Portfolio Manager focused on technology investments. Ali has published several papers in IEEE, has 13 patents and some pending in the area of analog ICs, and is currently researching analog chips for energy harvesting.