Compact Ultra Low Power Class AB Buffer Amplifier

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***Abstract* — Targeting the energy harvesting applications that require multiple channels of matched buffer amplifiers on a chip, a small rail-to-rail input-output, ultra low current, and low supply voltage (V_{DD}) buffer amplifier is presented. The contributions of this work are as follows: First, an output buffer driver utilizes a loser-take-all circuit (LTA) and a current mirror amplifier (CMA) circuit to regulate the current in either of the inactive sink or source output driver transistors (FET). In conjunction with the LTA and CMA, a complementary non-inverting current mirror (CNICM), monitors and rectifies the sink-source output signals before they are fed to the LTA circuit. Hence, the amplifier's current consumption, attributed to monitoring external loads, is substantially curbed. More importantly, because all the elements of the buffer driver (LTA, CMA, and CNICM) operate mainly in current mode, the output buffer driver is structurally fast and can operate with low V_{DD} of about $V_{GS}+2V_{DS}$. Second, a floating current source (FCS) function is emulated that can also operate with low V_{DD} and is fast in lieu of utilizing auxiliary common gate amplifiers (CGA). The FCS contains two complementary cascoded FET current sources where the middle cascoded FET's V_{GS}s are held constant and their drain currents are criss-crossed and fed to each other's source terminals, while CGAs regulate the V_{GS}s of the lower FETs, whose currents are substantially equalized and mirrored into the Amplifier's bias network. Montecarlo (MC) and worst case (WC) simulations indicate the following specifications are achievable: V_{DD} minimum ~ 0.8v; I_{DD} ~ 200nA; input voltage range rail to rail; output voltage range ~ 10mV from the rails; open loop gain (A_V) ~ 115dB with unity gain bandwidth (f_U) ~ 600KHz and phase margin (PM) ~ 30 degrees; power supply rejection ratio (PSRR) ~ - 88dB; common mode rejection ratio (CMRR) ~ - 120dB; slew rate (SR) ~ 2V/ 5uS; settling time (t_S) ~ 10uS; output resistor (R_L) capability ~10K Ohms; and die size rough estimate is 100 um per side.**

Keywords — **buffer class AB amplifier, floating current source, loser take all, minimum current select, subthreshold, rail-to-rail, ultra low current, low voltage, bioelectronics, self-powered integrated circuits, wireless sensor network, smart dust, folded cascode transconductance amplifier, high speed, fast, internet of things, energy harvesting, wearable electronics, biometrics, smart sensor array, batteryless, resistor free.**

I. Introduction & The Contributions of This Work

The emerging markets such as energy harvesting, self-powered ICs, bio-metrics, wearable electronics, batteryless IoT and WSN, to name a few, generally require class AB buffer amplifiers [1-21][24] having the following characteristics: (1) low cost and rugged quality for high-volume applications based on standard CMOS fabrications, (2) small size to match DC, AC, and transient specifications between multiple amplifier channels on a chip, such as octal or 16-channels, (3) ultra low currents, (4) rail-to-rail input-output voltage span, (5) low V_{DD}, (6) controlled low currents in the inactive output driver FET while being capable sinking and sourcing large currents for low resistive loads. For example, in simultaneous toxicity detection, multiple toxicity sensor's resistance can drop significantly with sensors activation, (7) powering up the IC with different back-up harvesters, such as solar combined with kinetic, may impose inconsistent V_{DD} patterns on the IC. Moreover, the availability of harvestable power may be unpredictable. Such applications would benefit from an amplifier's fast power-up times and better PSRR performance.

TABLE I: Amplifier Typical Specification & Comparisons

Typical Specs	[1] Sim'	[2] Sim'	[3] SiO2	This Work Sim'	See Fig
FOM (f_u/I_{DD})	3.4	3.6	0.03	30	
V_{DD} min (V)	2.5	1.8	np	0.8	2
I_{DD} (nA)	50E3	83E4	325	200	3,4
L_{CMOS} (µm)	0.18	0.18	0.18	0.18	
A=Area $(\mu m)^2$	94^2	np	62^2	100^2	22
Rails - ΔV_{IN}	0	200m	np	0	7,8,16
Rails - ΔV_{OUT}	np	200m	np	10mv	7,8,16
SR+/- (V/µs)	11	1280	0.6	0.4	18,19,20,21
$R_L(\Omega)$	np	np	np	10k	9,10,19,21
t_S (µs) to 1%	0.1	0.0066	np	10	18,19,20,21
f_u (MHz)	17.3	300	0.01	0.6	10,11,12
PM = φ (°)	68	81	90	30	10,11,12
PSRR+/- (dB)	93	np	np	88	13,14
$CMRR_{1Hz}$ (db)	87	np	np	120	15
A_v (db)	100	53	60	115	10,11,12
Noise $_{1KHz}$ $(nV/\sqrt{Hz})$	np	np	np	680	16

Besides meeting the requirements outlined above, the incremental contributions of this rail-to-rail buffer amplifier are: First, a simple circuit that emulates the function of a FCS (patent pending) is presented that is suitable for complementary rail-to-rail FCTAs. The proposed FCS runs with low V_{DD} and it makes the FCTA bias current less sensitive to common mode voltage swings. Second, a small output buffer driver (patent pending) is presented that is composed of CNICM, LTA, and CMA, all of which operate chiefly in current mode that enables the output driver buffer to run fast and with low V_{DD}. Although the proposed buffer amplifier is tailored for ultra low power applications, but its benefits can be extended by operating the FETs in normal mode, instead of the subthreshold region, as in for example high current and high-speed applications.

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II. Floating Current Source & Amplifier

Please see Fig. 1 that depicts FCS (patent pending) [1-21][24]. The proposed low voltage FCS contains two cascode current sources, the lower N_{f6}, N_{f5} and the upper P_{f5}, P_{f6}. The I_{Pf4} biases N_{f3} which controls VGS_{Nf6} and thereby sets I_{Nf6}. The I_{Nf4} biases P_{f3} which controls VGS_{Pf6} and thereby sets I_{Pf6}. Functioning as a first auxiliary common gate amplifier (CGA:P_{f4}, N_{f3}) regulates the VGS_{Nf5} until $I_{Nf5} = I_{Pf4}+I_{Nf6}+I_{Pf6}$. Concurrently, the second auxiliary amplifier (CGA: N_{f4}, P_{f3}) regulates the VGS_{Pf5} until $I_{Pf5} = I_{Nf4} + I_{Pf6} + I_{Nf6}$. Given that $I_{Nf4} = I_{Pf4} = i$, hence $I_{Pf5} = I_{Nf5} = 3i$, which biases up the current mirrors (N_{a5}, N_{a6} and P_{a5}, P_{a6}) in the FCTA gain stage. In summary, some of the benefits of utilizing the proposed FCS are that (1) it uses a few FETs and it is small, (2) it can operate at low V_{DD}, (3) utilizes CGA topology that is inherently fast, which helps speed up the dynamic response of FCTA, and (4) it provides reasonable matching between upper and low cascoded current sources which improves amplifier's offset and noise, Note that here, the g_m variations, due to complementary FCTA inputs getting cut off at either rails, are not corrected because the savings in current consumption, die area, and impact on dynamic response outweighs the benefit of tail current correction.

The bias stage can also work at low power supply ($V_{DD} \geq V_{GS} + 2V_{DS}$), where bias current ($I_{BIAS}$) is generated by applying $\Delta VGS_{Pb3,4} \approx \eta V_T \ln(8)$ across drain-source of P_{b1} which is the active resistor [22-24]. Here, $I_{BIAS} \propto f(\mu_{PMOS}, V_T)$ where μ_{PMOS} and V_T are tightly controlled in fabrication.

Setting aside the contribution of the output buffer driver, this category of subthreshold FCTA's gain $A_V \propto (V_A/V_T)^2$ and its bandwidth is roughly $f_u \propto (g_m/C_o) \propto (I_{BIAS}/V_T)/C_o$, where C_o is the effective capacitance at nodes Z_N and Z_P [26].

III. Output Buffer Driver

Please see Fig. 1 that illustrates the simplified buffer driver (patent pending) circuit schematic. Output FETs contain P_{o1} and N_{o1} . The CNICM mirrors, scales, and rectifies the FET currents. It contains $P_{m1}, P_{m2}, P_{m4}, P_{m5}$ plus N_{m3}, N_{m6} on the upper level, and $N_{m1}, N_{m2}, N_{m4}, N_{m5}$ plus P_{m3}, P_{m6} on the lower level. The LTA, receives the CNICM rectified outputs, and in effect compares and selects the smallest of the two currents flowing in P_{o1} and N_{o1}. The LTA circuit contains N_{L1}, N_{L2}, N_{L3} plus P_{L1}, P_{L2}. The CMA, in concert with the FCTA, regulates the current in the inactive FET based on the LTA signal. The CMA circuit contains N_{m1}, N_{m2}, N_{m4}.

Let's first discuss the steady state condition (φ_{SS}) when there is current equilibrium at nodes Z_N and Z_P, and there is no external load (R_L). Let's set aside non-idealities (e.g., no offsets or mismatches), $k = s$, and operate current mirrors at $i = I_{BIAS}$. Here, $I_{No1} \approx k \times i \approx I_{Po1} \approx s \times i \rightarrow I_{Nm1} \approx i \approx I_{Pm1} \rightarrow I_{Pm3} \approx 2i$ and $I_{Nm3} \approx 2i$ are split in half $\rightarrow I_{Nm1} \approx I_{Nm2} \approx i \approx I_{Nm4}$ and $I_{Pm1} \approx I_{Pm2} \approx i \approx I_{Pm4}$. Also, $I_{Pm6} \approx 2i$ and $I_{Nm6} \approx 2i$ are also split in half $\rightarrow I_{Pm4} \approx i \approx I_{Pm5} \approx I_{PL1} \approx I_{PL2}$, and $I_{Nm4} \approx i \approx I_{Nm5} \approx I_{NL1}$. Note that I_{Pm5} and I_{Nm5} represent the inputs, and I_{Nr1} represents the output of the LTA circuit. The I_{Nr1} also represents the input to the CMA. In φ_{SS}: $I_{NL1} \approx i \approx I_{PL1} \rightarrow I_{PL1} - I_{NL1} \approx I_{NL2} \approx 0 \approx I_{NL3} \rightarrow$ The CMA receives all of $I_{PL2} \approx i$ current that flows through $N_{r1} \rightarrow I_{PL2} \approx I_{Nr1} \approx I_{Nr2} \approx i$ which is equal to the current in $I_{Pr1} \approx i$. In summary, during φ_{SS}, LTA selects current equality with LTA (I_{Pm5}, I_{Nm5}) $\approx I_{Pm5} \approx I_{Nm5} \approx i$, which is fed onto the input of CMA via N_{r1}. Accordingly, in the CMA: $I_{Nr1} \approx I_{Nr2} \approx I_{Pr1}$. During φ_{SS} and current equilibrium at nodes Z_P and Z_N: ($I_{Pa8} \approx I_{Na8}$) $\approx$ ($I_{Pa7} \approx I_{Na7}$) along with $I_{Nr2} \approx I_{Pr1} \rightarrow$ sink-source output FETs operate at $I_{No1} \approx k \times i \approx I_{Po1} \approx s \times i$

In the sink mode, but before φ_{SS}, the internal node Z_P and Z_N are initially pulled up towards $V_{DD} \rightarrow N_{O1}$ and N_{m1} are turned on hard $\rightarrow I_{No1} \gg i$ and $I_{Nm5} \approx 2i$. Also, prior to φ_{SS}: P_{o1} and P_{m1} are turned off or are nearly off $\rightarrow I_{Pm5} \approx 0 \rightarrow I_{PL1} \approx I_{PL2} \approx I_{Pm5} \approx 0$ and $I_{Nm5} \approx 2i \approx I_{NL1} \rightarrow$ The drain terminal of N_{L2} is pulled down towards $V_{SS} \rightarrow I_{NL2} \approx 0 \approx I_{NL3} \rightarrow$ Thus, before φ_{SS}: $I_{PL2} \approx 0 \approx I_{NL3} \rightarrow I_{Nr1} \approx 0 \approx$

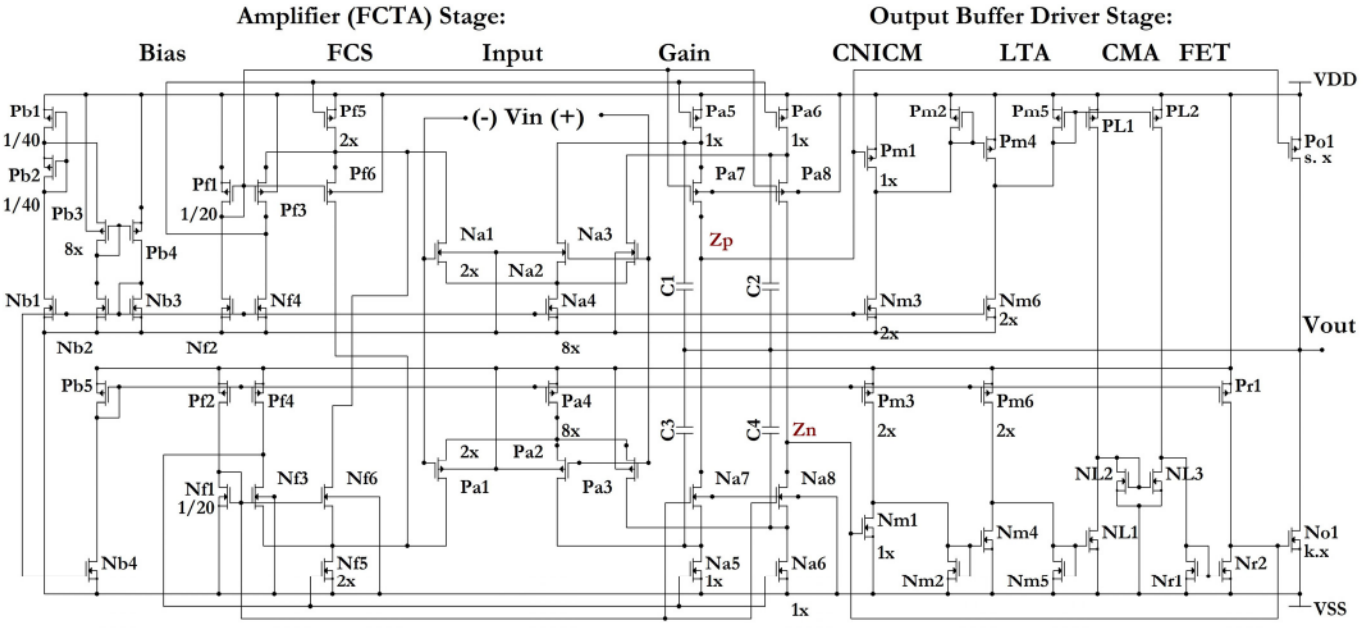

Figure 1. Simplified Amplifer Circuit (the floating current source and output buffer driver stage patents pending)

I_{Nr2}. In summary so far before φ_{SS}, the LTA (I_{Pm5} , I_{Nm5}) $\approx I_{Pm5} \approx 0$ is fed onto $N_{r1} \rightarrow I_{Nr1} \approx I_{Nr2} \approx 0 < I_{Pr1} = i$ at node Z_N which is a current imbalance. Accordingly, to neutralize this current imbalance, the loop containing FCTA coupled with LTA and CMA, regulate node Z_N by an infinitesimal increase in $(I_{Na7} \approx I_{Na8})$ above $(I_{Pa7} \approx I_{Pa8})$ which pulls down the voltages at Z_P and Z_N nodes minutely enough until P_{o1} (and its mirror $P_{m1}$and P_{m5}) turn back on sufficiently for $I_{Pm1} \approx I_{Pm2} \approx i \approx I_{Pm4} \approx I_{Pm5} \rightarrow I_{PL1} \approx i \approx I_{PL2}$, as the loop moves towards the φ_{SS} condition. Given the high-impedance of node Z_N, a tiny increase in I_{Pr1}, countering the infinitesimal increase of I_{Na8} over I_{Pa8}, can lift up V_G of N_{O1} enough for sinking excess current for an external load. Converging towards φ_{SS}, while N_{o1} can continue sinking current for an external load $\rightarrow I_{Nm1} \gg i \rightarrow I_{Nm5} \approx 2i \approx I_{NL1} \rightarrow I_{NL1} \approx 2i > I_{PL1} \approx i \approx I_{PL2} \rightarrow I_{NL1}$ pulls down on the drain terminal of N_{L2} towards $V_{SS} \rightarrow I_{NL2} \approx 0 \approx I_{NL3} \rightarrow$ the loop approaching φ_{SS}, with $i \approx I_{PL2}$, then $I_{PL2} - I_{NL3} \approx i$ is fed onto $N_{r1} \rightarrow I_{Nr1} \approx i \approx I_{Nr2} \approx I_{Pr1}$, which is current equilibrium at node Z_N. Just to summarize, having reached φ_{SS} current equilibrium at nodes Z_P and Z_N, the N_{o1} is still sinking excess currents: $I_{NO1} > I_{PO1} \rightarrow I_{Nm1} > I_{Pm1} \rightarrow I_{Nm5} \approx 2i > I_{Pm5} \approx i \rightarrow$ LTA$(I_{Pm5}, I_{Nm5}) \approx I_{Pm5} \approx i \leftrightarrow I_{Pm1} \approx i \approx I_{Po1} \times 1/s$, which demonstrates how the quiescent operating current for P_{o1} (inactive source FET) is reached, while the active FET, N_{o1}, continues sinking current for R_L.

In the current source mode, but before φ_{SS}, the Z_P and Z_N nodes are pushed down towards $V_{SS} \rightarrow P_{o1}$ and P_{m1} turn on and N_{o1} and N_{m1} turn off $\rightarrow$ before φ_{SS} current equilibrium, $P_{m5} \approx 2i$ and $N_{m5} \approx 0 \rightarrow$ In the LTA: $I_{Pm5} \approx 2i \approx I_{PL1} \approx I_{PL2}$, and $I_{Nm5} \approx 0 \approx I_{NL1} \rightarrow I_{PL2} - I_{NL1} \approx 2i \approx I_{NL2} \approx I_{NL3} \rightarrow$ before φ_{SS}: $I_{PL2} - I_{NL3} \approx 2i - 2i \approx 0 \rightarrow$ the net current is fed onto $N_{r1} \rightarrow I_{Nr1} \approx I_{Nr2} \approx 0 < I_{Pr1}$. In summary so far, before φ_{SS} current equilibrium, the LTA $(I_{Pm5}, I_{Nm5}) \approx I_{Nm5} \approx 0$ that is fed onto CMA $\rightarrow I_{Nr1} \approx I_{Nr2} \approx 0 < I_{Pr1} \approx$ i, which is a current imbalance. Accordingly, to neutralize this current imbalance, the loop containing FCTA coupled with LTA and CMA, lifts the V_G of N_{o1} and N_{m1} enough until $I_{Nr2} \approx I_{Pr1} \approx i$. Note that φ_{SS} current equilibrium at nodes Z_P and Z_N are satisfied when $(I_{Na8} \approx I_{Pa8}) \approx (I_{Na7} \approx I_{Pa7})$ and $I_{Nr2} \approx I_{Pr1} \approx i$, which occurs after the said loop regulates node Z_N high enough $\rightarrow I_{Nm1} \approx I_{Nm5} \approx i \approx I_{NL1}$, while P_{o1} continues to source excess current for an external load $\rightarrow I_{Pm1} \gg i \rightarrow I_{Pm5} \approx 2i \approx I_{PL1} \approx I_{PL2} \rightarrow I_{PL1} - I_{NL1} \approx i$, which is fed onto $I_{NL2} \approx i \approx I_{NL3} \rightarrow$ Moving towards φ_{SS} current equilibrium, $I_{PL2} - I_{NL3} \approx i \approx I_{Nr1} \approx I_{Nr2} \approx I_{Pr3}$ which is current balance at node Z_N. In summary, during φ_{SS} the P_{o1} can source current for R_L , while the loop regulates nodes Z_P and Z_N : Here $I_{Po1} > I_{No1} \rightarrow I_{Pm1} > I_{Nm1} \rightarrow I_{Pm5} > I_{Pm5} > I_{Nm1} \rightarrow$ at φ_{SS}: LTA$(I_{Pm5}, I_{Nm5}) \approx I_{Nm5} \approx i$ which is fed onto CMA via $I_{Nr1} \approx i \approx I_{Nr2} \approx I_{Pr3}$. As such, $I_{Nm1} \approx i \approx I_{No1} \times 1/k$, which demonstrates how the quiescent operating current for, N_{o1} (inactive sink FET) is reached, while the active FET, P_{o1}, continues sourcing current for the external load.

In summary the benefits of the proposed output buffer driver are as follows (1) buffer's FET count is small transistor which makes it low cost (2) it can operate at minimum $V_{DD} \geq 2V_{DS} + V_{GS}$, (3) the CNICM, LTA, and CMA chiefly operate in current mode which makes the buffer inherently fast, (4) CNICM effectively curbs the current consumption attributed to monitoring various R_Ls, (5) relatively wide bandwidth of the output buffer driver enables the FCTA to dominate the frequency response dynamics of the buffer amplifier, (6) operating in subthreshold, the buffer driver can run at ultra low currents, work with low V_{DD}, and have near rail-to-rail input-outputs, (7) it can provide high sink-source drive capability and controlled quiescent current in the inactive output sink-source FETs (8) it's based on standard CMOS process which is low cost, high quality, and readily available, and (9) the buffer driver arrangement utilizing CNICM coupled with LTA coupled with CMA can be tailored for high currents and high speeds.

IV. Monte Carlo & Worst Case Simulations:

Comparison table of specifications between some prior art and this work proposed is provided in Tables I. MOSIS/TSMC equivalent models are used for WC and MC simulations based on BSIM3v3.1 for 0.18µm CMOS. The $V_{DD} = 2v$, amplifier is in unity gain, Temperature (T) = 27℃, unless otherwise specified. Figure 2 is the WC indicating minimum V_{DD}~0.8v measured by increasing V_{DD} until V_{ofs} and I_{DD} reach the steady state levels. Figure 3 is the MC with average $I_{DD} \approx 196nA$. Figure 4 shows the WC for $I_{DD} \leq 260nA$ throughout $-50\,℃ \leq T \leq +70℃$. Figure 5 is the MC for $-2mv \leq Vin_{OFS} \leq +2mv$. Figure 6 demonstrates WC $Vin_{OFS} \leq 300\mu V$ throughout $-50\,℃ \leq T \leq +70℃$. Figure 7 is the MC for Vin_{OFS} with $V_{DD} = 2v$ when spanning $50mv \leq V_{in} = V_{out} \leq 1.95v$, results in $-3mv \leq Vin_{OFS} \leq +3mv$ due to PMOS-NMOS FET mismatches when inputs hit the rails. Figure 8 is the WC for Vin_{OFS} with $V_{DD} = 0.8v$ when spanning $10mv \leq V_{in} = V_{out} \leq 790mv$, results in $0 \leq Vin_{OFS} \leq +150\mu v$. Figure 9 is the output driver FET currents, I_{SINK} and I_{SOURCE}, graphed as a function of R_L=10KΩ, 100KΩ, and 1MΩ, versus $50mv \leq V_{in} = V_{out} \leq 1.95v$. Figure 10 is the gain versus phase margin versus R_L = 50KΩ, 500KΩ, 5MΩ, and 50MΩ, versus frequency. Figure 11 is the WC gain versus phase margin versus frequency, which depicts typical $A_V \approx 116dB$ with $f_u \approx 600kH$ and $\varphi \approx 30°$. Note that the amplifier's DC gain, without the buffer stage, is typically about 75dB. Figure 12 is the MC gain versus phase margin versus frequency. Figure 13 is the WC PSRR for both V_{DD} ($\approx -88dB$) and V_{SS} ($\approx -89dB$) versus frequency. Figure 14 is MC PSRR for both V_{DD} and V_{SS} versus frequency. Figure 15 is the MC CMRR versus frequency, which indicates typical CMRR $\approx -120dB$. Figure 16 is the typical $Vo_{Noise} = 680nV/\sqrt{Hz}$ versus frequency at 1kHz , which is based on very preliminary noise models. Figure 17 is the WC $t_{start-up} \leq 20\mu s$ with V_{DD} pulsed to 2V from 0 (and $V_{in} = 1/2V_{DD}$ in unity gain configuration).

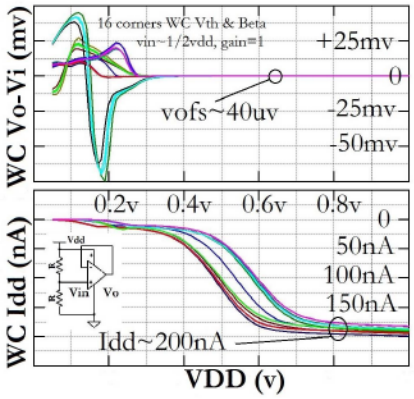

Fig. 2. Min' V_{DD} vs. I_{DD} & V_{OFS}(WC)

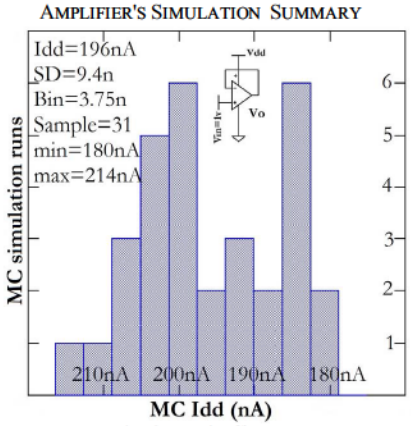

Fig. 3. I_{DD} (MC)

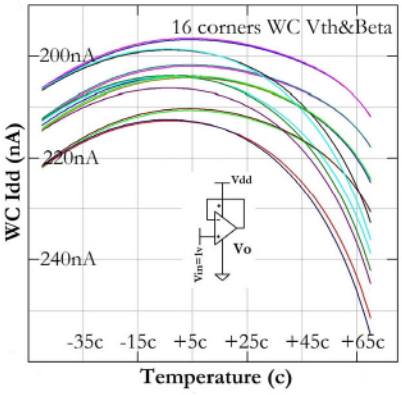

Fig. 4. I_{DD} vs. T (WC)

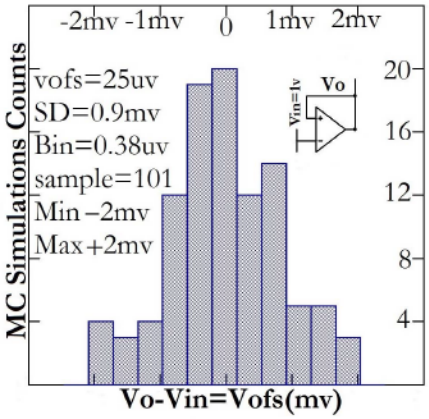

Fig. 5. Input V_{OFS} (MC)

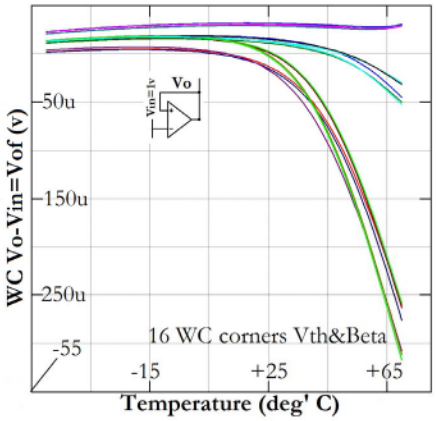

Fig. 6. V_{OFS} vs. T(WC)

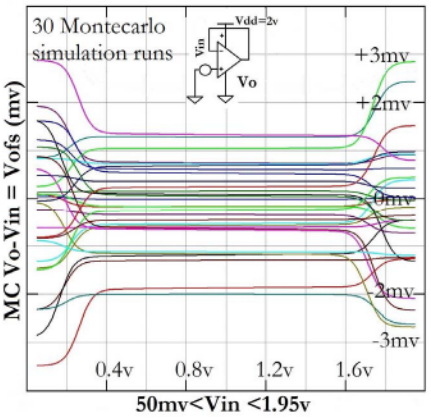

Fig. 7. V_{OFS} vs. V_{IN} (MC)V_{DD}@2v

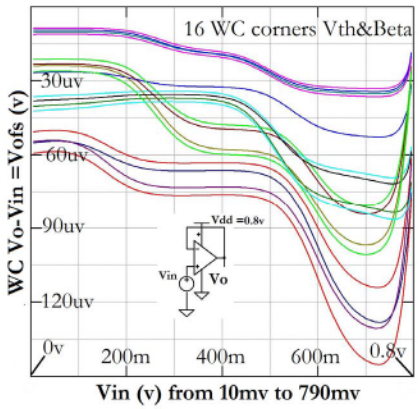

Fig. 8. V_{OFS} vs. V_{IN} (WC)V_{DD}=0.8v

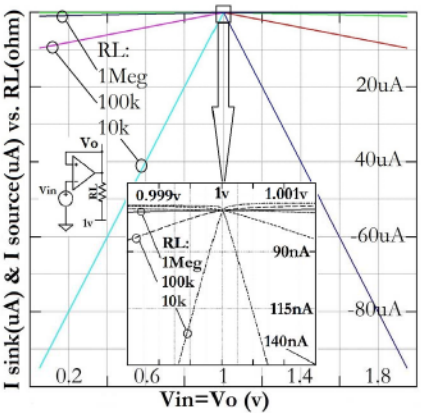

Fig. 9. V_{IN} vs. R_L ($I_{SINK-SOURCE}$)

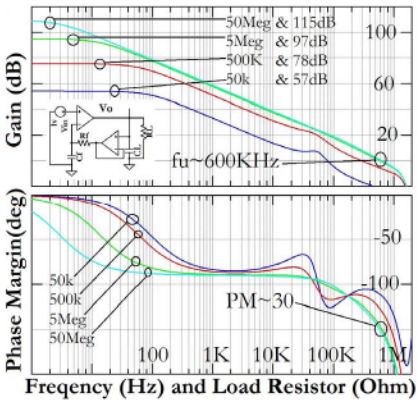

Fig. 10. Gain & Phase vs. vs. F vs. R_L

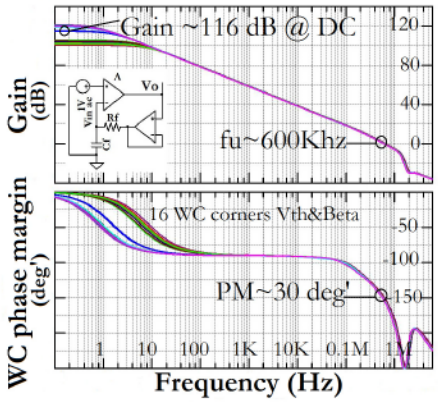

Fig. 11. Gain & Phase vs. F(WC)

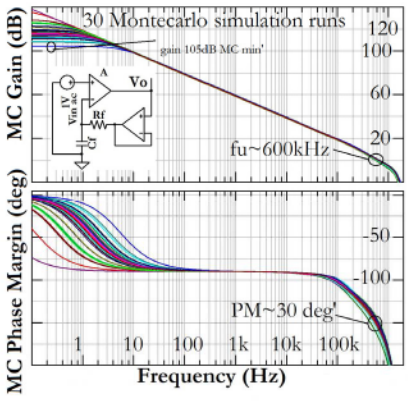

Fig. 12. Gain & Phase vs. F(MC)

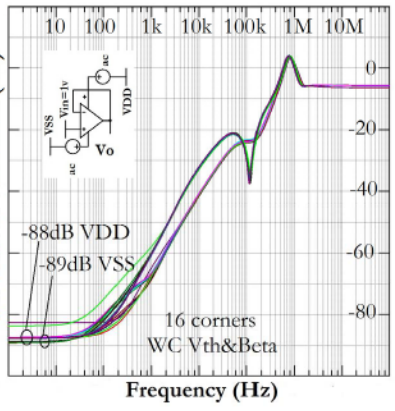

Fig. 13. $PSRR_{VDD/VSS}$ vs. F(WC)

AMPLIFIER'S SIMULATION SUMMARY CONTINUED & ROUGH AMPLIFIER LAYOUT

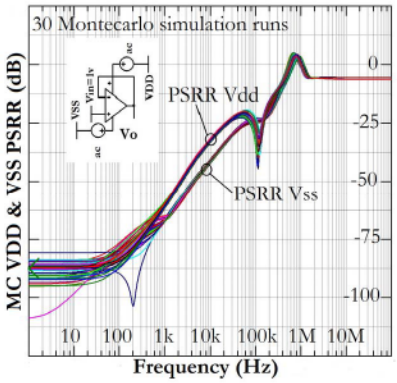

Fig. 14. $PSRR_{VDD/SS}$ vs. F(MC)

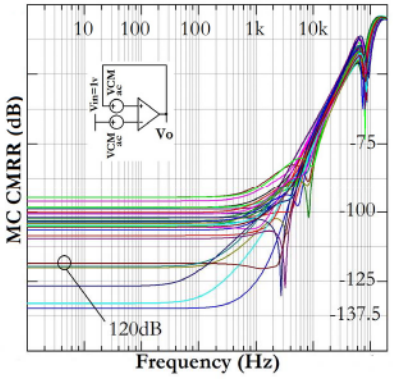

Fig. 15. CMRR vs. F(MC)

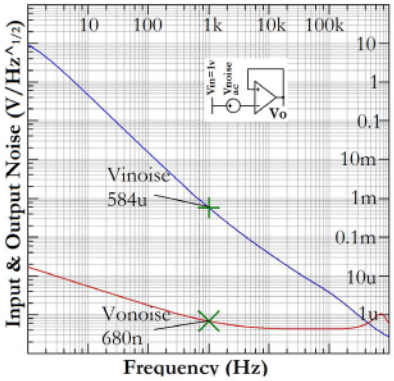

Fig. 16. Noise vs. F

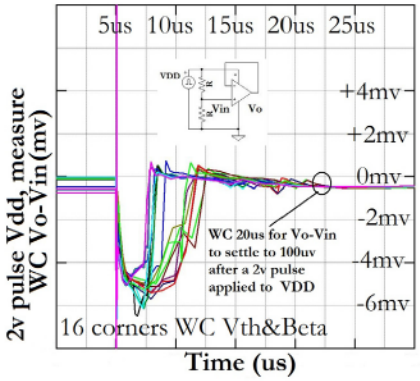

Fig. 17. start-up V_{DD} = 0↑2v (WC)

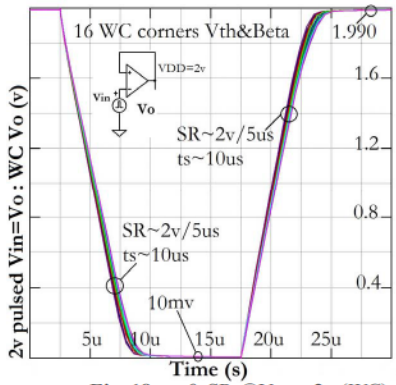

Fig. 18. τ_s & SR @V_{DD} = 2v (WC)

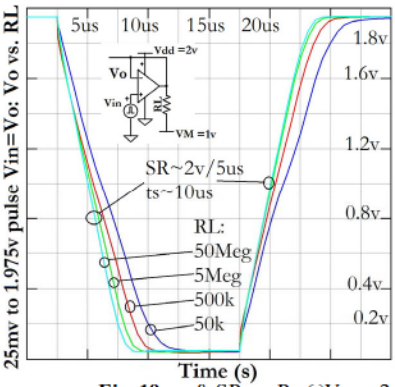

Fig. 19. τ_s & SR vs. R_L @V_{DD} = 2v

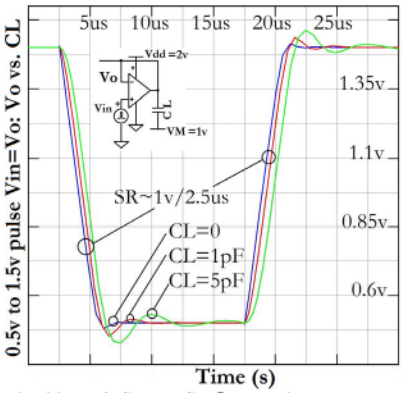

Fig. 20. τ_s & SR vs. C_L @V_{DD} = 2v

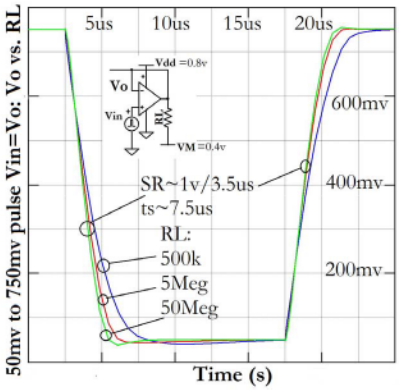

Fig. 21. τ_s & SR vs. R_L @V_{DD} = 0.8v

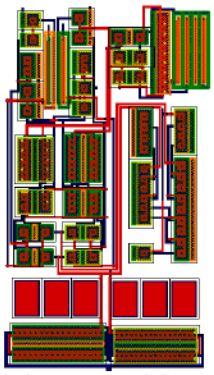

Fig. 22. Preliminary Layout (~80µm×120µm)

Figure 18 is the WC transient response (TR) for $V_{in} = V_O$ stepped to 1.99v from 10mv, indicating SR ~2V/5µS and τ_s ~ 10 µS. Figure 21 is the TR vs R_L for V_{DD} = 0.8v $V_{in} = V_O$ stepped to 750mv from 50mv, for R_L = 500KΩ, 5MΩ, and 50MΩ. Fig. 22 is preliminary layout rough area $(\sim 100\mu m)^2$.

V. SPECIFICATIONS RISK FROM CIRCUIT SIMULATION TO FABRICATION

The V_{OFS} mismatch in PMOS and NMOS input pairs will show up as distortion. Operating the output FET currents at ultra-low levels degrades amplifier's distortion performance. Substrate currents, FET parasitic leakages, and FET mismatches will undermine PSRR and CMRR performance, which is not captured in simulations adequately. Noise will be high at ultra low operating currents. The amplifier is not fit to drive capacitive loads. Leakages will double every 10°C and, as such, DC and AC performance will be degraded at hot. Small size FETs leak less, but noise and mismatch will be higher in smaller FETs. The smallest W/L are set at 3 times bigger than process minimum geometry to balance noise-offset-leakage performance. Offset voltage TC drift simulations are doubtful since model don't capture $\Delta V_{OFS}/\Delta T$ properly. Extra capacitors are placed in layout as back-up for amplifier's stability. Low noise, low distortion, operating at high temperature, and ability to drive capacitive loads are not within the scope of this work.

VI. Summary & Conclusion

An ultra low power near rail-to-rail input output buffer amplifier is presented with the following contributions: First, the buffer stage can work at low V_{DD}, while operating chiefly in current mode which makes it fast. Buffer deriver utilizes complementary non-inverting current mirrors that monitor and rectify sink-source output currents, whose outputs feed a loser take all circuit that selects the smallest of the sink or source currents. The output of loser take all circuit are fed onto a current mirror amplifier that regulates, in concert with the main amplifier, the minimum operating current in the inactive output sink-source FETs. Second, a circuit emulating the function of a floating current source, that bias the folded cascode amplifier's current mirror network, also works at low V_{DD} which helps improve amplifier's offset. The floating current source equalizes the upper PMOSFET (P_5-P_6) and lower NMOSFET (N_6-N_5) cascoded current mirrors. With the drain terminal of N_6 feeding the source of P_6 and drain of P_6 feeding source of N_6, the gate to source voltages of P_6 and N_6 are held constant by regulating the currents in N_5 and P_5. As such, N_5 and P_5 currents, that bias the currents in the FCTA gain stage, are substantially equalized since they each carry the sum of currents flowing in N_2 and P_2.

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