2017 IEEE International Autumn Meeting on Power, Electronics and Computing (ROPEC 2017). Ixtapa, Mexico

Low Noise Rail-To-Rail Amplifier Runs Fast At Ultra Low Currents And Targets Energy Harvesting

Ali Far
ali.t.far@ieee.org

Abstract — **An input-output rail-to-rail buffer amplifier is presented that is low noise, fast, and operates at ultra low currents. The amplifier targets energy harvesting applications that require low cost, high volume, and rugged manufacturing by avoiding use of non-standard device configurations or special processes. The main contributions of this work are: (1) The method of lowering voltage output noise by narrow-banding an amplifier, while introducing a time dependent bias current boost that is triggered by large differential input signals. Narrow-banding an amplifier to reduce its output noise, slows its dynamic response, and this method aims to restore and boost both the amplifier's slew rate and settling time. (2) Amplifier can operate at low V_{DD} of about V_{GS}+2V_{DS}, while running in subthreshold, based in standard 0.18u digital CMOS. (3) PMOSFETs are utilized as inputs, compensation capacitors, and bias resistors in both the amplifier and the boost stages, which helps optimize for yield and lower noise. More importantly, the dynamic response of both the main amplifier and the boost stage being substantially dependent on PMOSFET device parameters, facilitates a smoother dynamic response in and out of boost, over process and operating variations. Based on montecarlo (MC) and worst case (WC) simulations, the following specifications are achievable: voltage output noise (VO_{NOISE}) of 10 uv/Hz^1/2 at 1KHz, supply current (I_{DD}) ~ 500 nA; V_{DD} minimum ~0.6V; rail-to-rail voltage input (V_{IN}) range and output voltage (V_{OUT}) range of ~ +/- 25mv from the rails; output resistor load (R_L) ~2k Ohms; output capacitor load (C_L) ~1nF; slew-rate (SR) -/+ ~ 4/2.5 v/us; settling time (t_S) ~ 5us to 1%; power supply rejection ratio (PSRR) -/+ ~ 80dB/85dB, common mode rejection ration (CMRR) ~ 125dB, unity gain bandwidth (f_U) ~ 20KHz with phase margin (PM) ~ 75 degrees; open loop gain (G) ~ 85dB; preliminary area estimate of ~ 180 um per side.**

Keywords— **low noise, fast, batteryless, ultra low current, amplifier, class AB, buffer amplifier, minimum current selector, resistorless, subthreshold, loser take all, slew rate boost, rail to rail, high speed, WSN, self powered IC, RFID, adaptive biasing, internet of things, smart dust, IoT, energy harvesting, wearable electronics, sensor array, wireless sensor network, FCTA, FCS, smart sensor array, low power, low power supply, dynamic biasing, resistorless, power aware, current boost, current mode, CGA, CSA, current inverter.**

I. Introduction

Amplifiers are core building blocks in integrated circuits (IC), and one of their most important categories are class AB amplifiers which are broadly covered in prior art [1]-[7][14].

Readers can also refer to prior art for use of adaptive biasing or slew rate enhancements in amplifiers, generally with the objective of keeping the static power consumption low but increasing the amplifier's slew rates by means of dynamically raising the bias current when the amplifier's inputs experience large signals [8]-[12][14].

TABLE I: Amplifier Typical Specification & Comparison

Typical Specs	[13]	[12]	[11]	[2]	This work	
	Sim'	SiO_2	Sim'	Sim'	Sim'	Figure
CMOS (μm)	0.18	0.18	0.18	0.18	0.18	
Area (μm^2)	np	62^2	np	120^2	~180^2	2
$Vo_{noise\ 1KHz}$ ($\mu V/\sqrt{Hz}$)	np	np	np	1400	10	9
V_{DD} min (V)	1.8	np	0.6	0.6	0.6	3
I_{DD} (nA)	8E5	325	1E3	330	500	4,3
ΔVi_{RAILS}(mV)	±200	np	0	0	0	6,7,13
ΔVo_{RAILS}(mV)	±200	np	±28	±25	±25	15,16
V_{OS} (mV)	np	np	np	±3	±5	5,6,3
I_{DRIVE} (mA)	np	np	np	±0.2	±0.5	7
R_{L-min} (Ω)	np	np	np	5K	2K	7
C_{L-max} (pF)	2	10	np	5	1000	9,15,16
A_V (db)	53	60	51	78	85	8,9
f_U (MHz)	300	0.01	0.04	1	0.02	8,9
φ_M (°)	81	90	65	40	75	8,9
$PSRR_+/-$(dB	np	np	np	83/91	85/80	11
$CMRR_{DC}$ (db)	np	np	65	98	125	10
SR_-(v/μS)	1280	0.5	0.12	2	4	13,15,16
SR_+(v/μS)	1280	0.6	0.12	2	2.5	13,15,16
$\tau_{S+/-}$ (μs)	6ns	np	np	3	5	14,15,16

Next generation energy harvesting, and wireless batteryless electronics are emerging applications, that require ultra low power. All else equal, operating analog ICs at ultra low currents present some challenges such as high noise, slow dynamic response, and limited temperature spans. Moreover, subjecting an amplifier to low V_{DD}, limits its DC input-output span, and may require more expensive fabrication or special devices, such as depletion FETs, to free up the needed head-room to meet the required signal to noise ratios. The objective of this work is to present a method to solve most of the aforementioned challenges using low cost, rugged, and abundantly available standard digital CMOS manufacturing that also accommodates ease of process node portability.

II. Contributions of the Proposed Design

The contribution of this ultra low power amplifier is a method (patent pending) of suppressing Vo_{NOISE} by narrow-banding an amplifier, while independently reinvigorating the amplifier's narrow-banded dynamic response via boosting both its' slew rate and settling time, and here is how. PMOSFET capacitors are coupled to the high impedance node of an amplifier's gain stage to low pass filter its Vo_{NOISE}. Concurrently, a boost function can be triggered when the amplifier is subjected to large differential input signal. As

978-1-5386-0819-7/17/$31.00 ©2017 IEEE

such, by rapidly injecting a time dependant current into the amplifiers bias network, the amplifier's slew rate is boosted. When inputs approach balance (coarse equalization), a boost signal is triggered off. But here, instead of shutting down the boost current rapidly, a slow decaying current continues feeding the amplifier's bias, until it fades off. This boost-off phase accompanied with a decaying current (which is initially sizable enough when compared to the otherwise statically ultra low current operant in the un-boosted mode, and) roughly follows a single pole trajectory that helps boost the amplifier's settling time. It goes without saying that the whole amplifier operates in the subthreshold region when it is un-boosted, but its' input, transconductance gain, and output buffer stages transition in and out of saturation during the intermittent boosted states. It is also of note that PMOSFETs are used at inputs, and also as active resistors to set the bias currents for both the amplifier and the boost input stages, which establishes both their input's transconductance (gm_{PMOS}). Moreover, PMOSFET's capacitance are employed to set the dominant poles of both the amplifier and boost stages. Hence, the dynamic response of the amplifier and the boost stage track each other, over operating, and process variations, and therefore follow a reasonably smooth and stable passage, in and out of boost.

III. Amplifier's Bias, Input, and Output Stages

Here is a brief description summary of the proposed buffer amplifier (patent pending) with the simplified circuit schematic illustrated in Fig. 1 [1-2][4-5]:

In the bias stage, a PMOSFET's differential gate-to-source voltage, $\Delta Vgs_{Mb3-4} \approx \eta_{PMOS} \times V_T \ln(b)$, is placed across an active PMOSFET resistor M_{b1} (in triode). Hence, the bias current is mostly independent of V_{TH} and chiefly a function of V_T and μ_{PMOS}. This trait helps with yield and specification's stability of the amplifier over manufacturing process and temperature variations [13-14].

In the input stage, the primary inputs composed of PMOSFETs $M_{i1}, M_{i2} - M_{i3}$ receive their tail current via M_{i19}, but run out of head-room when the common mode input voltage approaches V_{DD}. When V_{IN} nears V_{DD}, M_{b20} clamps the source terminals of $M_{i1}, M_{i2} - M_{i3}$ and steers their tail currents away and onto $M_{i7}, M_{i8} - M_{i6}$ via M_{i20}. Here, the amplifier's secondary input PMOSFET pair $M_{i7}, M_{i8} - M_{i6}$ take over the input operations, after being level shifted down via NMOSFET source followers $M_{i4} - M_{i6}$. As such, the input's gm_{PMOS} ($\approx i_b/(\eta_{PMOS} \times V_T$ with subthreshold slope factor $1.5<\eta_{PMOS}<2$) is held fairly constant for keeping the same tail current while inputs traverse rail-to-rail [1-2][4-5]. Please see [14] for mathematical formulations (DC, AC, noise, transient) of folded cascode amplifiers that is utilized here. At

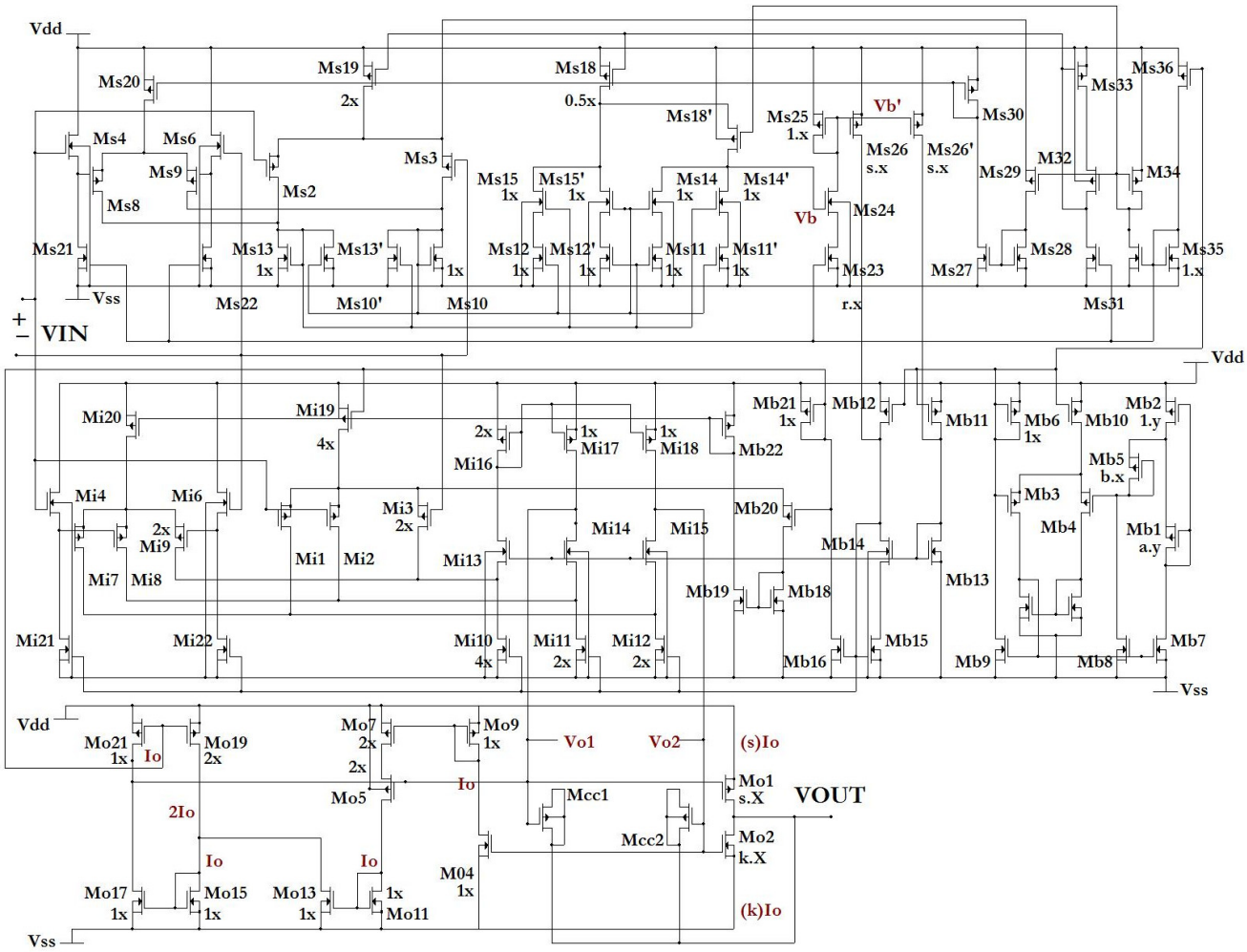

Figure 1. Proposed Amplifier (patent pending)

the gain nodes of the amplifier, V_{o1} and V_{o2}, the high impedance is roughly a function of $\sim V_A/ i_b$. Moreover, large size PMOSFET capacitors M_{cc1} and M_{cc2} ($\gg M_{o1}, M_{o2}$) set the dominant poles and band-pass V_{o1} and V_{o2}, and thereby filter out the amplifier Vo_{noise}. For example, comparative simulations depicted in Fig. 12. indicate Vo_{noise} improvements to ~10 $\mu V/\sqrt{Hz}$ with the band passing and the boost functions compared to ~700 $\mu V/\sqrt{Hz}$ at 1KHz without them.

The bottom section of Fig. 1 is the amplifier's output stage [2][7-8]. It is composed of minimum current selectors (MCSs: $M_{o4} - M_{o9} - M_{o5} - M_{o7}$), and inverting current mirrors (ICM) that is part of the current feedback amplifiers (CFA_N composed of ICM_N $M_{o11} - M_{o13} - M_{o15} - M_{o17}$ plus current sources $M_{o19} - M_{o21}$). The MCSs track the currents in output driver FETs , $M_{o1} - M_{o2}$, which are scaled and mirrored into the CFAs. The MCS tracks the sink-source output FET currents, and regulates the minimum operating current in the inactive sink-source output FET, and it operates with low $V_{DD} \geq V_{GS} + 2V_{DS}$. The output stage, chiefly operates in current mode, and as such it has a high bandwidth. Thus, filtering out the noise in the high impedance gain stage of the amplifier that drives the output stage, can be optimized without being hindered by the output stage dynamic response.

IV. Boost Stage

The input stage of the boost and the amplifier circuits are largely identical, consisting of the PMOSFET primary pair (M_{s2}-M_{s3}) that handles $V_{SS} \leq V_{IN} \leq V_P$, where at $V_{IN} = V_P$ the M_{s2}-M_{s3}, and M_{s19} run out of head-room [1-12]. At $V_{IN} \geq V_p$, M_{s29} clamps the source terminal of M_{s2} and steers M_{s19}'s current via M_{s28}, M_{s27}, and M_{s30} onto the current source, M_{s20}, which biases the boost stage's secondary input pair. For $V_p \leq V_{IN}$, the DC level shift of NMOSFET source-followers (M_{s4}-M_{s6}) provides the secondary PMOSFET pair (M_{s9}-M_{s8}) and its current source M_{s20} with the needed operating headroom.

Let's take the case $V_{SS} \leq V_{IN} \leq V_P$ when the secondary input path is off. First, when the amplifier's inputs are in steady-state then the boost signal remains off. Here, the $I_{Ms2} \approx I_{Ms3} \approx I_{Ms10} \approx I_{Ms13} \approx i_b$. In this state, for the MCSs M_{s12}-M_{s15}, $M_{s12'}$-$M_{s15'}$, M_{s11}-M_{s14}, and $M_{s11'}$-$M_{s14'}$ we get $I_{Ms12} \approx I_{Ms15'} \approx I_{Ms14} \approx I_{Ms11'} \approx I_{Ms10} \approx i_b$. Similarly, $I_{Ms15} \approx I_{Ms12'} \approx I_{Ms11} \approx I_{Ms14'} \approx I_{Ms13} \approx i_b$. Please note that, for example, M_{s10} and M_{s13} (with W/L=1x each operating at i_b) are mirrored into the MCS composed of series association of M_{s12}-M_{s15} (with W/L=1x), and hence $I_{Ms12} = I_{Ms15} \approx i_b/2$. Boost stage can function without MCSs $M_{s12'}$ - $M_{s15'}$ and $M_{s11'}$ - $M_{s14'}$, which are added to help balance transients, and injection cancelations. When the amplifiers' inputs are near small signal balance, the $\min(I_{Ms12}, I_{Ms15}) \approx \min(I_{Ms12'}, I_{Ms15'}) \approx \min(I_{Ms11}, I_{Ms14}) \approx \min(I_{Ms11'}, I_{Ms14'}) \approx i_b/2$. Accordingly, $I_{Ms18} \approx i_b$ is used up by $\min(I_{Ms12}, I_{Ms15}) + \min(I_{Ms12'}, I_{Ms15'}) \approx i_b$, which causes $M_{s18'}$ to starve. With $I_{Ms18'} \approx 0$ and $\min(I_{Ms11}, I_{Ms14}) + \min(I_{Ms11'}, I_{Ms14'}) \approx i_b$, the node V_b is pulled down. Therefore, M_{s24} is shut off, which blocks the currents through M_{s23}, M_{s25}, M_{s26}, and $M_{s26'}$ off as well. Here, the amplifier's bias current supplied by M_{s11}, and M_{s12} remains un-boosted.

Second, with $V_{SS} \leq V_{IN} \leq V_P$, when large differential signal transients are applied at the inputs, then all of M_{s19} current $2i_b$ would flow through M_{s3}. Consequently, I_{Ms2}, I_{Ms13}, I_{Ms15}, $I_{Ms12'}$, I_{Ms11}, and $I_{Ms14'}$ run near or at zero nano-amperes and $\ll I_{Ms3}$, I_{Ms10}, I_{Ms12}, $I_{Ms15'}$, I_{Ms14}, and $I_{Ms11'}$ Therefore, $0 \approx \min(I_{Ms12}, I_{Ms15}) \approx I_{Ms15} \approx \min(I_{Ms12'}, I_{Ms15'}) \approx I_{Ms12'} \approx \min(I_{Ms11}, I_{Ms14}) \approx I_{Ms11} \approx \min(I_{Ms11'}, I_{Ms14'}) \approx I_{Ms14'} \ll 2i_b$. Here, MCSs conduct near or at zero currents, and thus all of M_{s18} current i_b passes onto $M_{s18'}$, which pulls the node V_b up (the boost-on signal). Therefore, M_{s24} turns on allowing $I_{Ms23} \approx r \times i_b$ to add its boost current onto M_{s25}, which is mirrored and scaled up onto M_{s26}, and $M_{s26'}$. Note that here, the dynamic current's peak $I_{Ms26} \approx I_{Ms26'} \approx s \times r \times i_b$, which is summed with the amplifier's (static) bias current network via M_{b11}, and M_{b12}. Initially, when the boost signal is triggered on, $I_{Ms23} \approx r \times i_b \approx I_{Ms25}$ slews the node $V_{b'}$. This node has a time constant set roughly by the equivalent capacitance dominated by C_{Ms26} and $C_{Ms26'}$ and the impedance $1/g_m$ of M_{s25}, in saturation region, in light of the transitions from subthreshold to saturation region in the intermittent boosted state. Comparative simulations in Fig 13. depicts improvement in the amplifier positive SR to 2.5v/µs from 0.007 v/µs, and negative SR to 4 v/µs from 0.009 v/µs, with the boost function enabled versus without, respectively.

As the amplifier loop begins regulating and inputs nearly equalize (coarse balance), then the boost off signal is triggered, and M_{s24} cuts off M_{s23} current from the $V_{b'}$ node. As such, $I_{Ms25} - I_{Ms26} - I_{Ms26'}$ current start their slow decay towards zero with a transient current profile that approximates a single pole trajectory, while this decaying transient current is still being injected into the amplifier operating bias current network. As just noted, although the capacitance at $V_{b'}$ node is dominated by equivalence of $C_{Ms26}+C_{Ms26'}$, but $V_{b'}$ node's $1/gm$ (impedance) increases with time as I_{Ms25} current fades off while M_{s25} makes its transitions from operating in the saturation region to subthreshold. As stated before, initially in boost off mode, I_{Ms25} is sizable enough, compared with the amplifier's un-boosted static current, to help speed up the amplifier's τ_s. For example, simulations depicted in Fig. 17 shows $\tau_s \sim 5\mu s$ compared to ~15 µs, with the boost function enabled versus without, respectively.

In summary, the benefits of the proposed circuit are: First, lower noise, and most other attributes of the amplifier including its gain, bandwidth, static power consumption, common mode range, PSRR, and CMRR are generally not

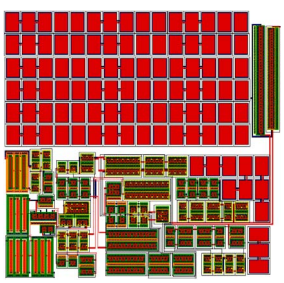

Fig. 2. Preliminary layout and rough die area ~ $180\mu m^2$

AMPLIFIER'S MC & WC SIMULATIONS SUMMARY

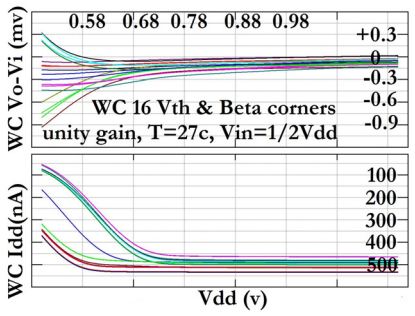

Fig.3. V_{OFS} vs. I_{DD} vs V_{DD} (WC)

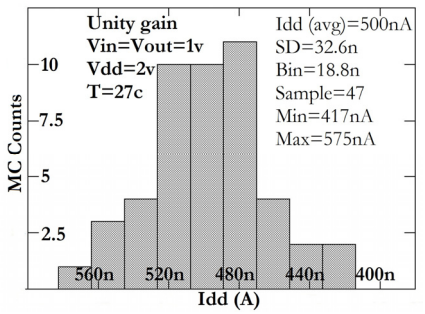

Fig. 4. I_{DD} (MC)

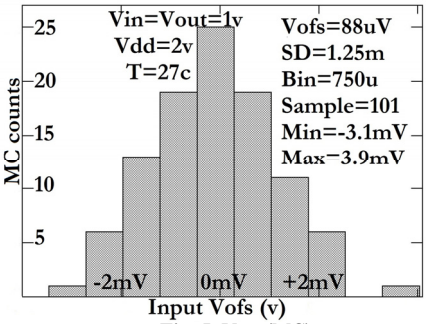

Fig. 5. V_{OFS} (MC)

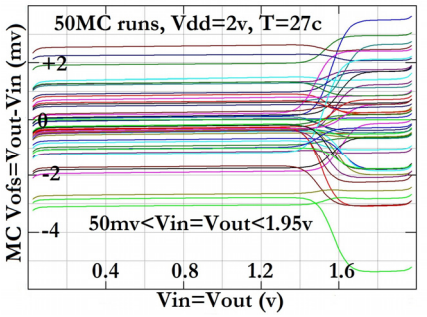

Fig. 6. V_{OFS} vs. V_{IN} (MC)

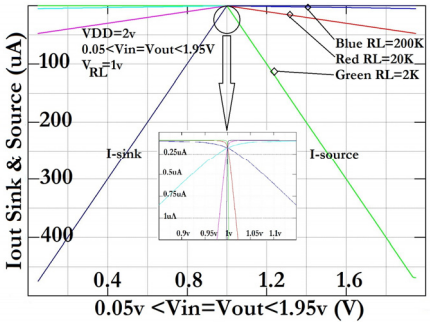

Fig. 7.V_{IN} vs. R_L (I_{SINK} & I_{SOURCE})

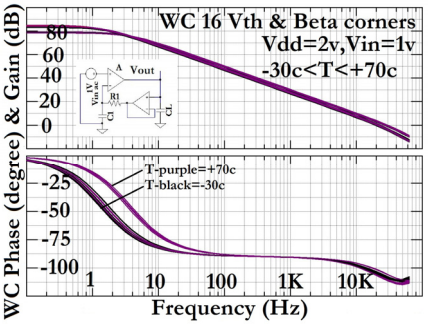

Fig. 8. Gain/Phase vs. Freq. vs. Temp. (WC)

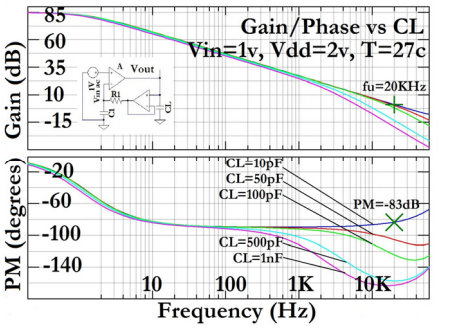

Fig. 9. Gain/Phase vs. Freq. vs. C_L (WC)

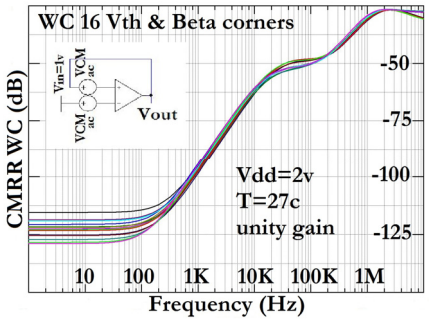

Fig. 10. CMRR vs. Freq. (WC)

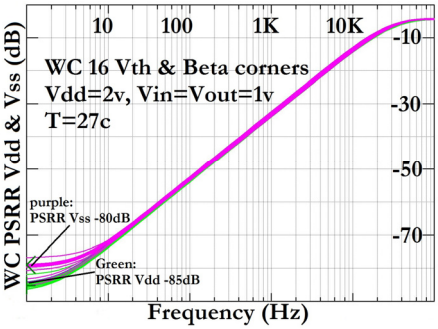

Fig. 11 PSRR vs. Freq. (WC)

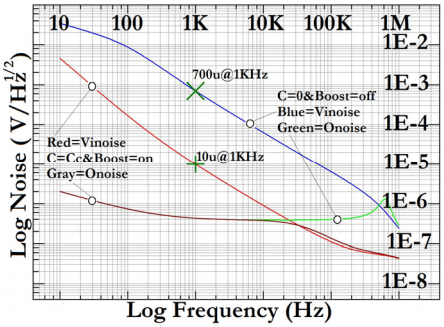

Fig. 12. Noise vs. Freq. with & w/o boost

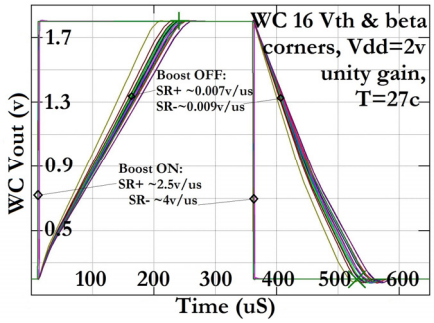

Fig. 13. SR with & w/o boost (WC)

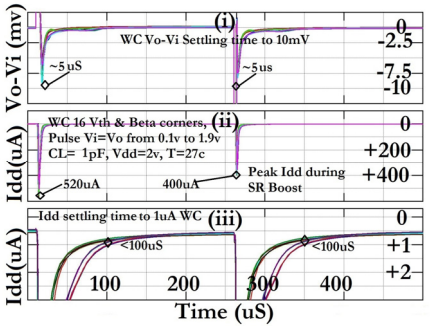

Fig. 14. V_{OUT} & I_{DD} vs. Large Signal Vin (WC)

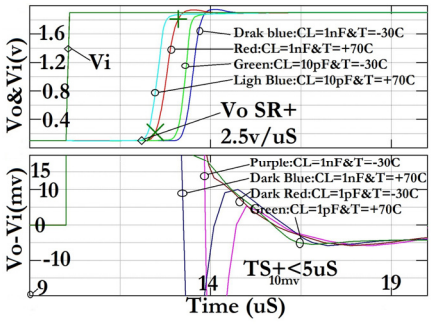

Fig. 15. V_{OUT}/I_{DD} SR+ and τ_{S+} vs. C_L vs. Temp (WC)

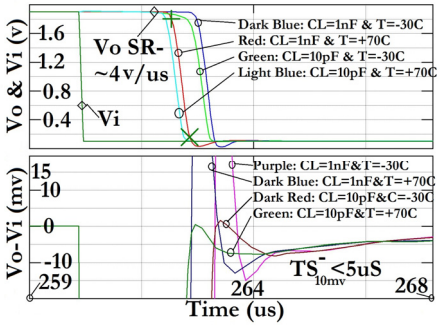

Fig. 16. V_{OUT}/I_{DD} SR- and τ_{S-} vs. C_L vs. Temp (WC)

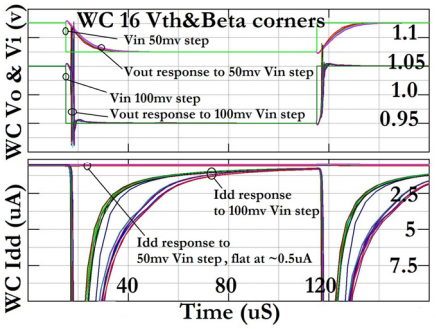

Fig. 17. V_{OUT} & I_{DD} vs. Small Signal Vin (WC)

inputs experience large differential signals. Second, amplifier's input structure and that of the boost stage are substantially similar, and hence the boosting function accommodates the full common mode range and power supply span. Third, the maximum boost current, $s \times r \times i_b$, is fixed and is proportional to amplifier's static bias current, i_b , which helps control peak dynamic current consumption. This trait also facilitates the boost stage's peak speed to tracks that of the main amplifier, over process and operating variations. Such is the case, in part because i_b is independent of V_{TH} and mostly a function of V_T and μ_{PMOS} which are more tightly controlled in manufacturing. Fourth, as noted earlier, the AC, slew rate, and transient profiles of the main amplifier and that of the boost circuit should approximately track each other over operating and process variations. This is because generally, the amplifier and the boost stage's operating currents, gain ($\propto(V_A/V_T)^2$), and input's $1/g_m$ ($\propto \eta_{PMOS}.V_T/i_b$) track each other, as do their poles at the high impedance node of the amplifier that are roughly a function of $r_o \approx V_A/i_b$ and $C_{PMOSFET}$. Fifth, care is taken to minimize dependence of amplifier's specifications on multiple device parameters such as NMOSFET, $V_{THN/P}$, and N+/P+ resistors. Instead, amplifier's specifications mostly rely on PMOSFETs which dominate pertinent signal paths, and this can help optimize yield and help lower noise (e.g., PMOSFET 1/f noise ≪ NMOSFET 1/f noise) further. Sixth, the switching threshold of the amplifier's input stage from small signal to large signal needs to be large enough (e.g., offset mismatch between the boost and the amplifier input stages, ΔV_{OFS}) so that a false or premature turning on of the boost function is avoided. This is the case considering, the amplifier and boost stage input's $1/gm_{PMOS}$ where $i_b \approx 10s$ of nano-amperes. Moreover, inclusion of $M_{s13'}$ and $M_{s10'}$ (less than 10% of W/L M_{s13} and M_{s10}) at boost's input stage, provide some hysteresis as gaurd-band against unwanted boost signal toggles for cases when input pulses become equivalent to boosted slew rate.

V. Summary of Monte Carlo & Worst Case Simulations:

MOSIS/TSMC BSIM3v3.1 equivalent models for 0.18μm CMOS are used for WC and MC simulations. Please see Fig. 2. which is a rough amplifier layout placement. Table I is a summary of specifications and comparisons with prior art. Simulation's conditions are $V_{DD} = 2v$, T=27℃, with amplifier set up in unity gain, unless otherwise specified on the plots. Figure 3 is WC for minimum $V_{DD} =$ ~0.6V validated by ramping V_{DD}while tracking V_{OFS} vs. I_{DD}. Figure 4 is I_{DD} MC simulation profile indicating a $\pm$16% variation band, which is proportional to amplifier's input's $1/g_m$ and its AC response variations. Figure 5 is V_{OFS}'s MC simulation of ~ $\pm$ 3.5mV. Figure 6 is MC simulation for V_{IN} vs. V_{OFS} indicates the ΔV_{OFS} between the primary PMOS and the secondary NMOS+PMOS FET inputs. Figure 7 is typical simulation showing R_{LOAD} vs. V_{IN} vs. output driver currents, $I_{Mo2} = I_{SINK}$ and $I_{Mo1} = I_{SOURCE}$. This graph shows that when I_{Mo2} is in non-sink mode or when I_{Mo1} is in non-source mode, then their currents are regulated at ~100nA. Figure 8 is WC for AC response depicting gain (typ. A_V ~ 85db) vs. phase (typ. φ ~ 75∘) vs. Frequency (typ. (f_U ~ 20KHz) vs temperature ($-30℃<T<+70℃$), where $C_{LOAD} = 50pF$. Figure 9 is the amplifier's typical AC response as a function of $10pF < C_{LOAD} < 1nF$. Figure 10 is WC for CMRR (typ. ~ -125dB at DC) vs. Frequency. Figure 11 is WC for $PSRR_{VDD}$ (typ. ~ -85dB at DC) and $PSRR_{VSS}$ (typ. ~ -80db at DC) vs. frequency. Figure 12 is the noise vs. frequency simulations, which indicates Vo_{noise} of ~10μV/$\sqrt{Hz}$ at 1KHz with the narrow-banding capacitor and boost stage, vs. ~700μV/$\sqrt{Hz}$ at 1KHz without them (based on very preliminary noise models). Figure 13 is WC for large signal (LS) transient response (TR) for V_{OUT} vs. time, which shows a 360× to 440× increase in SR, with the boost stage as compared to without it. Figure 14(i) shows WC LS τ_S ~ 5μs to 10mv. Figure 14(ii) is WC I_{DD} spiking to ~520μA during 'boost on' mode. Figure 14(iii) shows WC 'boost off' mode, when I_{DD} decays to its static level of ~500nA in less than 100μs. Figures 15 and 16 show typical large signal (V_{IN} pulsed between 0.1v and 1.9v) transient response vs. $10pF < C_{LOAD} < 1nF$ vs. $-30℃ < T < +70℃$. Here τ_S, ~ 5μs and SR_+ ~ 2.5v/μs and SR_- ~ 4v/μs. Figure 17 is WC (unity gain) superimposed transient response for both the small signal (50mv pulsed V_{IN}) and LS (100mv pulsed V_{IN}). The LS side shows that boost function is enabled in response to a 100mv pulsed V_{IN}, when I_{DD} initially spikes to multiples of μA followed by 'boost off' mode decay current. As noted earlier, instead of shutting the boost current fast, this 'boost off' decaying current that feeds the amplifier's bias current, enhances the amplifier's τ_S. However, the small signal side shows that when boost function remains off, and I_{DD} remains under 500nA, then τ_S ~ 15μs to 5mv in response to V_{IN} pulsed 50mv.

VI. Specifications Risk From Circuit Simulation to Fabrication

Simulations are useful here for comparing Vo_{noise} performance with or without the proposed noise reduction method, but the absolute value of Vo_{noise}'s simulation results are not accurate because the noise models are very preliminary. The ΔV_{OFS}, between the amplifier's primary PMOSFET and secondary NMOSFET plus PMOSFET inputs, will materialize as distortion. Additionally, distortion will be elevated when the output stage has ultra low quiescent currents I_Q with large C_L and wide VIN_{P-P} swings, roughly governed by $I_Q/C_L \approx \omega \times V_{P-P}$, where the lowest distortion at the highest frequency is ω, in boost off phase. FET leakages doubles per $\Delta T \approx +10℃$, which derailed hot temperatures performance of ultra low current circuits . Low distortion and high-temperature performance are beyond the scope of this work. However, given most target energy harvesting applications experience (non-sinusoidal) impulse signals, low distortion is not required. Also, one sized and donut shaped FETs at 5 times the minimum size are used as a compromise between big FETs with more area to leakage, and small ones with more mismatch and noise. While MC simulations can capture the ΔV_{OFS} between the amplifier input stage and boost stage, SPICE

models do not capture $\Delta V_{OFS}/\Delta T$ accurately. The V_{OFS}, ΔV_{OFS}, and $\Delta V_{OFS}/\Delta T$ are components of the boost function's switching threshold. First prototypes use passive (instead of MOS) capacitors to band-pass noise for conservatism.

As shown in Fig. 18, the settling time of the proposed amplifier can be higher (e.g., $\tau_S = 15\mu s$) for a small signal (e.g., V_{IN} pulsed 50mv) pulse when boost function is not engaged. Therefore, it is foreseeable that in silicon, a temperature change of a few ℃ could shift ΔV_{OFS} a few millivolts, which can cause τ_S and (transient) I_{DD} to change from 5µs and 14µA, respectively, to 15µs and 0.5µA. As mentioned earlier, the hysteresis ($M_{s13'}$ and $M_{s10'}$) in the boost's input stage is added to guard against unwelcomed toggles between boost on and off states for conditions near the boost stage switching threshold. PMOSFET capacitors are non-linear and have voltage dependence. Hence, poly-metal capacitors are provided in layout as metal mask option for back-up in both the amplifier and boost stage for compensation guard band. Dummy PMOSFET and NMOSFET capacitors are also added in layout to gaurd-band for the capacitive loading of output driver FETs M_{01}, M_{02} and their influence on the tracking of the dynamic responses between the amplifier and boost stages. Excessively high PSRR and CMRR may be unattainable in silicon due FET mismatches and parasitic leakages. A power-on-rest is included although simulations show that leakages in bias section help self-start up by lifting M_{b7}, M_{b8}, and M_{b9}.

VII. Summary & Conclusion

To decouple noise performance from amplifier's speed, a method is presented which is to low pass filter an amplifier's output noise while boosting both its slew rate and the settling time. The amplifier's output stage is chiefly current mode, by utilizing minimum current selector and a current mirror inverter amplifiers, which makes it fast. Thus, the main amplifier folded cascode high gain node dominates and substantially low pass filter the output noise, without the output stage interfering. Concurrently, when large differential signals are detected at the narrow-banded amplifier's input, a boost function kicks in and speeds up both the slew rate and steeling time of the amplifier. The time dependency in the boost stage and amplifier's gain stage are chiefly a function of 1/gm and Cg of PMOSFETs. This trait helps with consistency of amplifier's dynamic response in and out of the boost over process and operating variations. As a result, a low output noise, rail-to-rail input-output, ~500nA amplifier, that can operate at V_{DD}~ 600mV is presented that has a gain of ~85db, PSRR of ~80dB, and CMRR of ~140dB, with + & - slew rate of ~2.5 & ~5V/us, and settling time of ~5µs. It can drive a ~2KΩ and ~1nF load.

References

[1] A. Far, "Small size class AB amplifier for energy harvesting with ultra low power, high gain, and high CMRR," *2016 IEEE International Autumn Meeting on Power, Electronics and Computing (ROPEC)*, Ixtapa, 2016, pp. 1-5.

[2] A. Far, "Amplifier for energy harvesting: Low voltage, ultra low current, rail-to-rail input-output, high speed," *2016 IEEE International Autumn Meeting on Power, Electronics and Computing (ROPEC)*, Ixtapa, 2016, pp. 1-6.

[3] K. J. De Langen and J. H. Huijsing, "Compact low-voltage power-efficient operational amplifier cells for VLSI," in *IEEE Journal of Solid-State Circuits*, vol. 33, no. 10, pp. 1482-1496, Oct 1998.

[4] A. Far, "Enhanced Gain, Low Voltage, Rail-To-Rail Buffer Amplifier Suitable For Energy Harvesting", submitted to ROPEC 2017 for consideration.

[5] A. Far, "Compact Ultra Low POwer Class AB Buffer Amplifier", submitted to ROPEC 2017 for consideration.

[6] V. C. Vincence *et al.*, "A low-voltage CMOS class-AB operational amplifier," Circuits and Systems, 2002. ISCAS 2002. IEEE International Symposium on, 2002, pp. III-603-III-606 vol.3.

[7] Fan You *et al.*, "Low-voltage class AB buffers with quiescent current control," in *IEEE JSSC*, vol. 33, no. 6, pp. 915-920, Jun 1998

[8] Seevinck, E. *et al.*, "Universal Adaptive Biasing Principle for Micropower Amplifiers," in Solid-State Circuits Conference, 1984. ESSCIRC '84. Tenth European , vol., no., pp.59-62,

[9] Y. Tsuruya *et al.*, "A nano-watt power CMOS amplifier with adaptive biasing for power-aware analog LSIs," ESSCIRC (ESSCIRC), 2012 Proceedings of the, Bordeaux, 2012, pp. 69-72.

[10] M. Rezaei, E. Zhian-Tabasy and S. J. Ashtiani, "Slew rate enhancement method for folded-cascode amplifiers," in Electronics Letters, vol. 44, no. 21, pp. 1226-1228, October 9 2008.

[11] Hong-Yi Huang *et al.*, "High-gain and high-bandwidth rail-to-rail operational amplifier with slew rate boost circuit," 2006 IEEE International Symposium on Circuits and Systems, Island of Kos, 2006.

[12] M. R. Valero *et al.*,"Slew rate enhancement based on use of squaring circuits," in Electronics Letters, vol. 51, no. 3, pp. 219-220, 2 5 2015.

[13] A. T. Far, "ultra-low power bias current generation and utilization in current and voltage source and regulator devices," U.S. Patent 9 519 304, December 13, 2016

[14] Allen P.E. , "Analog integrated circuit design", John Wiley & Sons 1997.

Ali Far received the B.S. in EECS from UC Berkeley in 1983. He got his MSEE in 1986, MBA. in 1989, Juris Doctor in Law in 1997, and M.A. in Psychology in 2010, all from Santa Clara University. He is working on his M.A. in Philosophy at SFSU. He joined Plantronics in 1982 as an Audio Engineer. Between 1983 to 1985 he was a data converter Design Engineer with Precision Monolithic PMI (now part of ADI). From 1985 to 1992, he worked at MPS (now part of MaxLinear) as Design and Marketing Manager working on converters, S/Hs, high-speed amplifiers, and regulators. Then, Ali joined MVT (now part of Creative Labs) as Director of Design, making multi-media chips. Between 1994 to 1997, he worked at TelCom (now part of Microchip)as VP of Design, where he developed converters, high-power regulators, and power management chips. In 1998, Ali joined Prudential Securities, as a Semiconductor Analyst and Vice President covering investment in the analog industry. Between 2000 to 2006, he worked at Galleon, where he was an Analyst and Managing Director covering technology equities broadly, including semiconductors, storage, and networking. In 2008, he founded Spherix where he worked as an Analyst and Portfolio Manager focused on technology investments. Ali has published several papers in IEEE, has 13 patents and some pending in the area of analog, and is currently researching analog ICs for energy harvesting.