Chopper Instrumentation Amplifier Design with Fully Symmetric Loops for Input Impedance Boosting

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***Abstract* — This paper presents a chopper instrumentation amplifier (IA) architecture with two symmetric differential negative capacitance generation feedback (NCGFB) loops. The NCGFB design technique enables to cancel parasitic capacitances of cables and electrodes at the IA input in order to boost the input impedance. The negative capacitance is generated through feedback loops containing digitally programmable capacitor banks that can compensate for an extra input capacitance of up to 100 pF. A chopping technique is also introduced to enhance the noise performance of NCGFB IAs with input impedance boosting. The proposed amplifier is based on the capacitively-coupled IA (CCIA) architecture with additional circuit-level innovations to increase input impedance and improve noise performance. Two NCGFB loops have been added to further boost the input impedance. These NCGFB loops include a low-pass filter (LPF) to suppress ripples from the chopping prior to feeding the signal back to nodes at which capacitances are cancelled. We present an analysis to verify the stability of the loops as well as their effects on boosting the input impedance. The full symmetry of the NCGFB loops enables the use of identical capacitor banks to maintain a high common-mode rejection ratio (CMRR). The IA was designed and fabricated in 65-nm CMOS technology with a 1.2V supply and consumes 2.46 µW. Chip measurements show that the IA has a 44-dB gain, 40-Hz bandwidth, a total harmonic distortion (THD) of -44.3 dB with 35 mV_{pp} sinusoidal output at 10 Hz, CMRR > 90.9 dB, a 92.3 dB power supply rejection ratio (PSRR), 0.54-µV integrated input-referred noise over a bandwidth of 0.5 - 40 Hz with a noise efficiency factor of 4.75, and an input impedance of 1.9 GΩ at 10 Hz even with an extra input capacitance of 100 pF.**

***Index Terms* — Electroencephalography (EEG), dry electrodes, instrumentation amplifier, negative capacitance generation, input impedance boosting, chopping.**

I. Introduction

Instrumentation amplifiers (IAs) are essential during the acquisition of biosignals such as electroencephalography (EEG), electrocardiography (ECG) and electroretinography (ERG). IAs are typically the first block of the analog front-end that processes the signals prior to conversion with an analog-to-digital converter for digital processing. Hence, being the first block in a system, reducing noise levels is of foremost importance during their design. In addition, when integrating IAs as part of analog front-ends with low-power analog computing circuits for feature extraction [1]-[6] or when aiming to implement energy harvesting on the chip [7]-[8], it becomes crucial to prioritize the reduction of power consumption. Furthermore, gel-free electrodes (dry electrodes) are becoming increasingly popular in long-term EEG monitoring applications due to their practical advantages over wet electrodes. However, the use of dry electrodes is associated with high contact impedance at the skin interface. Hence, high input impedance is an essential requirement for instrumentation amplifiers to acquire EEG signals with high fidelity.

In this paper, we present an IA for low-power analog front-ends in EEG signal monitoring applications. The IA was derived from the chopped capacitively-coupled IA (CCIA) architecture discussed in [9]. As visualized in Fig. 1, it consists of an operational amplifier (OPAMP) with open-loop gain A_{OL}, two capacitors (C_1, C_2), and three choppers (at the input, in the feedback, and at the output; CH_{in}, CH_{fb}, CH_{out}).

A potential solution for enhancing the input impedance entails incorporating a classical negative impedance converter (NIC) at the input of the instrumentation amplifier (IA). Fig. 2(a) illustrates a simplified NIC schematic employing positive feedback, which could be employed to produce negative capacitance at the IA's input node if Z represents a capacitor [10]-[11]. The input impedance for an ideal operational amplifier with infinite open-loop gain can be calculated according to the following equations:

$$Z_{in} = -Z \times \frac{R_1}{R_2} \quad (1)$$

$$Z_{in} = -Z, \text{ when } R_1 = R_2 \quad (2)$$

However, this approach necessitates an additional amplifier, introducing undesirable power and area consumption. Furthermore, the extra amplifier would introduce additional noise

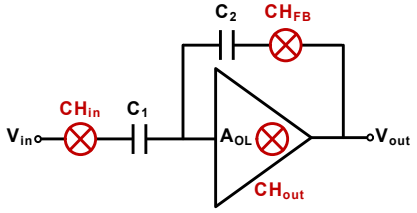

Fig. 1. Simplified representation of a capacitively-coupled instrumentation amplifier with chopping [9].

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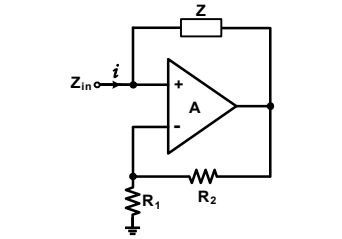
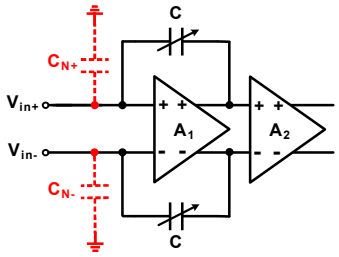


(a)



(b)

Fig. 2. (a) Standalone negative impedance converter. (b) Negative impedance generation with reuse of the first CCIA stage (A_1).

directly at the input of the IA. On the other hand, the negative capacitance generation scheme in this paper is integrated into the IA by reusing the gain of the first stage (A_1) to avoid the addition of an extra stage. As visualized in Fig. 2(b), this configuration allows to generate a negative input capacitance, whereas resistor R_{fb} (Fig. 3) is used to stabilize the bias point. We further discuss this approach in detail in Section III-C. In addition, a stability analysis and discussion for this design technique is provided in Section III-D.

The proposed CCIA has the following innovations: Two symmetric negative capacitance generation feedback (NCGFB) loops (labelled as loop 2 and loop 3 in Fig. 3) were constructed

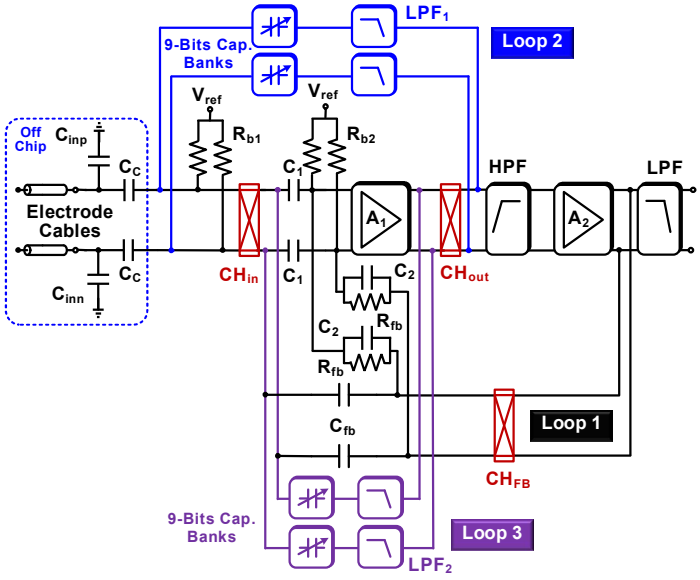


Fig. 3. Proposed chopper IA with NCGFB loops.

to boost the differential input impedance even further instead of using only loop 1 as a sole positive feedback loop. With this approach, the input impedance is increased through cancellation of extra capacitances at the input such as those associated with cables, electrodes, and package/board parasitics. Each NCGFB loop is a form of positive feedback. However, in contrast to loop 1, which is equivalent to the positive feedback loop (PFL) in [9], loops 2 and 3 in Fig. 3 include low-pass filters (LPFs) and variable capacitor banks. The LPFs suppress chopping ripples of the feedback signal for capacitance cancellations that enhance the IA input impedance as described in Section III-C. Loop 2 operates at low frequencies to compensate for C_{in}, whereas loop 3 compensates for parasitics associated with C_1 while operating with a wider bandwidth (BW) within the chopper switches. Furthermore, the variable capacitors in the feedback loops enable to nullify a wide range of capacitances. The analyses in Section III-C and Section III-D show the impact of the NCGFB loops on the IA input impedance together with a stability verification. According to simulations of the amplifier design discussed in this paper, the additions of loop 2 and loop 3 increase the input impedance by more than 9×.

The first IA architecture with NCGFB for input impedance boosting was reported in [12] with a direct current feedback architecture, but without incorporating chopping. However, the IA in [12] had relatively high-power consumption and input-referred noise due to the resistive feedback. In addition, the lack of symmetry in the NCGFB loops (due to a current mirror in the input stage) led to a limited common-mode rejection ratio (CMRR). In contrast, the IA introduced in this paper utilizes a combination of a low-power chopper CCIA architecture and symmetric NCGFB loops, resulting in a configuration that achieves high input impedance, low noise, high CMRR, and low power consumption. The design approach reduces the power consumption by 9× and the noise level by 7× compared to [12]. Furthermore, two symmetric differential NCGFB loops (loop 2 and loop 3) were constructed to cancel the input capacitances at two positions instead of only one position in prior work [12], which improved the input impedance by 1.33×.

Motivated by the analysis in [13], the fully symmetric features of the proposed IA enable the use of identical NCGFB capacitor banks, leading to a symmetric topology with higher CMRR. In our prior work [14], a chopper IA with a single differential NCGFB loop was designed using a current feedback architecture. On the other hand, the chip measurements of the first CCIA-based IA architecture with two differential NCGFB loops in this paper reveal significant improvements with regards to power and noise.

Using a new DC-servo loop (DSL) strategy, a novel approach to achieving high IA input impedance (4.6 GΩ) for neural and biopotential signal sensing was presented in [15] with a reported integrated input-referred noise of 2.1 μV_{RMS} across the BW of 1-200 Hz and with a 2.14 µW power consumption. Another recent work [16] introduces a chopper-stabilized multipath Current-Feedback Instrumentation Amplifier (CFIA) that is adaptable to function as a general-purpose operational amplifier (OPA). Employing a Local Positive Feedback Loop (LPFL), both the CFIA and OPA achieve gain-independent

impedance enhancement while preserving the advantages of chopping. The design has an excellent input impedance of 1.8 GΩ with a 3.78 μV_{RMS} integrated input-referred noise, across a wide BW of 100 Hz - 10 kHz with a power consumption of 5.35 mW. An IA specifically designed for dry-contact two-electrode ECG measurements [17] has a high input impedance of 7.5 GΩ, integrated input-referred noise of 8.5 μV_{RMS} across a BW of 100 Hz and consumes 10.5 µW. In comparison to existing works, our proposed design has input impedance of 1.9 GΩ with low 0.54 μV_{RMS} integrated input-referred noise (across its 0.5-40 Hz BW) and 2.46 µW power consumption. In addition, our work implements on-chip calibration to adapt to different input capacitances (i.e., different cable lengths) by digitally controlling the NCGFB loops [12].

This paper is organized as follows. Section II provides background information on CCIA design and on the proposed chopper architecture. Circuit design considerations and analyses are discussed in Section III. Section IV presents measurement results with discussions, whereas conclusions are made in Section 0.

II. Chopper Instrumentation Amplifier with Dual NCGFB Loops

A. Background

In general, chopping techniques involve the modulation of the input signal to shift the signal to a higher frequency before processing it further within the amplifier. It helps to reduce the impact of flicker (1/f) noise that is more severe at lower frequencies. Once the signal has been amplified in a higher frequency band with less flicker noise, it is down-converted back to its original frequency range. It is noteworthy that the output flicker noise of the amplifier is only modulated once and shifted to a higher frequency at the amplifier output [18]. Typically, an LPF is used to select the desired signal band and to suppress high-frequency noise and ripples caused by the modulators.

The three-OPAMP IA, CFIA, and resistive feedback IA (RFIA) are common traditional IA architectures. In comparison, the chopper CCIA architecture has recently been utilized to achieve relatively low power consumption with low noise operation [9], [19]-[21].

Several recent papers introduced innovative approaches to enhance the performance of IAs for different applications. Notably, [22] introduces a power-up calibration strategy to mitigate offset-induced output ripple. The design achieves a 0.25 μV_{RMS} integrated input-referred noise across a BW of 0.1-10 Hz and a power consumption of 1.5 µW. Moreover, [23] presents a technique for enhancing the common-mode rejection ratio (CMRR) with an integrated input-referred noise of 3.2 μV_{RMS} across a BW of 0.5-400 Hz with a power consumption of 2.76 µW. Furthermore, [24] proposes a Current-Balance IA (CBIA) that eliminates the requirement for input stage linearization with an integrated input-referred noise of 0.6 μV_{RMS} across a BW of 0.3-100 Hz, and with a power consumption of 3.96 µW. However, these studies either exhibit input impedance below 500 MΩ or do not provide input impedance measurement results. In this paper, we introduce a design technique to boost the input impedance to 1.9 GΩ while achieving an integrated input-referred noise of 0.54 μV_{RMS} across a BW of 0.5-40 Hz with a power consumption of 2.46 µW.

As shown in Fig. 1, the three choppers are crucial for improving noise performance and minimizing offset voltages [25]. The gain of the CCIA depends on the ratio between the two capacitors (C_1/C_2), which achieves reliable gain accuracy through the matching of the capacitors using proper layout techniques. Generally, the CCIA can be designed with high power efficiency because its OPAMP dominates the noise level. The current consumption of the CCIA can be minimized by selecting C_1 and C_2 values with relatively high impedances in the frequency range of interest, which makes the CCIA suitable for low-power applications.

B. Proposed Architecture

Fig. 3 displays the block diagram of the proposed chopper CCIA architecture with NCGFB loops, which consists of two OPAMP stages (A_1 and A_2), capacitors (C_1 and C_2) that determine the gain of the IA, three choppers (CH_{in}, CH_{out} and CH_{fb}), a high-pass filter (HPF), several LPFs and feedback capacitor banks. The IA is AC-coupled through off-chip capacitors (C_C) in order to block DC offsets such as from electrodes. In combination with the on-chip bias resistors (R_{b1} ≈ 10 GΩ), a minimum C_C value of 500 pF is required to create high-pass filtering with a cut-off frequency of 0.03 Hz such that the signals of interest can pass. The gain of the IA can be estimated as follows:

$$G = \frac{A_{OL}}{1+A_{OL}\ C_2/C_1} \tag{3}$$

where A_{OL} is the open-loop gain of the OPAMP, which should be very high to achieve better gain accuracy. Hence, two amplification stages are used to achieve high gain. Fig. 4 shows that the first stage is a folded cascode stage that has a high DC gain of 59.9 dB. The second stage is a class-A output stage that provides large output swing with a gain of 13.3 dB, where a Miller compensation capacitor (C_m) was added to ensure stability. The input impedance of the IA is strongly influenced by the combination of the input chopper CH_{in} and the input capacitor C_1. With chopping, the low equivalent capacitor impedance magnitude of $1/(2 \cdot f_{ch} C_1)$ causes the overall input

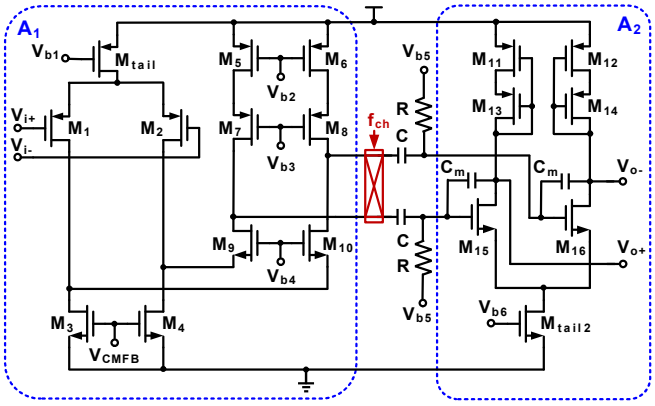


Fig. 4. Schematic of amplifiers A_1 and A_2.

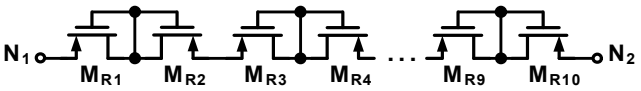


Fig. 5. Pseudo-resistor configuration.

impedance to be low, where f_{ch} is the chopper frequency. For this reason, the input impedance is boosted using two approaches that are combined in this architecture: 1) a PFL as in [9], which contains CH_{fb} and C_{fb}, denoted as loop 1 in Fig. 3; as well as 2) two differential NCGFB loops that are discussed in the Section III, denoted as loop 2 and loop 3 in Fig. 3. The OPAMP input DC voltage level is defined using V_{ref}, R_{b1} and R_{b2}; where R_{b1} and R_{b2} are high-resistance pseudo-resistors as in [12], [26]-[28]. Utilizing pseudo-resistors provides the benefit of area efficiency over conventional resistor types, making them especially well-suited for compact integrated circuit designs. They are implemented using 10 PMOS devices as shown in Fig. 5, with a total area of 42.3 µm × 8.59 µm and 52 µm × 7.3 µm, respectively. The ripples produced by the choppers are suppressed by a LPF at the IA output.

III. Circuit Design Considerations and Analyses

In the proposed CCIA (Fig. 3), C_1 and C_2 are metal-insulator-metal (MIM) capacitors with values of 50 pF and 300 fF, respectively. Hence, the expected closed-loop gain is 44 dB. MIM capacitors were used due to their good precision, minimal noise contribution and relatively small fringe capacitance. Furthermore, the specific values for C_1 and C_2 were selected to attain a gain of 44 dB while ensuring stability, linearity, and noise performance. The chopper frequency f_{ch} should be chosen to be higher than the 1/f noise corner frequency of the first stage (A_1). Therefore, its value was selected to be 4 kHz in this design. Without compensation, the input impedance would be approximately 2.5 MΩ based on the selected values of C_1 and f_{ch}. The resistor-capacitor HPF after A_1 (Fig. 4) blocks the DC offset to avoid amplification by A_2. The resistor in each HPF was implemented with a pseudo-resistor using 10 PMOS devices as in [12]. An equivalent value of 284 GΩ was obtained with a 213.8 µm × 26 µm layout area. The capacitor is a MIM capacitor with a value of 20 pF, which was obtained with a 182.6 µm × 96.5 µm layout area. This combination results in a cutoff frequency of 0.03 Hz, which is lower than the EEG signals of interest. Wide design margins were intentionally used to ensure that the cutoff frequency of the HPF remains significantly below 0.1 Hz despite of pseudo-resistor variations. This objective was achieved through a strategic selection of the transistor channel lengths across a range from 60 nm to 5 µm. As a result, the simulated HPF cutoff frequencies exhibit values between 0.01 Hz and 0.08 Hz across various statistical process corners. Furthermore, a common-centroid layout style has been used to mitigate the influence of device mismatches, which also incorporated dummy guard rings. A common-mode feedback (CMFB) circuit is used within A_1 to regulate the gate voltage (V_{CMFB}) of transistors M_3 and M_4 as shown in Fig. 4.

As explained earlier, the input impedance of the CCIA would be low (~2.5 MΩ), which creates the need for input impedance enhancement techniques. Here, boosting of the input impedance is realized through two mechanisms. First, loop 1, which consists of CH_{fb} and C_{fb} in Fig. 3, compensates some of the drawn input current through the input chopper by converting the output voltage into current and injecting it at the input node. Here, C_{fb} was chosen to be equal to C_2 to boost the input impedance as demonstrated in [9], which leads to a simulated input impedance of around 161.7 MΩ for this design when only loop 1 is activated. However, the input impedance is still relatively low without the second technique applied in the proposed CCIA, which involves the NCGFB loops. The main purpose of the NCGFB loops is to cancel the undesired capacitances at the input, including those from electrode cables. In the proposed CCIA, two differential NCGFB loops are used, which are loop 2 and loop 3 in Fig. 3. Each loop consists of a LPF (LPF_1, LPF_2) and 9-bit capacitor banks. Loop 2 targets to cancel the parasitic capacitances of the electrode cables and CH_{in}, while loop 3 partially cancels the parasitic layout capacitances that are primarily associated with the bottom plate of C_1. With this approach, the input impedance can be boosted to above 1 GΩ with extra input capacitance (C_{in}) values up to 100 pF. This capacitance value was selected to represent a cable length in the approximate range of two to seven feet based on characteristics of commonly used cables such as shielded twisted-pair, coaxial, multiconductor, and flat ribbon cables; which typically exhibit capacitances per length of 15-50 pF/ft [29]-[31]. The activation of the additional NCGFB loops (loop 2 and loop 3) increased the simulated input impedance to 1.47 GΩ. Note that after activating the NCGFB loops, the simulated gain reduced by approximately 1 dB while the input-referred noise did not change significantly compared to simulations in which only loop 1 was activated.

The complete IA with NCGFB loops and chopping was simulated with combinations of process corner cases (SS, TT, FF), ±5% supply voltage changes (1.14 V, 1.2 V, 1.26 V), and different temperatures (-20˚C, 27˚C, 85˚C). With these variations, the worst-case input impedance was 1.002 GΩ,

Table I. Simulation results for the complete IA design

CMOS Techn. (nm)	65
Chopper Frequency (kHz)	4
Power (µW)	2.26
Gain (dB)	44
Integrated Input-Referred Noise (μV_{RMS}) [BW]	0.40 [0.5 - 40 Hz]
THD (dB)	-86.4 (35 mV_{pp} out @ 10 Hz)
CMRR (dB)	121
PSRR (dB)	83
Input Impedance (GΩ)	1.5 @ 10 Hz
NEF*	3.12
Area (mm^2)	0.49

* Noise Efficiency Factor (NEF) = $V_{RMS,in} \times \sqrt{\frac{2 \times I_{tot}}{\pi \times V_T \times 4KT \times BW}}$

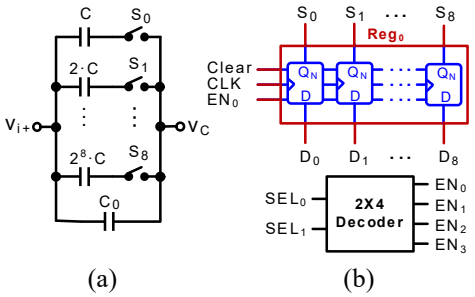


Fig. 6. (a) A 9-bit programmable capacitor bank, and (b) an example of one control register with an enable input that is generated using a 2×4 decoder.

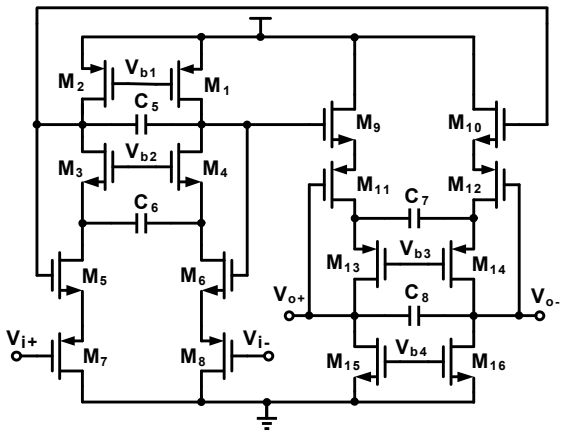


Fig. 7. 4th -order LPF schematic [35].

indicating the robustness of the NCGFB loops. Furthermore, the most significant gain variation of 11.7% occurred with the (TT corner, 1.26 V, -20˚C) conditions, and the worst-case noise of 0.94 μV_{RMS} was observed in the (SS corner, 1.14V, 85˚C) case. Monte Carlo simulations with 10 runs revealed a CMRR mean (μ) of 121.5 dB with a standard deviation (σ) of 9.1 dB. As discussed in Section IV, the measured CMRR value exceeds 90.9 dB, falling within the (μ-σ) range. Similarly, the simulated mean (μ) of the PSRR was 83.2 dB with a standard deviation (σ) of 8.8 dB. The measured PSRR value of 92.3 dB discussed in Section IV lies within the (μ+σ) range. The simulation results of the IA (TT corner, 1.2 V supply, 27˚C) are summarized in Table I.

A. Capacitor Banks

For the generation of adjustable negative capacitances, four programmable capacitor banks are utilized in the NCGFB loops to support digitally-controlled calibrations in systems-on-a-chip [14], [32]. As depicted in Fig. 6(a), each capacitor bank consists of nine capacitors and nine switches in addition to one capacitor without a switch. The value of capacitor (C_0) is 100 fF, whereas the unit capacitor (C) has a value of 10 fF, such that the largest switched capacitance is 2.56 pF. Hence, the minimum and maximum capacitance values that can be generated are 100 fF and 5.21 pF, respectively. These values were chosen to be able to boost the input impedance with extra input capacitance (C_{in}) values up to 100 pF. The switches are implemented with PMOS transistors having a digitally controllable gate voltage (S_0-S_8). PMOS transistors were used because of their ability to provide low leakage current in the off state with the voltage levels at the nodes where the capacitor banks are connected. Four registers are used for controlling the four banks through only nine lines (D_0-D_8), which are connected to external switches on the test board. Each register consists of nine data flip flops (DFFs), and all four registers share the same nine control input lines. Hence, an Enable (EN) signal is needed to select a certain register to be loaded. These EN signals are generated through two selection lines and a decoder as shown in Fig. 6(b). Using this configuration, only nine control lines are used to control the total of 36 capacitors.

B. LPFs Design

The LPFs filter out the chopping spikes before the signals enter the capacitor banks in the NCGFB loops and after the second stage of the IA (A_2). The LPFs in the feedback loops help to boost the input impedance even further. These filters are 2nd-order unity-gain Sallen-Key filters [33]. Sallen-Key filters offer a maximally flat magnitude response and well-defined cutoff frequencies, ensuring precise control over signal BW and attenuation characteristics, which is critical in this application. Furthermore, they exhibit excellent stability and robustness against component variations, temperature changes, and manufacturing tolerances, ensuring consistent performance across diverse operating conditions. The OPAMP used in the LPFs is a two-stage Miller-compensated OPAMP with a PMOS input pair [34], which ensures stability and low-noise performance. The cutoff frequencies are 3.5 kHz and 515 Hz for LPF_1 and LPF_2, respectively.

The output LPF schematic is displayed in Fig. 7, which is a 4th-order low-power topology with a cutoff frequency of 40 Hz, which is appropriate for EEG feature extraction in wearable devices utilizing dry electrodes [1]. It consists of two pseudo-differential biquad stages, where each stage exhibits a body effect but in a complementary manner. Hence, the overall gain is not attenuated and is approximately 0 dB [35]. Furthermore, this LPF topology was chosen for its low power consumption.

C. Input Impedance Analysis

As previously stated, the incorporation of the Sallen-Key LPF within each NCGFB feedback loop serves the purpose of attenuating the chopping spikes that impact the input impedance value. The LPF can be characterized by a second-order transfer function expressed as follows:

$$H_{LPF}(s) = \frac{1}{1 + a \cdot s + b \cdot s^2} \tag{4}$$

$$a = 2 \times C_3 \times R, \quad b = C_3 \times C_4 \times R^2 \tag{5}$$

Therefore, the calculation of the single-ended input impedance can be obtained through the utilization of the following equations, derived from the analysis of the simplified schematic

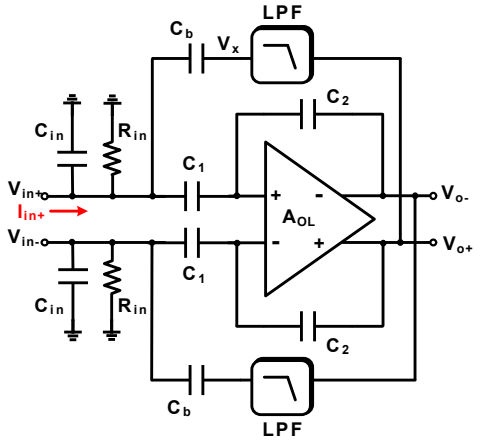


Fig. 8. Simplified schematic for input impedance analysis.

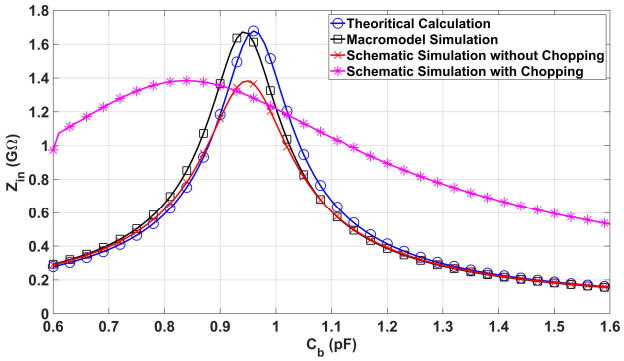


Fig. 9. Input impedance evaluations at 10 Hz vs. C_b.

depicted in Fig. 8 with the corresponding IA design parameters values. In this schematic, the variable capacitor C_b represents the capacitor bank. Moreover, the amplifier is represented by a single-stage amplifier with an open-loop gain (A_{OL}) which characterized by a first-order function given by

$$A_{OL}=\frac{A_o}{1+\frac{s}{\omega_o}} \tag{6}$$

where A_o represents the DC open-loop gain and ω_o represents the open-loop -3 dB cutoff frequency. A_o is designed to be sufficiently high so that the two differential inputs of the OPAMP can be effectively regarded as virtual AC grounds. Based on these assumptions, the single-ended input impedance can be derived as follows:

$$I_{in+}=C_b\times(V_{in+}-V_x)\cdot s+V_{in+}\times(C_{in}\cdot s+\frac{1}{R_{in}})+V_{in+}\times C_1\cdot s \tag{7}$$

$$V_x=H_{LPF}(s)\times V_{O+}=H_{LPF}(s)\times\frac{A_{OL}}{1+A_{OL}\times\frac{C_2}{C_1}}\times V_{in+} \tag{8}$$

$$I_{in+}=V_{in+}(\frac{1}{R_{in}}+(C_{in}+C_1)\cdot s+C_b(1-\frac{1}{1+a\cdot s+b\cdot s^2}\times\frac{A_{OL}}{1+A_{OL}\times\frac{C_2}{C_1}})\cdot s) \tag{9}$$

$$Z_{in+}=\frac{1}{\frac{1}{R_{in}}+(C_{in}+C_1)\cdot s+C_b(1-\frac{1}{1+a\cdot s+b\cdot s^2}\times\frac{A_{OL}}{1+A_{OL}\times\frac{C_2}{C_1}})\cdot s} \tag{10}$$

The third term in the denominator of Eq. (10) enables to nullify the effects of the input capacitance C_{in} and the impact of C_1. This compensation is accomplished by employing the variable capacitance C_b and leveraging the closed-loop gain of the IA. When designing with high open-loop gain (A_{OL}), the third term in the denominator depends predominantly on the ratio between C_1 and C_2. At low frequencies, the LPF gain in Eq. (4) is approximately equal to 1, which requires careful selection of the component values in Eq. (5) to ensure that the LPF cutoff frequency is higher than the BW of interest. When this condition is met, then the numerator of Eq. (10) can be simplified further to approximate Z_{in+} as follows:

$$Z_{in+}\approx\frac{1}{\frac{1}{R_{in}}+(C_{in}+C_1)\cdot s+C_b(1-\frac{C_1}{C_2})\cdot s} \tag{11}$$

The approximation accuracy of the input impedance equation can be substantiated through four different modeling implementations of the test schematic in Fig. 8, which are: (i) employing Matlab for numerical evaluation of the input impedance equation, (ii) simulation of the test schematic utilizing an IA macromodel based on Eq. (6). (iii) simulation of the test schematic utilizing the IA as a transistor-based amplifier designed in 65-nm CMOS technology, and (iv) simulation as in (iii) but with choppers (CH_{in}, CH_{out}, CH_{fb}). Fig. 9 represents the input impedance at a frequency of 10 Hz as a function of C_b, where both the theoretical calculations (methodology i) and the macromodel simulation (methodology ii) yield a maximum input impedance value of approximately 1.6 GΩ. Similarly, the schematic simulation (methodology iii) and the schematic with chopping simulation (methodology iv) resulted in a maximum input impedance around 1.4 GΩ. The maximum input impedance value occurs at C_b 0.96 pF, 0.95 pF, 0.94 pF and 0.84 pF for the four evaluations, respectively. The slight difference of the optimum C_b value between the theoretical calculations and the macromodel simulation can be attributed to the assumption made in the theoretical analysis with an ideal virtual short circuit directly at the inputs of the OPAMP (A_{OL}). Conversely, the difference between the theoretical calculations and the schematic simulation can be attributed to the presence of parasitic capacitance associated with the transistors and to the chopping mechanism, which leads to a lower input impedance value.

D. NCGFB Loop Stability

The NCGFB loop comprises a positive feedback configuration, which includes the Sallen-Key LPF and the capacitor bank. Therefore, it is essential to ensure the stability of this loop. As shown in Fig. 8, the open-loop gain can be expressed as follows:

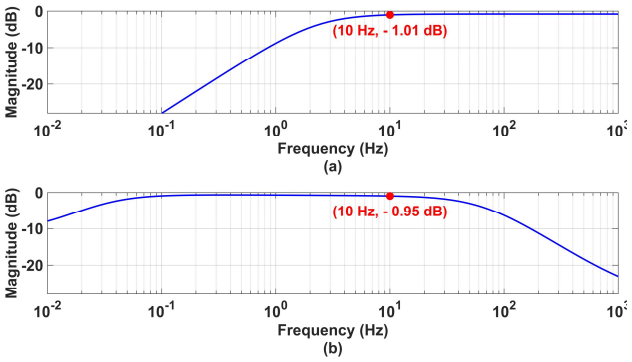


Fig. 10. NCGFB loop gain vs. frequency: (a) numerical evaluation, (b) schematic simulation result (with chopping).

$$Loop\ Gain = A_{CL}(s) \times H_{LPF}(s) \times H_{VD}(s) \tag{12}$$

where $A_{CL}(s)$ is the closed-loop gain of the amplifier illustrated in Fig. 8, which is the same gain as in Eq. (3). $H_{LPF}(s)$ is the transfer function of the LPF as written in Eq. (4). Furthermore, $H_{VD}(s)$ represents the transfer function of the voltage divider involving C_b, C_{in}, C_1 and R_{in} in Fig. 8, which is determined by the following equation:

$$H_{VD}(s) = \frac{(C_b \times R_{in}) \cdot s}{1 + R_{in} \times (C_b + C_{in} + C_1) \cdot s} \tag{13}$$

Therefore, the equation for the total loop gain becomes:

$$Loop\ Gain = \frac{A_{OL}}{1 + A_{OL} \times \frac{C_2}{C_1}} \times \frac{1}{1 + a \cdot s + b \cdot s^2} \times \frac{(C_b \times R_{in}) \cdot s}{1 + R_{in} \times (C_b + C_{in} + C_1) \cdot s} \tag{14}$$

The stability of the NCGFB loop can be verified by examining Fig. 10(a), which was obtained through numerical evaluation of Eq. (14) with the corresponding design parameters. On the other hand, Fig. 10(b) shows the transistor-level schematic simulation result with chopping. In both Fig. 10(a) and Fig. 10(b), the loop gain consistently remains below 0 dB, which ensures stability. The validity of this condition is expected based on Eq. (14), where the three numerators are always smaller than their corresponding denominators, resulting in a loop gain that remains below 0 dB. The lower cutoff frequency of the simulated loop gain in Fig. 10(b) is less than the lower cutoff frequency observed with the numerical evaluation. This discrepancy can be attributed to the presence of RC biasing configurations at the transistor level, which are not captured by the equations for the numerical evaluation. Similarly, the higher cutoff frequency of the loop gain in Fig. 10(b) is less than the corresponding cutoff frequency shown in Fig. 10(a). This difference is due to parasitic capacitances associated with the choppers, pseudo-resistors and transistors in the amplifier.

The input-referred noise of the proposed CCIA can be estimated as in [15], [19], [36]; where the key difference is the impact of the two filters LPF_1 and LPF_2:

$$\overline{V_{n,in}^2} = \left(\frac{C_{tot}}{C_1}\right)^2 \left(\overline{V_{n,in,A_1}^2}\right) + H_{VD}^2(s) \left(\overline{V_{n,out,LPF_1}^2} + \overline{V_{n,out,LPF_2}^2}\right) + \left(\overline{I_{n,R_{fb}}^2} + \overline{I_{n,R_{b1}}^2} + \overline{I_{n,R_{b2}}^2}\right) \overline{R_{in,eq}^2} \tag{15}$$

In equation (15), C_{tot} represents the total capacitance consisting of C_1, C_2 and the parasitic capacitance at the input of A_1, $\overline{V_{n,in,A_1}^2}$ denotes the input-referred noise of the first stage of the CCIA (A_1), $H_{VD}(s)$ is the transfer function in Eq. (13), $\overline{V_{n,out,LPF_1}^2}$ is the output-referred noise of LPF_1, $\overline{V_{n,out,LPF_2}^2}$ is the output-referred noise of LPF_2, $\overline{I_{n,R_{fb}}^2} = 8kT/R_{fb}$ is the noise current of R_{fb}, $\overline{I_{n,R_{b1}}^2} = 8kT/R_{b1}$ is the noise current of R_{b1}, and $\overline{I_{n,R_{b2}}^2} = 8kT/R_{b2}$ is the noise current of R_{b2}; where k is the Boltzmann constant and T the absolute temperature in Kelvin.

In order to minimize the noise impact of LPF_1 and LPF_2, the following condition should be satisfied:

$$C_{in} + C_1 \ll C_b \tag{16}$$

As discussed in Section III, the design value of C_1 and the maximum achievable value of C_b are 50 pF and 5.21 pF respectively, which fulfill this condition.

Given that C_2 and the parasitic capacitance at the input of A_1 are significantly smaller than C_1, the ratio C_{tot}/C_1 is approximately equal to 1. Thus, the CCIA can be very power-efficient with relatively high closed-loop gain (>5). Furthermore, since R_{fb}, R_{b1} and R_{b2} are resistances with high values (in the GΩ range), their noise current can be neglected. When satisfying the above assumptions, the input-referred noise of the CCIA can be estimated with the following simplified equation:

$$\overline{V_{n,in}^2} \cong \frac{8kT\gamma}{g_{m1,2}} \left(1 + \frac{g_{m3,4} + g_{m5,6}}{g_{m1,2}}\right) \tag{17}$$

With the values of this design ($g_{m1,2}$ = 13.33 µS, $g_{m3,4}$ =13.82 µS, and $g_{m5,6}$ = 2.75 µS) and assuming $\gamma = 2/3$, we obtain $\overline{V_{n,in}^2}$ = 3.71 fV^2/Hz. Therefore, the expected integrated input-referred noise across the BW (0.5-40 Hz) equals to 0.38 μV_{RMS}. This analytically calculated result was confirmed by comparing it with the transistor-level simulation result and the measured value of 0.4 μV_{RMS} and 0.54 μV_{RMS} respectively, which are listed in Table I and Table II.

IV. Chip Measurement Results

A prototype chip was designed and fabricated with 65-nm CMOS technology. Even though technologies with longer channel length are sufficient for this IA's frequency range, the 65nm technology was selected to target easier integration into systems-on-a-chip with circuits for wireless connectivity in the future. It was assembled in a S/B 48L package and tested on a printed circuit board (PCB). Fig. 11 displays the chip layout and micrograph. The IA layout occupies 0.49-mm^2 of die area. An off-the-shelf amplifier (AD8421) on a reliable evaluation board (EVAL-INAMP-82RMZ), which is commercially available, was used to convert the differential IA output to a single-ended output with the capability of driving the off-chip measurement equipment. The AD8421 was not soldered onto the PCB to

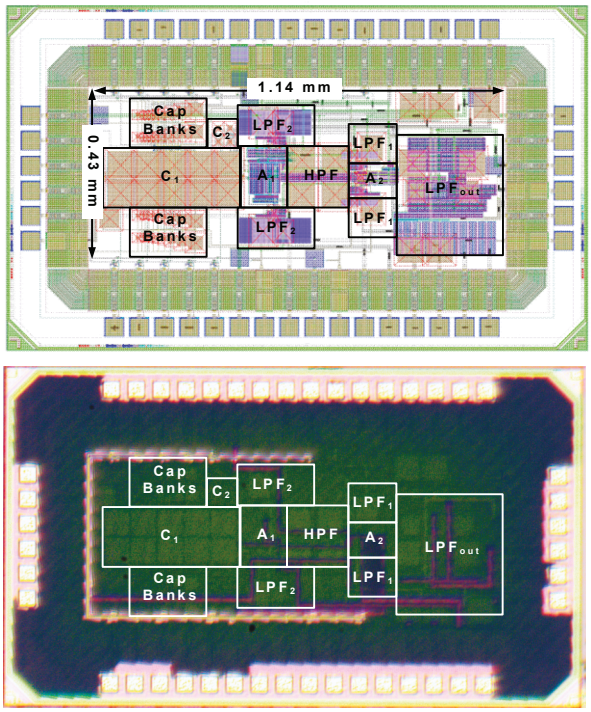


Fig. 11. Chip layout and micrograph.

avoid any unnecessary increase in PCB dimensions. On the main PCB with the IA, an amplifier (AD8131) is connected to the IA inputs in order to convert from a single-ended input to a differential signal.

The measurement setup to test the prototype chip is visualized in Fig. 12, where connection 1 was used to measure the transient gain of the IA, and connection 2 was used to measure the THD. Connection 2 was also used during the frequency response measurements, but while connecting the input attenuator to the dynamic signal analyzer (instead of the signal generator) for the frequency sweep.

The measured frequency response of the proposed CCIA with NCGFB is displayed in Fig. 13, which was plotted after de-embedding the gain of the amplification on the PCB. The IA's low-frequency gain is 44 dB with a -3dB frequency of 40 Hz. The transient output measured with a 230-μV_{pp} sinusoidal input signal at 10 Hz is shown in Fig. 14, where the measured differential output voltage of the IA is 35-mV_{pp}. The annotated 470-mV_{pp} value in the figure includes the 23 dB gain of the off-chip amplification on the PCB. The output spectrum with 230-

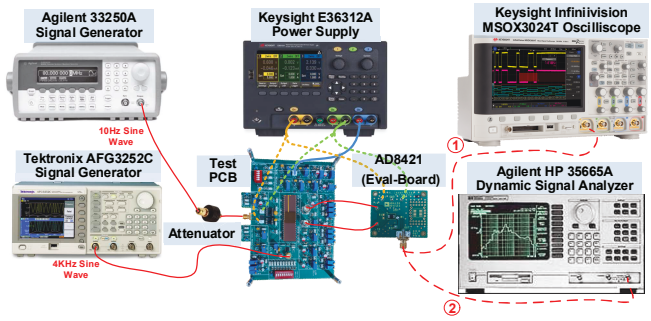


Fig. 12. Measurement setup for the characterization of the prototype chip.

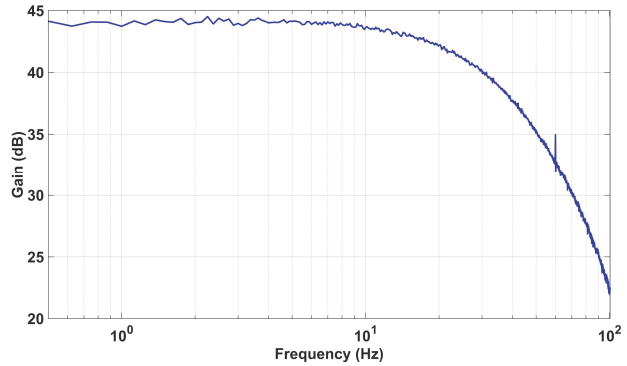


Fig. 13. Measured frequency response.

μV_{pp} sinusoidal input and 35-mV_{pp} directly at the IA output is displayed in Fig. 15, showing that the THD is -44.4 dB under this condition is dominated by the third-order harmonic distortion (HD_3) component (with other distortion components under the noise floor). When the same input signal is applied to the IA with a ±150 mV DC offset, the gain variation is less than 0.6 dB and the HD_3 remains below -44 dB. With a swing of 300 mV_{pp} directly at the IA output, the HD_3 increases to -39.65 dB. On the other hand, a low-swing input of 4-μV_{pp} was also applied to the IA, which resulted in a signal that is visible at 10 Hz above the output noise level in Fig. 16.

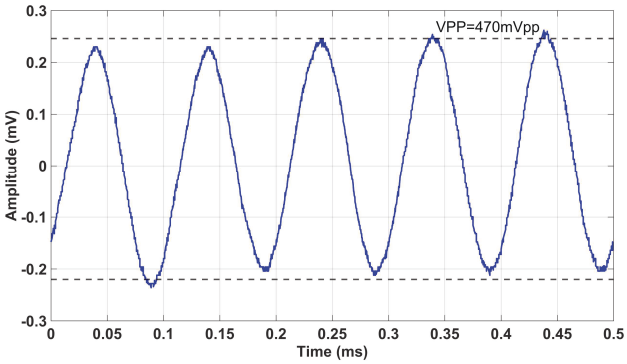


Fig. 14. Transient output waveform measured with a 230-μV_{pp} sinusoidal input at 10 Hz: 35-mV_{pp} IA output (470-mV_{pp} output with amplification on the PCB).

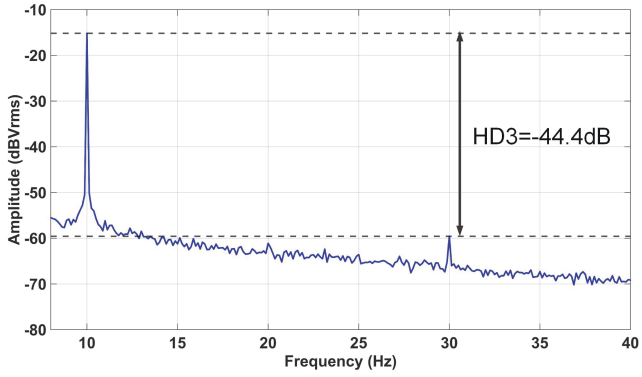


Fig. 15. Output spectrum measured with a 230-μV_{pp} sinusoidal input (10 Hz) and 35-mV_{pp} IA output (470-mV_{pp} output with amplification on the PCB).

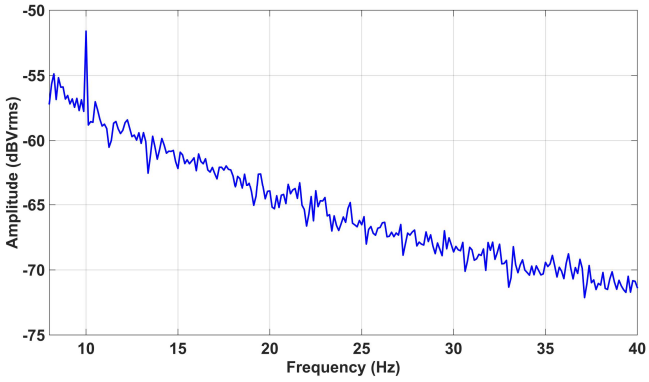


Fig. 16. Measured output spectrum with a 4-μV_{pp} sinusoidal input (10 Hz) and 0.52-mV_{pp} IA output (7.4-mV_{pp} output with amplification on the PCB).

Fig. 17 shows the measured output noise spectrum from three different test cases. First, the noise was measured for the IA with the evaluation board (blue line). Second, it was measured for the evaluation board only (red line) with the IA powered down but the off-chip amplifier on the evaluation board powered up. With these results, the noise of the evaluation board was de-embedded to extract the IA's noise (pink line), which resulted in a total of 0.54-μV_{RMS} integrated input-referred noise in the BW of 0.5 - 40 Hz.

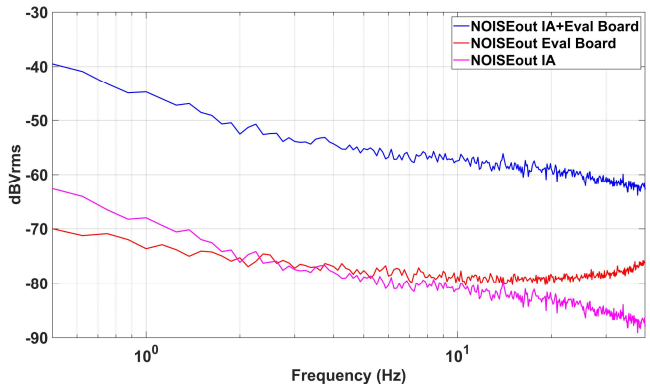


Fig. 17. Measured output noise spectra.

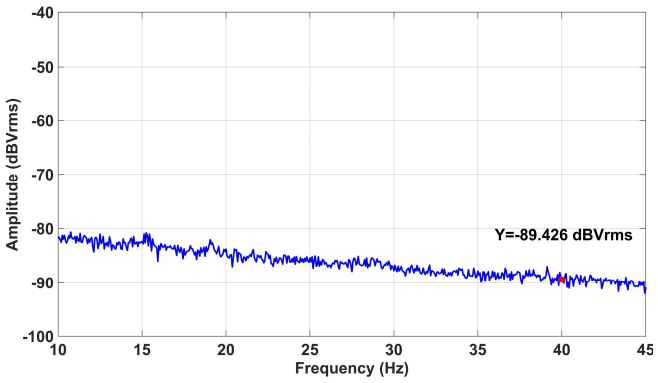


Fig. 18. Measured differential output voltage spectrum of the IA with a 1.5 mV_{pp} sinusoidal input signal at 40 Hz.

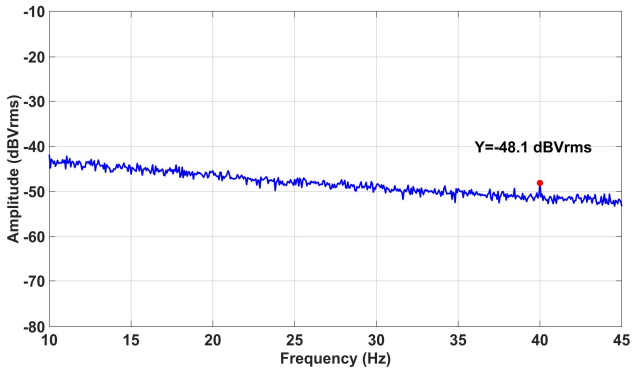
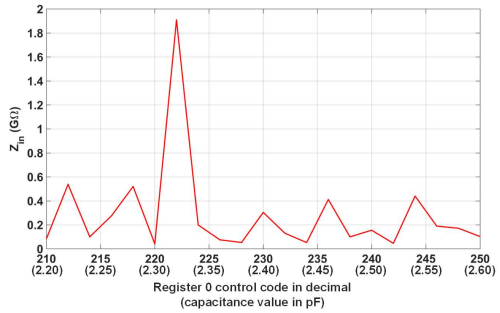
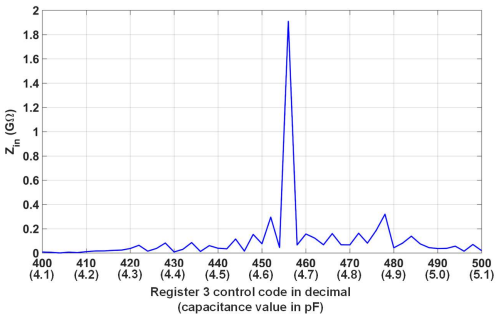


Fig. 19. Measured differential output voltage spectrum of the IA with a sinusoidal signal of 200 mV_{pp} at 40 Hz added to the supply voltage.

The measured differential output voltage spectrum of the IA with a common-mode sinusoidal signal input of 1.5 mV_{pp} (-65.5 dBV_{RMS}) at 40 Hz is displayed in Fig. 18. This $\leq$ -89.4 dBV_{RMS} output measurement includes the gain of the off-chip amplification on the evaluation board (23 dB). Hence this result implies a common-mode gain less than -46.9 dB, and that the CMRR exceeds 90.9 dB. The measured CMRR remains around this value until the input common-mode voltage reaches 30 mV_{pp} (-39.48 dBV_{RMS}), at which the CMRR degrades by approximately 1 dB to 90.0 dB. A common-mode input of 100 mV_{pp} (-29.03 dBV_{RMS}) at 60 Hz results in a CMRR degradation of approximately 1.4 dB, yielding a measured CMRR of 89.5 dB.



(a)



(b)

Fig. 20. Measured input impedance at 10 Hz with extra off-chip input capacitance of 100 pF: (a) sweep of the Register 0 control code while keeping Register 1 @ 431, Register 2 @ 416, Register 3 @ 456, (b) sweep of the Register 3 control code while keeping Register 1 @ 431, Register 2 @ 416, Register 0 @ 222.

The measured differential output voltage of the IA with a sinusoidal input signal of 200 mV_{pp} (-23 dBV_{RMS}) at 40 Hz applied on top of the supply voltage is shown in Fig. 19. The measured -48.1 dBV_{RMS} output at 40 Hz includes the gain of the 23 dB off-chip amplification. Hence this result implies a power supply gain of -48.3 dB. Consequently, the PSRR is 92.3 dB.

The input impedance was measured by connecting a 400 MΩ test resistor (R_s) in series directly at each input of the IA using jumpers on the PCB. In this configuration, the peak-to-peak amplitude of the output transient voltage (V_{opp}) was measured while a sinusoidal input voltage (V_{spp}) was applied at 10 Hz, such that the input impedance can be determined according to the following equation:

$$Z_{inSE} = \frac{R_s \times V_{opp}}{V_{spp} \times A_{CL} - V_{opp}} \tag{18}$$

The optimum measured input impedance is 1.9 GΩ, as can be observed in Fig. 20. To obtain these plotted results, the input impedance was measured during a sweep of the control code in one register, while keeping the other registers constant at their optimum value. For illustration, the codes of Register 0 and Register 3 were swept in the plots in Fig. 20 because they control the NCGFB capacitance banks that compensate for the extra 100 pF capacitances connected at the IA inputs on the PCB. Register 1 and Register 2 control the NCGFB capacitor bank for cancellation of the on-chip parasitic capacitances (including those associated with the bottom plates of the C_1 capacitor in Fig. 3).

Table II provides a comparison of the measured results and other state-of-the-art IA designs. Compared to other works, this design achieves a low noise level while consuming low power. Some tradeoffs can be noticed from the state-of-the-art results. Although the noise level is slightly higher compared to the IA in [40], our design has lower power consumption and higher input impedance while using a single supply voltage. It is worth noting that the work presented in [41] attains an input impedance of up to 15 GΩ at 10 Hz with an added capacitance of 82 pF, while dissipating 3.83 µW from two power supplies (1 V and 1.5 V). The work stands out as it also provides the ability to compensate for additional capacitance at the inputs, while demonstrating that automatic calibration with fine resolution permits to further boost the input impedance. We conclude that the CMRR of this work is higher than the measured value of 90.9 dB based on a simulated mean of 121.5 dB and a standard deviation of 9.1 dB. However, it was not possible to measure the value of the CMRR beyond the 90.9 dB level reported in Table II due to the noise floor limitation of the

Table II. Comparison between the state-of-the-art IA designs.

	[9], 2011	[12], 2017	[37], 2020	[38], 2019	[39], 2020	[15], 2021	[22], 2021	[23], 2021	[40], 2022	[41], 2022	[16], 2023	[24], 2023	[17], 2023	**This Work**
Techn. (nm)	65	130	180	180	180	180	180	180	180	110	180	350	180	**65**
Chopp. Freq. (kHz)	5	-	5	20	6	10	5	0.5	10	5	25	1	-	**4**
Supply (V)	1	1.2	1.8	1.8	1.2	1	1.2	1.2	0.5/1.8	1/1.5	5	3	1.8	**1.2**
Power (µW)	1.8	23.28	10.44	3.24	2.4	2.14	1.5 (8 slices)	2.76	4.5	3.83	5350	3.96	10.5	**2.46**
Gain (dB)	40	30-40	40-49.5	40	40	40	40	40	60	61-74	20	34	34	**44**
BW (Hz)	0.5-100	0.5-45.5	0.5-250	0.35-5.4k	0.04-932	200	~100	400	300	0.5-300	850k	0.3-100	50k	**40**
Integrated Input-Referred Noise (μV_{RMS})	0.64* (0.5-100Hz)	3.75** (0.5-45.5Hz)	0.7 (0.5-100Hz)	0.65 (0.3-200Hz)	1.8 (0.5-500 Hz)	2.1 (1-200Hz)	0.25* (8 slices) (0.1-10 Hz)	3.2 (0.5-400Hz)	0.22 µV (3-300Hz)	0.36 (0.5-300Hz)	3.78*** (100-10kHz)	0.6 (0.3-100Hz)	8.5 (100Hz)	**0.54 (0.5-40Hz)**
THD (dB)	-	-49** ($60mV_{pp}$ out @5Hz)	-	-61 ($500mV_{pp}$ out @5Hz)	-82 ($1.6V_{pp}$ out @69Hz)	-	-	-	-63 ($500mV_{pp}$ out @50Hz)	-53.2 ($2.5mV_{pp}$ in)	-	-40.9 ($200mV_{pp}$ out@10Hz)	-	**-44.3 ($35mV_{pp}$ out@10Hz)**
CMRR (dB)	134 @ DC	77.6** @10Hz	102 @50Hz	> 100	>90	-	109 @ DC	>110 @ 50/60Hz	84	92 @ 20Hz	128 @5Hz	99.8 @50Hz	109 @50Hz	**> 90.9 @ 40Hz**
PSRR (dB)	120 @ DC	74** @10Hz	72 @50Hz	> 70	-	-	92 @ DC	>83 (1-400Hz)	88	100 @ 10Hz	122 @5Hz	102 @50Hz	-	**92.3 @ 40Hz**
Input Impedance (GΩ)	0.03	>1.42** @20Hz >0.57** @50Hz	2.4 @60Hz	0.44 @50Hz	>1 @50Hz	4.6 @0.01Hz	-	-	>1	15 @10Hz	1.8 @5Hz	0.46 @50Hz	7.5 @1Hz 0.3 @50Hz	**1.9 @10Hz**
NEF****	3.30	95	4.83	2.37	4.40	8.40	3.48 (8 slices)	9.40	1.30	1.54	47.96	2.73	79.2	**4.75**
Area (mm^2)	0.1	0.183	0.99	0.2	0.46	0.19	0.57	1.57	0.18	0.75	0.9	0.41	0.34	**0.49**

* Calculated from the NEF ** Measured with IA, filter and variable gain amplifier

*** Calculated from the reported noise spectral density and BW **** Noise Efficiency Factor (NEF) = $V_{rms,in} \times \sqrt{\frac{2 \times I_{tot}}{\pi \times V_T \times 4KT \times BW}}$

test setup and equipment, as can be seen from Fig. 18. In practice, we expect that packaging and PCB optimizations can improve the CMRR and PSRR.

The results in Table II indicate a tendency for the noise efficiency factor (NEF) to improve with BW in the sub-1 kHz frequency range. The IA in this work has a 40 Hz BW with suitability for EEG feature extraction in wearable devices with dry electrodes [1], which is limited by the LPF at the output in Fig. 3, hence restricting the achievable NEF.

V. Conclusion

A chopper IA architecture with symmetric NCGFB loops was designed and fabricated with a 65-nm technology and a 1.2-V supply. The NCGFB loops are digitally programmable to boost the input impedance up to 1.9 GΩ with 100 pF extra capacitance at each of the IA inputs. Prototype chip measurements of the proposed instrumentation amplifier demonstrated significant improvements in noise performance and input impedance while overall maintaining state-of-the-art performance compared to other instrumentation amplifiers. The IA has a measured gain of 44 dB with 40 Hz BW, and a total harmonic distortion of approximately -44 dB with 35-mV_{pp} output swing. Remarkably, the measured input impedance is 1.9 GΩ at 10 Hz. Furthermore, the measured CMRR exceeds 90.9 dB at 40 Hz, along with a PSRR of 92.3 dB. An integrated input-referred noise of 0.54 μV_{RMS} was measured across a BW spanning from 0.5 Hz to 40 Hz.

Acknowledgements

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