

Write Voltage Optimization to Increase Flash Lifetime in a Two-Variance Gaussian Channel

Ava Asmani*, Semira Galijasevic*, Richard D. Wesel

Department of Electrical and Computer Engineering

University of California, Los Angeles

Email: {ava24, semiragali, wesel}@ucla.edu

Abstract—For a two-variance model of the Flash read channel that degrades as a function of the number of program/erase cycles, this paper demonstrates that selecting write voltages to maximize the minimum page mutual information (MI) can increase device lifetime. In multi-level cell (MLC) Flash memory, one of four voltage levels is written to each cell, according to the values of the most-significant bit (MSB) page and the least-significant bit (LSB) page. In our model, each voltage level is then distorted by signal-dependent additive Gaussian noise that approximates the Flash read channel. When performing an initial read of a page in MLC flash, one (for LSB) or two (for MSB) bits of information are read for each cell of the page. If LDPC decoding fails after the initial read, then an enhanced-precision read is performed. This paper shows that jointly designing write voltage levels and read thresholds to maximize the minimum MI between a page and its associated initial or enhanced-precision read bits can improve LDPC decoding performance.

Index Terms—mutual information maximization, Flash memory, low-density parity-check code, enhanced precision, progressive reads

I. INTRODUCTION

A. Background

Flash memory is among the most widely utilized data storage technologies in electronic devices. Techniques that prolong reliable Flash memory performance are therefore worthy of study in response to rapidly increasing data storage demands.

Programming requires applying charge to the Flash cell to set the voltage level, or write voltage, at which current will flow. Each Multi-Level Cell (MLC) has four possible write voltages, one for each two-bit input. Each bit maps to a different page in the Flash cell [1]. Data is read through the application of various voltages or read thresholds on the gate to sense the presence or absence of current [2].

One iteration of programming, reading and erasing data is referred to as a Program and Erase Cycle or P/E Cycle. As the number of P/E Cycles of a device increases, the device becomes less reliable until the frame error rate (FER) becomes too high, indicating the end of its useful lifetime [3]. Sources of distortion in the Flash read channel include programming noise, cell-to-cell interference, and charge leakage induced by device wear-out [4]. Therefore, this research strives to find

proper write voltage levels and read thresholds that minimize degradation of the device, subject to noise of the cell, while still allowing for successful memory storage.

For a specified LDPC code rate such as 8/9, when the mutual information (MI) between the write voltage and the bits read from the Flash read channel falls below the LDPC code rate, page failure is unavoidable. Wong et al. [5] optimizes initial and enhanced precision read thresholds by maximizing the MI between the input and output of the Flash read channel. However, in [5], the most-significant bit (MSB) page fails about 250 P/E cycles before the least-significant bit (LSB) page for the same precision level. Wong et al. also does not explore optimizing write voltage levels.

Researchers have previously explored the benefits of optimizing initial read [6] or write [7] voltage levels using the techniques of maximizing MI as introduced in [8]. [9] proposes a search algorithm of write level optimization to minimize error probability in multilevel coding and bit-interleaved coded modulation (BICM). In [10], voltage level optimization is performed to accomplish minimizing the overall bit-error rate (BER) and equalizing page BERs. Both [9] and [10] consider hard decoding reads without analyzing the benefits of optimizing enhanced precision thresholds, write voltages and hard read thresholds simultaneously. Optimization of both read and write voltage levels is explored in [11] and [12]. In [11] write voltages are optimized such that the overall probability of error is minimized, while read thresholds are optimized for maximizing total MI in the same manner as [8], but with a different Flash channel model. In both papers optimization techniques are not compatible with practical Flash memory coding structure where each page is encoded independently.

This paper uses MI maximization to jointly optimize write voltages and read thresholds in the context of practical Flash memories, which use equally-sized pages, encode each bit of a cell into a distinct page, and use progressive reads with enhanced precision to decode pages when the initial read fails. To maximize the Flash lifetime, we seek to equalize the performance of the pages associated with different bits as in, e.g., [9], [10]. Since data is written before the controller knows whether enhanced precision is needed, the same write voltages must be used for both initial reads and the progressive reads. Therefore, a choice must be made between selecting the write voltages that optimize the performance of the initial read or the enhanced reads.

This research is supported by National Science Foundation (NSF) grants CCF-1911166 and CCF-1955660. Any opinions, findings, and conclusions or recommendations expressed in this material are those of the author(s) and do not necessarily reflect views of NSF.

* The first two authors contributed equally to this work.

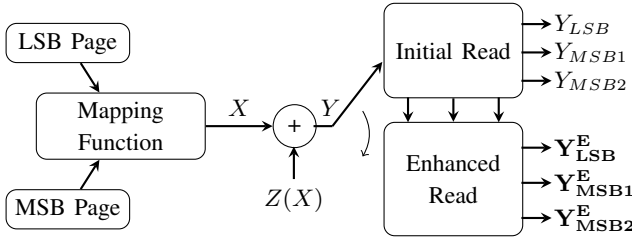


Fig. 1. Flash system model with initial and enhanced precision reads.

Thus, we consider jointly optimizing write voltages and read thresholds to maximize three distinct MIs. One approach is to select the write voltages and read thresholds to maximize minimum page MI between the page bit and the initial reads. This is the scenario of [9], [10], although those papers minimize bit error rate rather than maximize MI. Our second approach jointly optimizes the write voltage levels, initial read thresholds, and enhanced precision read thresholds to maximize minimum page MI between the page bit and all receiver information available after the enhanced precision read. Our third approach optimizes write voltages for the limiting case of enhanced precision where full “soft” information is available, i.e. controller learns the exact voltage where current begins to flow, as in [13].

B. Contributions

The main contributions of this paper are as follows:

- This paper compares three approaches to optimizing write voltage levels, maximizing the minimum of a specific MI 1) the MI for the initial read or 2) the MI after with enhanced precision or 3) the soft MI. The minimum MI for the initial read provided the best overall performance for the channel studied.
- Among these three choices, information theoretic analysis and LDPC simulations show that maximizing the minimum MI for the initial read seems to be preferable for increasing the lifetime in P/E cycles until the LDPC frame error rate (FER) exceeds 10^{-6} .

C. Organization

The remainder of this paper is organized as follows. Sec. II discusses the model of the Flash read channel. Sec. III summarizes the optimization of read thresholds for the initial read and for enhanced-precision to maximize the MI between the channel input and the specific outputs of that read operation. Sec. IV describes the joint optimization of write voltages and read thresholds to maximize one of three distinct MIs. Sec. V compares the three proposed approaches of Sec. IV to the write voltages and read thresholds used by [5]. Sec. VI presents the FER performance of LDPC simulations using the original write voltages of [5] and write voltages of each optimization technique. Sec. VII concludes the paper.

II. FLASH CHANNEL MODEL

Following [5], Fig. 1 shows the system model and read channel where the bits of the LSB and MSB page induce

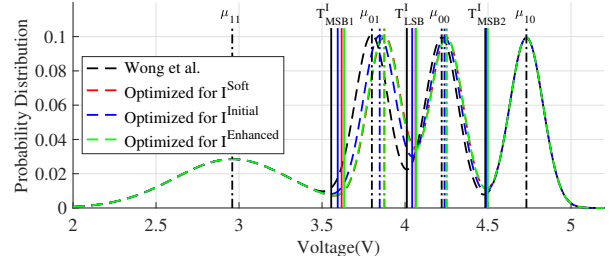


Fig. 2. Flash model at 1600 P/E Cycles. Enhanced precision read thresholds would be placed to the left and right of each initial read threshold T_{MSB1}^I , T_{LSB}^I and T_{MSB2}^I . Solid lines represent initial read thresholds and dotted-dashed lines represent write voltages μ_{11} , μ_{01} , μ_{00} and μ_{10} .

the written voltage X , which is distorted by signal-dependent Gaussian noise $Z(X)$ to produce Y . As in [5], $Z(X)$ is approximated by a Gaussian distribution with two possible variances. Following the general behavior of Flash cells, the lowest value of X corresponding to an un-programmed cell has the larger variance and the noise for all of the other cells has the smaller variance because the feedback loop associated with programming reduces certain distortions. Note that the mean of $Z(X)$ is not X because there are distortions such as retention loss and read disturb that shift the mean in addition to distortions that add variance [1].

As shown in Fig. 1, the initial read for the LSB page produces the bit Y_{LSB} . For the MSB page, the initial read produces two bits Y_{MSB1} and Y_{MSB2} . Y_{LSB} , Y_{MSB1} and Y_{MSB2} represents whether the output voltage Y is above or below the initial read thresholds T_{LSB} , T_{MSB1} and T_{MSB2} , respectively. If the LDPC decoder fails to find a valid code-word with the initial read, an enhanced precision read provides additional bits. The enhanced read produces the variables Y_{LSB}^E , Y_{MSB1}^E and Y_{MSB2}^E which are each vectors of two variables representing whether the real number output voltage Y is above or below the enhanced precision read thresholds placed to the left and right of each initial read threshold.

Fig. 2 shows an example of the two-variance Gaussian model for an MLC at 1600 P/E cycles. The means of the middle two means or write voltages and initial read thresholds are placed four ways. One way is according to [5], which is considered as a baseline. The three new placements are according to the three optimization objectives described later in this paper. The means and variances used in [5] for each multiple of 100 P/E cycles can be found in [14]. As the number of P/E cycles increase, retention losses causes the spacing between the input means to decrease and the variance of the programmed levels to increase.

III. READ THRESHOLD OPTIMIZATION

Wong et al. [5] optimized initial read thresholds T_{LSB}^I and $\mathbf{T}_{MSB}^I$ (a vector containing T_{MSB1}^I and T_{MSB2}^I) as a function of the means and variances of the two-variance Gaussian channel, according to the following two optimizations:

$$\max_{\{T_{LSB}^I\}} I_{LSB}^I \quad \text{and} \quad \max_{\{\mathbf{T}_{MSB}^I\}} I_{MSB}^I, \quad \text{with} \quad (1)$$

$I_{LSB}^I = I(X_{LSB}; Y_{LSB}^I)$ and $I_{MSB}^I = I(X_{MSB}; \mathbf{Y}_{MSB}^I)$, where X_{LSB} and X_{MSB} are the two input bits, one for the LSB page and one for the MSB page using this MLC Flash cell. $\mathbf{Y}_{MSB}^I$ is a vector containing Y_{MSB1}^I and Y_{MSB2}^I . As observed in [5], since T_{LSB}^I affects only Y_{LSB}^I and not $\mathbf{Y}_{MSB}^I$ and conversely $\mathbf{T}_{MSB}^I$ affects only $\mathbf{Y}_{MSB}^I$ and not Y_{LSB}^I , maximizing I_{LSB}^I and I_{MSB}^I are independent optimizations when the write voltages are assumed to be fixed and not included in the optimization.

Enhanced precision read thresholds $\mathbf{T}_{LSB}^E$ (a vector containing T_{LSB}^{left} and T_{LSB}^{right}) and similarly defined vectors $\mathbf{T}_{MSB1}^E$ and $\mathbf{T}_{MSB2}^E$ are found by solving the following two optimization problems

$$\max_{\{\mathbf{T}_{LSB}^E\}} I_{LSB}^E \quad \text{and} \quad \max_{\{\mathbf{T}_{MSB1}^E, \mathbf{T}_{MSB2}^E\}} I_{MSB}^E, \quad \text{with} \quad (2)$$

$I_{LSB}^E = I(X_{LSB}; Y_{LSB}^E, \mathbf{Y}_{LSB}^E)$ and $I_{MSB}^E = I(X_{MSB}; \mathbf{Y}_{MSB}^E, \mathbf{Y}_{MSB1}^E, \mathbf{Y}_{MSB2}^E)$. $\mathbf{Y}_{LSB}^E$ is a vector containing Y_{LSB}^{left} and Y_{LSB}^{right} . $\mathbf{Y}_{MSB1}^E$ and $\mathbf{Y}_{MSB2}^E$ are similarly defined vectors. As with the initial reads, the I_{LSB}^E and I_{MSB}^E calculations for the enhanced reads are independent optimizations when the write voltages are assumed to be fixed and not included in the optimization. In [5], enhanced precision read thresholds are chosen after initial read thresholds are found according to Equation 1.

IV. WRITE VOLTAGE LEVELS THAT OPTIMIZE PAGE MI

For MLC Flash, there are four voltage levels, which we will refer to according to the two-bit input label that is associated with each level. Looking again at Fig. 2, the write voltages from left to right are μ_{11} , μ_{01} , μ_{00} , and μ_{10} .

In this paper, the write voltages are assumed to completely determine the means of the Gaussian distributions observed during the read operation. In practice charge retention issues and read-disturb in real Flash memory systems cause the means of the read distributions to vary from the voltages written to the device [1]. Our optimization methods can easily incorporate a known relationship between the write voltage and the mean of the read distribution.

This section describes three techniques, with each technique maximizing the minimum of a specific page MI. We assume that the erased state mean μ_{11} cannot be changed by the controller. Similarly, we assume that the rightmost mean μ_{10} is already maximized and would not be further adjusted by the controller. Thus, our optimization only modifies the middle two write voltage levels, μ_{01} and μ_{00} .

All three optimization objectives explored in this paper are solved in MATLAB using `fminsearchcon` function [15] which utilizes the Nelder-Mead Simplex Method to perform a direct search over multidimensional space. When using the `fminsearchcon` function to maximize the minimum of I^{Soft} , the write voltages are initialized to those found in [14].

A. Maximizing Minimum of $I^{Initial}$ for LSB and MSB

The first technique jointly optimizes the write voltage levels μ_{01} , μ_{00} and all initial read thresholds to maximize the minimum page MI for the initial read. Since the write voltage

levels are deterministic of both I_{LSB}^I and I_{MSB}^I a joint optimization is required as follows:

$$\max_{\{T_{LSB}^I, \mathbf{T}_{MSB}^I, \mu_{01}, \mu_{00}\}} \min(I_{LSB}^I, I_{MSB}^I), \quad (3)$$

I_{LSB}^I and I_{MSB}^I MIs are $I^{Initial}$. The optimization is initialized with the write voltage levels and initial read thresholds found to optimize I^{Soft} described below. Enhanced precision read thresholds for this optimization objective are found by applying the optimized write voltages and initial read thresholds to Eqn. 2.

B. Maximizing Minimum of $I^{Enhanced}$ for LSB and MSB

The second technique jointly optimizes the write voltage levels μ_{01} , μ_{00} , the initial read thresholds and the enhanced precision read thresholds to maximize the minimum page MI for the enhanced read. Since the write voltage levels are deterministic of both I_{LSB}^E and I_{MSB}^E , a joint optimization is required as follows:

$$\max_{\{T_{LSB}^I, \mathbf{T}_{MSB}^I, \mathbf{T}_{LSB}^E, \mathbf{T}_{MSB1}^E, \mathbf{T}_{MSB2}^E, \mu_{01}, \mu_{00}\}} \min(I_{LSB}^E, I_{MSB}^E), \quad (4)$$

I_{LSB}^E and I_{MSB}^E are considered $I^{Enhanced}$. The optimization is initialized with the write voltage levels, initial and enhanced precision read thresholds found to optimize I^{Soft} described below.

C. Maximizing Minimum of I^{Soft} for LSB and MSB pages

The third technique finds write voltages that maximize the page MIs $I(X_{MSB}; Y)$ and $I(X_{LSB}; Y)$ where Y is the real number output voltage of the Flash read channel. These MIs are considered I^{Soft} because they utilize the soft output Y . Write voltages are deterministic of both $I(X_{MSB}; Y)$ and $I(X_{LSB}; Y)$, so they must be jointly optimized. When performing the optimization to find the minimum page MI of I^{Soft} , the write voltages are initialized to those found in [14]. Initial read thresholds and enhanced precision read thresholds for this optimization objective are found by applying these write voltages to Eqn. 1 and Eqn. 2, respectively. Methods outlined in methods [4] and [16] allow the realization of the variances and means of the erase state and highest voltage input of the Flash device every 100 P/E cycles. Optimized thresholds and write voltages found using methods outlined in this paper can then be pulled from a lookup table formulated offline. Learning the parameters of the Flash channel has been researched extensively to allow novel optimization techniques, like the one presented in this research, to extend the lifetime of Flash memory devices.

V. PAGE MI VS. P/E CYCLES FOR THREE OBJECTIVES

A. Comparing Performance for $I^{Initial}$ vs. P/E Cycles

$I^{Initial}$ is the MI between the output found from the initial reads and the LSB or MSB page input. Fig. 3 shows plots of $I^{Initial}$ for each page calculated with the voltage levels and initial read thresholds from [5] and each of the three optimization objectives.

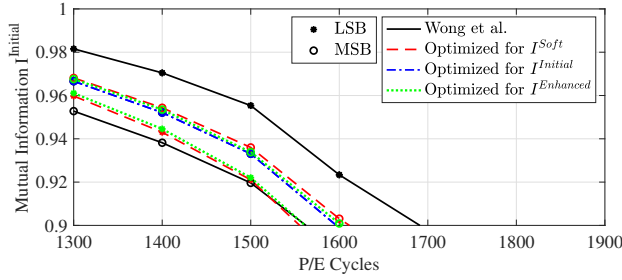


Fig. 3. Plot of $I^{Initial}$ vs P/E Cycle for the MSB and LSB for each optimization technique and original mean voltages and initial read thresholds from Wong et al.

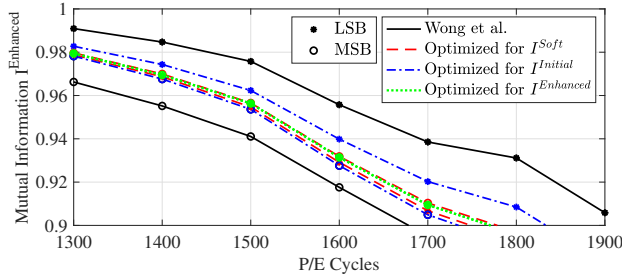


Fig. 4. Plot of $I^{Enhanced}$ vs P/E Cycle for the MSB and LSB for each optimization technique and original mean voltages and initial read thresholds from Wong et al.

For the mean voltages optimized to maximize $I^{Initial}$, the MSB and LSB page fail (have an MI below 0.9) simultaneously at 1590 P/E cycles. Thus, mean voltages optimized for $I^{Initial}$ increase the initial-read lifetime of the device by around 40 P/E Cycles compared to values from [5]. Operating the Flash device with mean voltages and initial read thresholds optimized for $I^{Enhanced}$ leads to a similar initial-read lifetime as using values from [5]. Mean voltages optimized for I^{Soft} decreases the initial-read lifetime of the device by around 7 P/E cycles.

B. Comparing Performance for $I^{Enhanced}$ vs. P/E Cycles

$I^{Enhanced}$ measures the MI between the output bits produced by the initial and enhanced reads and the LSB or MSB of the input. Fig. 4 shows the values of $I^{Enhanced}$ for each page calculated using the write voltages, initial read thresholds and enhanced precision thresholds from [5] and each of the three optimization objectives.

The mean voltages optimized for $I^{Enhanced}$ the MSB and LSB page fail simultaneously at about 1767 P/E cycles, increasing the Flash memory's enhanced-read lifetime by around 90 P/E cycles compared to the original mean voltages and initial read thresholds from Wong et al. The mean voltages optimized for $I^{Initial}$ and I^{Soft} have slightly worse initial-read lifetimes than the mean voltages optimized for $I^{Enhanced}$, but both increase the Flash memory's enhanced-read lifetime significantly as compared to the original mean voltages from Wong et al.

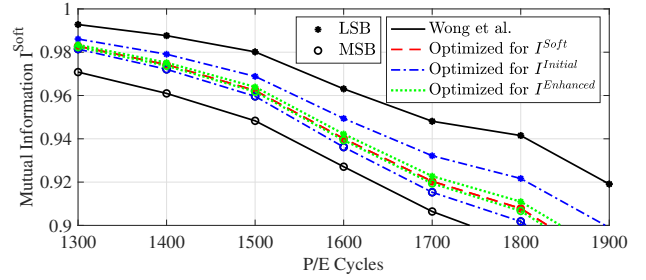


Fig. 5. Plot of I^{Soft} vs P/E Cycles for the MSB and LSB for each optimization technique and original mean voltages and initial read thresholds from Wong et al.

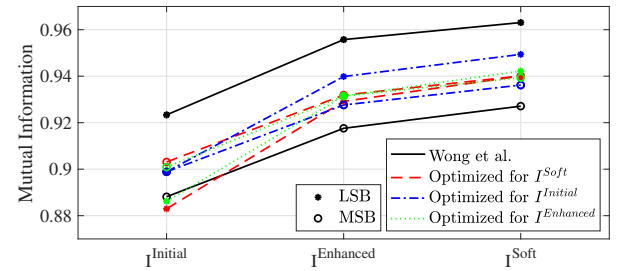


Fig. 6. Comparison of three MI measures for all sets of means and thresholds at 1600 P/E Cycles

C. Comparing Performance for I^{Soft} vs. P/E Cycles

I^{Soft} calculates the amount of information the real number output voltage reveals about the binary input LSB or MSB. Fig. 5 shows I^{Soft} of each page calculated using the write voltages from [5] and each of the three optimization objectives.

Write voltage levels optimized for a real number output lengthen Flash memory lifetime by approximately 90 P/E Cycles compared to the lifetime with the original means of [5] and provides the greatest lifetime change of all three optimization methods. However, practical Flash devices do not have access to the real valued voltage Y . Instead, they must decode the page data using only a few bits of information about Y obtained by comparing Y with various read thresholds.

Fig. 6 shows the values $I^{Initial}$, $I^{Enhanced}$, and I^{Soft} at 1600 P/E cycles for all four ways of selecting the mean voltages. The lifetime of the flash device is determined by the page with the shortest lifetime. While the MSB page lifetime decreases for all optimization techniques as compared to [5], the LSB page lifetime is increased so the lifetime of the device with optimized write voltages is increased. For each of the three possible MIs $I^{Initial}$, $I^{Enhanced}$, and I^{Soft} , the mean voltages optimized to maximize the minimum of that MI result in the MSB and LSB page MIs of that type being essentially identical. The mean voltages optimized for other MIs have a lower minimum page MI. Figs. 3, 4, 5, and 6 reveal that parameters optimized to maximize one MI do not generate optimal results for other MIs.

Write voltages are selected before knowing whether the initial read or the enhanced read will be required for LDPC

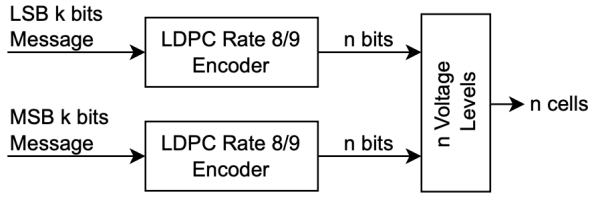


Fig. 7. Block diagram of independent encoding of MSB and LSB pages.

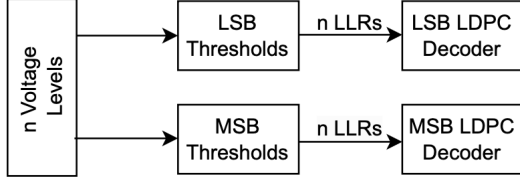


Fig. 8. Block diagram of independent decoding of MSB and LSB pages.

decoding. One optimization approach must be picked. Since I^{Soft} is not practically relevant, let's focus attention on $I^{Initial}$ and $I^{Enhanced}$. Looking at $I^{Initial}$ in Fig. 6, the performance of the means optimized for $I^{Enhanced}$ is significantly worse than the performance of the means optimized for $I^{Initial}$. In contrast, looking at $I^{Enhanced}$ in Fig. 6, the means optimized for $I^{Initial}$ perform only slightly worse than the means optimized for $I^{Enhanced}$. Thus, for the channel studied, the MI results indicate that the best overall performance will be obtained by using $I^{Initial}$ to optimize the write voltages. This will give the absolute best performance on the initial read and the performance for the enhanced read will be almost as good as having optimized specifically for that case.

VI. PERFORMANCE WITH LDPC CODES

A. Independent Encoding and Decoding Procedure

A protograph-based low-density parity check (LDPC) code [17] of rate 8/9 encoding 14,400 message bits into 16,200 codeword bits is used to simulate frame error rates (FERs) for initial and enhanced read decoding. Fig. 7 illustrates that two independent k -bit messages, each for the LSB and MSB pages, are encoded into two separate codewords of n bits, which are then combined and mapped to n voltage levels. The decoder in Fig. 8 uses the n voltage levels to determine the log-likelihood ratio (LLR) for each page independently in accordance with the thresholds. For initial read decoding, Y_{LSB}^I will produce two LLR regions for the LSB page, while Y_{MSB}^I produce three LLR regions for the MSB page. For enhanced-read decoding, Y_{LSB}^I and Y_{LSB}^E will produce four LLR regions for the LSB page, while Y_{MSB}^I , Y_{MSB2}^E and Y_{MSB1}^E will result in seven LLR regions for the MSB page.

B. LDPC Simulations Results

Fig. 9 shows initial read decoding FER vs. P/E cycles for simulations obtained using optimized mean voltages and initial-read thresholds for $I^{Initial}$ and $I^{Enhanced}$ and FER curves obtained using original mean voltages and initial read

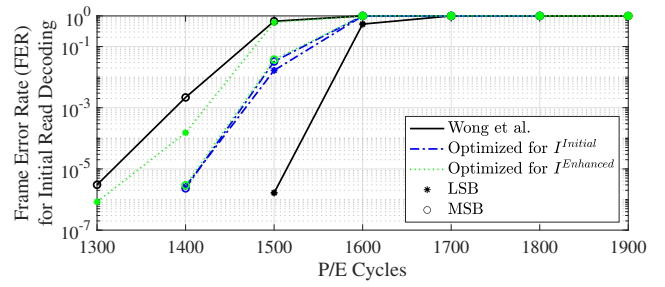


Fig. 9. FER vs. P/E Cycles for initial read decoding of MSB and LSB pages.

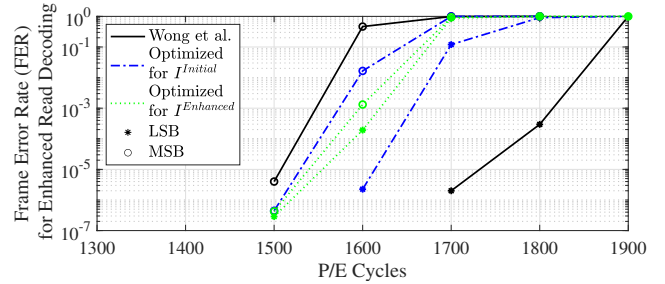


Fig. 10. FER vs. P/E Cycles for enhanced precision decoding.

thresholds from Wong et al. Construing lifetime as when FER of either MSB or LSB page exceeds 10^{-6} , the initial-read lifetime for mean voltages optimized for $I^{Initial}$ is about 1400 P/E cycles, offering a 100 P/E cycle improvement over the means used in Wong et al. [5]. Initial-read lifetime for mean voltages optimized for $I^{Enhanced}$ is about 1300 P/E cycles, slightly better than the means used in Wong et al. [5]. Consistent with Fig. 3, the FER performance for both MSB and LSB pages is similar for the means optimized for $I^{Initial}$.

Fig. 10 shows enhanced-read-decoding FER vs. P/E cycles for simulations obtained using the various mean voltages. Construing lifetime as when FER of either page exceeds 10^{-6} , the enhanced-read lifetime for mean voltages optimized either for $I^{Initial}$ and for $I^{Enhanced}$ is about 1510 P/E cycles, improving the lifetime over means used in Wong et al. [5]. Consistent with Fig. 4, FER performance for both MSB and LSB pages is similar for the means optimized for $I^{Initial}$.

VII. CONCLUSION

This research demonstrates the additional benefits to Flash memory lifetime that can be achieved by optimizing write voltage levels and thresholds for Flash memory with progressive reads. Optimizing $I^{Initial}$, i.e. for initial-read performance, was the most effective method of maximizing the minimum MI of the MSB and LSB pages in terms of increasing lifetime, whether lifetime is construed as the number of P/E cycles until the MI of a page fell below 0.9 or until the FER of a page rose above 10^{-6} . LDPC simulations showed a strong correlation between MI and LDPC FER performance, confirming that selecting mean voltages to maximize the minimum MI of a page also obtains mean voltages that achieve similar FER performance, and thus extended device lifetime.

REFERENCES

- [1] Y. Cai, Y. Luo, E. F. Haratsch, K. Mai, and O. Mutlu, "Data retention in mlc nand flash memory: Characterization, optimization, and recovery," in *2015 IEEE 21st International Symposium on High Performance Computer Architecture (HPCA)*, 2015, pp. 551–563.
- [2] R. Bez, E. Camerlenghi, A. Modelli, and A. Visconti, "Introduction to flash memory," *Proceedings of the IEEE*, vol. 91, no. 4, pp. 489–502, 2003.
- [3] Q. Li, A. Jiang, and E. F. Haratsch, "Noise modeling and capacity analysis for nand flash memories," in *2014 IEEE International Symposium on Information Theory*, 2014, pp. 2262–2266.
- [4] H. Wang, N. Wong, T.-Y. Chen, and R. D. Wesel, "Using dynamic allocation of write voltage to extend flash memory lifetime," *IEEE Transactions on Communications*, vol. 64, no. 11, pp. 4474–4486, 2016.
- [5] N. Wong, E. Liang, H. Wang, S. V. S. Ranganathan, and R. D. Wesel, "Decoding flash memory with progressive reads and independent vs. joint encoding of bits in a cell," in *2019 IEEE Global Communications Conference (GLOBECOM)*, 2019, pp. 1–6.
- [6] Y. Yeh, A. Fazeli, and P. H. Siegel, "Optimal placement of read thresholds for coded nand flash memory," in *ICC 2021 - IEEE International Conference on Communications*, 2021, pp. 1–7.
- [7] C. Duangthong, W. Phakphisut, and P. Supnithi, "Capacity enhancement of asymmetric multi-level cell (mlc) nand flash memory using write voltage optimization," in *2019 34th International Technical Conference on Circuits/Systems, Computers and Communications (ITC-CSCC)*, 2019, pp. 1–4.
- [8] J. Wang, T. Courtade, H. Shankar, and R. D. Wesel, "Soft information for ldpc decoding in flash: Mutual-information optimized quantization," in *2011 IEEE Global Telecommunications Conference - GLOBECOM 2011*, 2011, pp. 1–6.
- [9] C. Duangthong, W. Phakphisut, and P. Supnithi, "Search algorithm of write voltage optimization in nand flash memory," in *2017 International Electrical Engineering Congress (iEECON)*, 2017, pp. 1–4.
- [10] Y. Kim, J. Kim, J. J. Kong, B. V. K. V. Kumar, and X. Li1, "Verify level control criteria for multi-level cell flash memories and their applications," in *EURASIP J. Adv. Signal Process*, no. 196, 2012.
- [11] C. A. Aslam, Y. L. Guan, and K. Cai, "Dynamic write-level and read-level signal design for mlc nand flash memory," in *2014 9th International Symposium on Communication Systems, Networks Digital Sign (CSNDSP)*, 2014, pp. 336–341.
- [12] —, "Read and write voltage signal optimization for multi-level-cell (mlc) nand flash memory," *IEEE Transactions on Communications*, vol. 64, no. 4, pp. 1613–1623, 2016.
- [13] S. Galijasevic and R. D. Wesel, "Optimizing write voltages for independent, equal-rate pages in flash memory," in *2022 56th Asilomar Conference on Signals, Systems, and Computers*, 2022, pp. 168–174.
- [14] H. Wang. Flash model: mean and standard deviation. [Online]. Available: <http://www.seas.ucla.edu/csl/codes/enhnPrecisionMuSigma.txt>
- [15] J. D'Errico. fminsearchbnd, fminsearchcon. [Online]. Available: <https://www.mathworks.com/matlabcentral/fileexchange/8277-fminsearchbnd-fminsearchcon>
- [16] W. Sun and J. Zheng, "A low-complexity retention noise parameter estimation for mlc nand flash memory," in *ICC 2019 - 2019 IEEE International Conference on Communications (ICC)*, 2019, pp. 1–6.
- [17] S. V. S. Ranganathan. Flash LDPC code: rate 8/9. [Online]. Available: http://www.seas.ucla.edu/csl/codes/Flash_Rate_8_9_LDPC.txt