A Scalable, Binary Phase, Millimeter-Wave Reconfigurable Intelligent Surface

Aditya S. Shekhawat, Bharath G. Kashyap, Russell W. Raldiris Torres, Georgios C. Trichopoulos
ECEE, Arizona State University, USA
{aditya.shekhawat, bharath.kashyap, rraldiri, gtrichop}@asu.edu

***Abstract*—We present a 1-bit reconfigurable intelligent surface (RIS) operating at millimeter-waves (mmWaves) that employs a 2.5D integration topology for size scalability and a randomized phase delay pattern to suppress quantization lobes. As opposed to fixed beam metasurfaces, RISs require a biasing and control circuitry to excite the necessary phase shift distribution across the aperture. Additionally, binary phase RISs result in coarse phase modulation and require additional transmission lines within every unit cell to mitigate the quantization lobes. The proposed RIS topology features a tiled topology that includes the radiating elements, phase shifters, delay lines, shift registers, and necessary connectors to interface with the control board. We present a RIS tile comprising 64 elements arranged in a 16×16 array and a control board to house the control unit, RIS tiles, and power supply. The prototype tile is designed to operate at 28 GHz with electronic beam-steering in both azimuth and elevation planes. It is fabricated using printed circuit board (PCB) technology and characterized using a mmWave radar cross section (RCS) measurement setup. The proposed architecture can be utilized to realize arbitrary large apertures and helps achieve quantization lobe reduction of more than 10 dB.**

***Keywords*—5G communications, metasurface, beam steering, millimeter waves.**

I. Introduction

Except for the sub-6GHz bands, 5G and futureG wireless communications rely on millimeter-wave (mmWave) frequencies to achieve higher data rates, extend broadband internet to a larger portion of the population, and potentially perform new promising applications and services that combine the synergy of sensing and communications. However, the effort to achieve practical coverage of mmWave signals stumbles on the unfavorable propagation characteristics of higher frequency electromagnetic wave (EM) waves. mmWaves cover much shorter distances than the sub-6GHz signals due to absorption and/or strong scattering from most materials in a typical communication channel. As such, it is prevalent for the user equipment (UE) to receive unacceptably low signal-to-noise (SNR) signals or experience no coverage at all. Densifying the base station (BS) network is an approach that could improve signal coverage but will come at a substantial capital expenditure due to the costs associated with the hardware, real-estate acquisition, installation, and maintenance of such complicated systems.

Alternatively, reconfigurable intelligent surfaces (RISs) could provide a solution to the mmWave coverage challenges [1]-[2]. RISs are low-cost, low-profile planar devices capable of redirecting incident mmWave to a desirable direction(s)

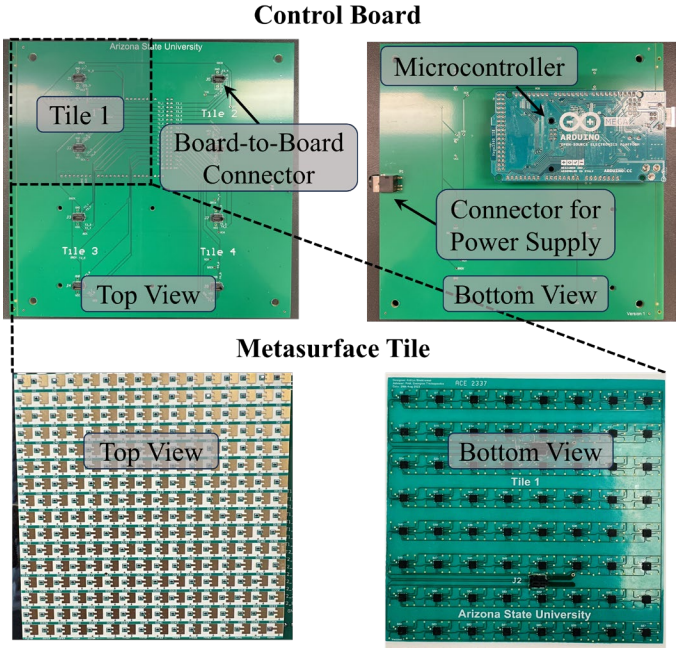

Fig. 1. mmWave RIS prototype consisting of the control board (top) and 16×16 1-bit metasurface tiles (bottom).

without the need of generating an RF power (passive), thus being potentially ultra-low power systems. Hence, RISs can be considered "smart mirrors," enabling anomalous reflections instead of natural specular reflections. By placing RISs in strategic locations, additional propagation paths are provided, covering non-line-of-sight (NLoS) areas and/or improving the SNR. Besides improving or extending the signal coverage, RISs can modulate the channel to provide increased security on the physical layer or leverage electronic beamforming for sensing applications. Nevertheless, one of the key advantages of RISs is the inherent scalability of the topology to electrically large apertures that can provide the desired benefits of signal gain and narrow beams. However, scalability can be practically limited by the complexity of the biasing and control circuits, among other potential factors.

A RIS is a metasurface with hundreds or thousands of subwavelength radiating elements. Each element is integrated with phase shifters (such as radio-frequency (RF) PIN diodes, MEMs, varactors, etc.) that can modulate the phase and/or amplitude of incident wavefronts, allowing the reflected waves to be redirected to desirable directions. Although multi-bit phase shifters or varactors can provide fine phase control, both approaches face challenges with respect to circuit

2024 IEEE/MTT-S International Microwave Symposium - IMS 2024 | 979-8-3503-7504-6/24/$31.00 ©2024 IEEE | DOI: 10.1109/IMS40175.2024.10600436

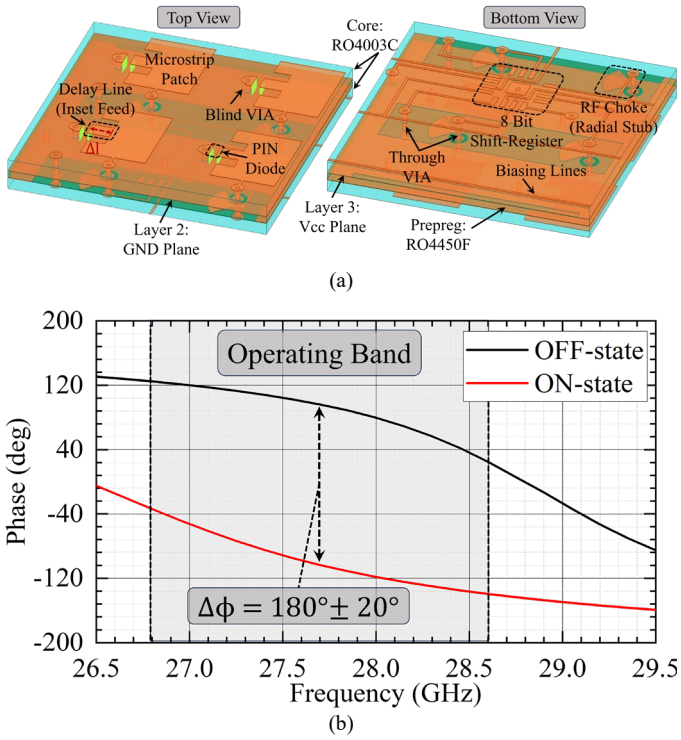

Fig. 2. mmWave compact super-cell design (a) 3D top and bottom view, depicting various layers, RF elements, and footprints for DC components; (b) Simulated results using an electromagnetic solver (ANSYS HFSS): reflection phase vs frequency for both ON and OFF state.

complexity, power consumption, size, and losses at mmWave frequencies. On the other hand, these phase shifters require biasing circuitry and the use of a field-programmable gate array (FPGA) or microcontroller unit (MCU) with several channels to drive them. As such, realizing 1-bit quantization onto RIS for beamforming applications is highly preferred due to its simplified topology.

Furthermore, there has been limited published literature on practical designs and experimental demonstrations of the RIS, especially in the mmWave bands. Most of the experimental studies have been carried out in the sub-6 GHz band [3]-[6] and others around 10 GHz [7]-[8] and very few at mmWave [9]-[12]. Most of them exhibit limited scalability since either the electronic beamforming is implemented in a single plane (azimuth) as observed in [3], [6], and [7] or the aperture size is limited by the finite number of biasing lines which can be accommodated on the surface. The latter is because current topologies are mostly planar (2D) and routing a larger number of biasing lines would require additional PCB layers, which can be costly and impractical. Additionally, such an approach results in a more rigid design with less flexibility. Using a tiled architecture provides a modular design approach, resulting in a cost-effective topology when large surfaces are needed. A scalable, power-efficient, and easily fabricable control topology is attractive to control the phase shifters in single/multi-bit RISs. Accordingly, we have introduced a new topology in this work, which only requires strategic placements of the low-power series-in and parallel-out shift register (SR) ICs while the control board can be stacked at a

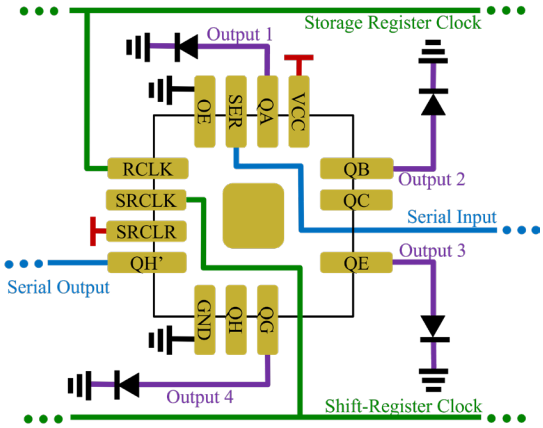

Fig. 3. The biasing circuitry schematic of the supercell: an 8-bit SR is connected to four unit cells and other SRs in series. 4 more bits are available in every supercell which can be used in future designs for dual polarization RISs or 2-bit phase control.

different layer (2.5D integration). Therefore, making it a compact solution to realize large apertures with no added complexity which can also benefit higher frequency and multi-bit architectures.

One of the other limitations of the existing RIS designs implementing binary phase modulation is the quantization (grating) lobe, which arises due to the periodicity in the phase quantization error when illuminated with a plane wave [13]. For the first time, in this work, a compact single-bit element design that uses a phase randomization technique introduced in [13] is adopted to suppress the undesired quantization lobes in electronic beam scanning. A prototype is designed at 28 GHz utilizing the proposed element and fabricated using the PCB technology, as shown in Fig. 1.

II. Reconfigurable Intelligent Surface Tile Design

The RIS tile comprises 256 (16 × 16) unit cells that contain a resonant microstrip patch (radiating element), an inset feed (delay line), and a mmWave PIN diode (MACOM MA4AGP907) on the top surface. Layer 2 is used as a common ground plane (RF/DC), and layer 3 is a common V_{cc} plane with periodic slots to accommodate the RF choke (λ/4 radial stub). Every RIS tile consists of two Rogers 4003C substrates (ε_r = 3.55 and tanδ = 0.0027) of 0.508mm thickness. The bottom layer consists of biasing components such as shift registers (SRs) and compact connectors to attach to the control board. To minimize the area of the biasing circuitry, we use an 8-bit shift register (SR) integrated circuit (IC) to supply biasing voltage to 4 neighbouring unit cell phase shifters (~3 mA per PIN diode). As such, the 2×2 unit cell topology forms a supercell with an area of λ×λ (wavelength at 28 GHz) that repeats across the RIS tile. Nevertheless, a 16×16 unit cell tile consists of 8×8 supercells which constitutes a computationally large model to analyse. To alleviate this modelling bottleneck, we model the RIS tile in a commercial electromagnetic field solver (ANSYS HFSS) as an infinite periodic array of supercells, which is a common approach in simulating and analysing large antenna arrays as well [14].

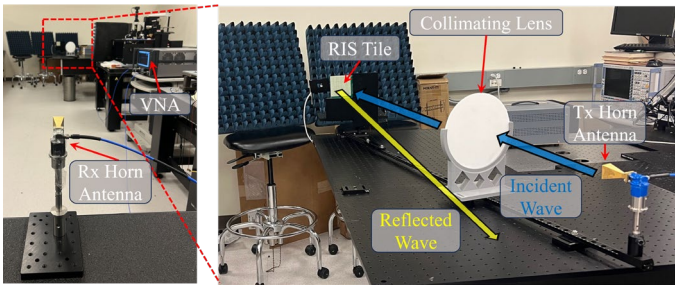

Fig. 4. Measurement setup used to characterize beamforming of the proposed 1-bit mmWave RIS.

The analysis focuses on evaluating the phase and magnitude of the reflected signals and accounts for the intricate multilayer topology of the radiating elements and biasing circuitry. To excite the elements, a Floquet port is used to evaluate the reflected wave's phase and magnitude when all 4 PIN diodes are in state 1, ON (180°), and state 2, OFF (0°). The reflection phase of both states is optimized by tuning the dimensions of the radiating element and feed to achieve the desired 180°±20° phase difference, as shown in Fig. 2b. The ON/OFF states of the switch are implemented using the measured S-parameters from the vendor.

To implement randomization, the pseudorandom phase delays for each unit cell were generated using the equation (1) from [13]. For maximum suppression of the quantization lobe level (QLL), random phase delays from 0°-180° were implemented in unit cells by varying the inset feed length (Δl) (as shown in Fig. 2a). As such, changing the length (Δl) of the delay line from shortest reference length to quarter-wavelength the necessary random phase delays are obtained. The required phase difference between the states is also maintained.

III. RIS Control Circuitry

The control topology is divided into two parts: first, the components required for each RIS tile, and second, the components needed for the control board. Each 16 × 16 RIS tile hosts 256 PIN diodes and 64 serial-in and parallel-out 8-bit SRs. Furthermore, two male micro connectors are placed on the bottom layer for board-to-board attachment. To fit the SR in a supercell, a 16-pin package (SN74HC595BRWN) is used because of the small footprint. Fig. 3 shows the SR footprint and the schematic of the various signals. The input/output pins of the SR are connected to the desired PIN diodes, clock signals, and power planes. Every 8-bit SR can control up to eight PIN diodes, although four are left floating for future use in dual-polarization or 2-bit phase shifter designs.

For the second part, a control board is designed to host components such as a microcontroller (Arduino Mega 2560), female micro board-to-board connectors, and a barrel connector for the external power supply. After the incident and reflection angle are determined, the bitstream is formed in a computer, based on the required quantized phase distribution. Then the microcontroller receives the bitstream and distributes the bits through the SRs to every PIN diode while the clock signals coordinate the bitstream flow.

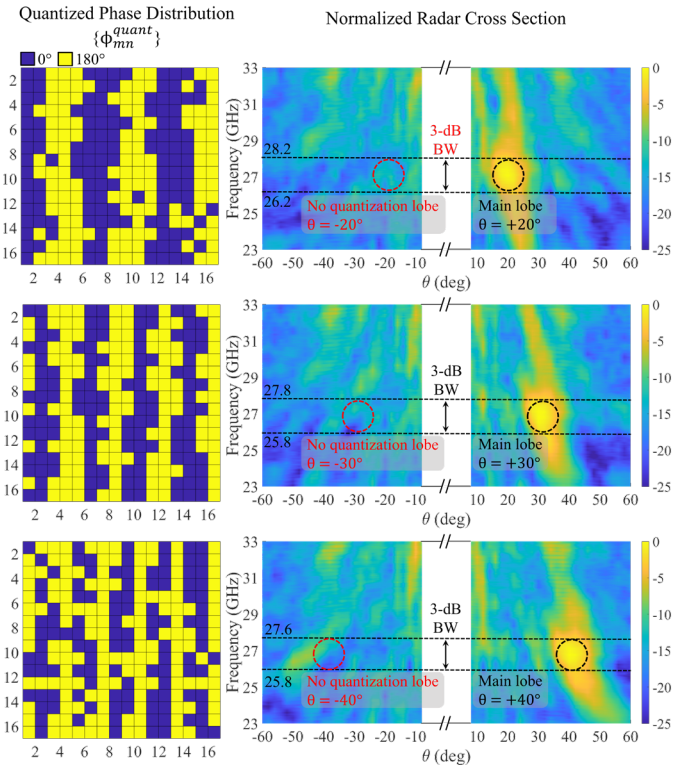

Fig. 5. Quantized phase distribution (left column) and measured normalized RCS pattern (right column) for various steering angles. The patterns were measured for normal incidence θ_i = 0° and reflection angles θ_d = 20°(top), 30°(middle), and 40°(bottom).

Since SRs can be cascaded in a row, arbitrary large RIS can be realized and controlled, albeit at the cost of decreased switching speeds between different phase distributions, as a greater number of SRs will be connected in series. However, the control board can be designed to accommodate any number of 16 × 16 RIS tiles, allowing the realization of large apertures to get higher beamforming gain. This topology is PCB compatible , and components being assembled on the top and bottom layers of the RIS help avoid complex wiring. Due to the simplicity of the biasing circuitry, the RIS operates at a couple of watts, but has the potential to operate at much lower levels if transistor-based switches are used [15]. Additionally, the topology can be scaled to higher frequency and multi-bit/dual-pol architectures.

IV. RIS Characterization

A. Measurement Quasioptical Setup

A quasioptical measurement setup is used to measure the bistatic RCS of the fabricated RIS prototype. The goal of this step is to emulate far-field conditions that are expected in a real-world wireless communications scenario where the RIS is illuminated by a plane wave. To achieve that, we employ a quasioptical setup where a transmitting horn antenna is feeding a large Teflon lens to create a collimating beam, thus approximating a plane wave across the RIS tile aperture, as shown in Fig. 4. Additionally, the quasioptical setup allows for limited overspill around the tile aperture that could interfere with the RCS measurement. Then a receiving horn

antenna is placed 5m away from the RIS tile to capture the scattered far-fields. The transmit and receive antennas are connected to the respective ports of a vector network analyser (VNA), and the measured coupled signal (e.g., S_{21}) is proportional to the RCS of the RIS tile. The RIS under test, the lens, and the transmitting horn are all mounted on an optical breadboard, which helps keep the measurement setup stable to provide accuracy and repeatability. As such, the transmitter is rotated radially around the center of the RIS from [-10°, -60°] to [+10°, +60°]. The scan angle range is limited due to the geometrical limitation of the setup (blockage from the lens).

B. Measured Radar Cross Section

The measured normalized RCS patterns of the RIS tile for normal incidence and various angles of reflections (θ_d = 20°, 30°, and 40°) are shown in Fig. 5. As expected, only one main beam appears at +20°, +30°, and +40°. In contrast, the quantization lobe at -20°, -30°, and -40° is suppressed due to random phases incorporated in the feed network of the RIS unit cells. The measurements show a QLL and side lobe level (SLL) below −10 dB, and the gain of the main beam drops less than 3 dB for a bandwidth of >2 GHz. The peak performance of the RCS is observed at 27.1 GHz, which differs from the designed frequency of 27.7 GHz. The shift is the contribution of multiple factors, such as fabrication tolerances and the dielectric constant value employed in the simulations.

V. CONCLUSION

We presented a modular and scalable RIS design approach based on 16 × 16 element, binary phase tiles operating at 5G mmWave frequencies. The measured RCS results of the RIS tile demonstrated a single main lobe with more than 10dB suppression of the quantization lobe at various reflection angles. Also, a 3-dB bandwidth of 7.4% and a half-power beamwidth of 8°, 9°, and 10° are obtained for 20°, 30°, and 40° reflection angles, respectively. Furthermore, the proposed topology can be extended to designs operating at higher mmWave frequencies and support dual polarization designs or 2-bit phase shifting with the same control circuitry.

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