Ultrathin High-Mobility SWCNT Transistors with Electrodes Printed by Nanoporous Stamp Flexography

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Abstract

To achieve high-performance printed electronic devices, scalable and cost-effective printing of high-quality metallic electrodes with narrow gaps, such for transistors with short channel lengths, is desirable. Here, we demonstrate short channel (<10μm) transistors, using thin (< 100-200 nm) electrodes fabricated by flexographic printing with nanoporous stamps, with single-wall carbon nanotubes (SWCNTs) as the network semiconductor. The nanoporous stamps comprise polymer-coated vertically aligned carbon nanotubes (CNTs) and facilitate control of the printed ink thickness in the 50-200 nm range. The measured on-off ratio and mobility meet or exceed those of previously reported SWCNT network transistors fabricated by alternative printing methods.

Keywords: printed electrodes, transistors, flexography, nanoporous stamps, SWCNT networks

Main Text

High-throughput, cost-effective manufacturing of electronics including radio frequency identification (RFID) tags[1], gas sensors, and light emitting diodes (LEDs) is essential to broader availability of technologies such as smart packages, wearable displays, and skin-conforming medical devices[2–6]. To expand the use of electronics in such daily-life products, silicon microfabrication processes are limited in terms of cost, throughput and substrate flexibility. Printed electronics utilizing scalable printing technologies, such as inkjet, screen printing, gravure and flexography are promising alternatives. Therefore, a massive number of research, development and production of printed electronic devices has been reported in the last two decades[7–10].

Transistors are a basic building block of printed electronics, and the transistor quality and performance are driven by the choice of materials, degree of miniaturization, and dimensional precision. For example, the performance of the printed displays[11,12] is driven by the thickness and the switching speed of the constituent thin-film transistors[13,14]. The speed of a thin-film transistor depends mainly on the semiconductor carrier mobility and the channel length, measured by the distance between the source and drain electrodes. Thick and non-uniform dielectric and electrode layers in transistors lead to lower breakdown voltages due to large localized electric fields[13]. Therefore, the performance of transistors manufactured by printing technologies are correlated with lateral resolution and minimum thickness of extant methods[9].

Most of printing technologies for electronics use liquid or polymeric inks, often containing colloidal nanoparticles that are annealed to form films after evaporation of the carrier solvent. As such, limitations to the feature size and thickness are attributed to the coupled, time-dependent fluid and solid mechanics of the printing process. Recently, flexographic printing with significantly finer printed feature dimensions was achieved using nanoporous stamps instead of traditional non-porous polymer stamps.[9] The nanoporous stamps can retain the ink within their volume[9,15], enabling the printed pattern to precisely replicate the shape of stamp features without suffering the squeeze-out and dewetting instabilities that are common in traditional flexography with non-porous elastomeric stamps. Nanoporous flexography, which is capable of printing conductive, dielectric, and semiconducting nanoparticle inks into features having ~3 μm minimum width and ~30-50 nm thickness at high speed (0.1 m/s) [9,16], is therefore attractive for printing high performance transistors as elements of future integrated devices.

Here, we demonstrate thin (< 100-500 nm), short channel (<10μm) transistors, using electrodes fabricated by flexographic printing with nanoporous stamps, with single-wall carbon nanotubes (SWCNTs) as the network semiconductor. We designed and fabricated a bottom gate, top-contact transistor as shown in Fig.1A. The device consists of a p-doped silicon gate electrode (resistance = 0.001-0.005 Ω-cm, thickness = 500 μm), thermally grown silicon dioxide (thickness = 300 nm, University Wafer Product No. 1583) dielectric layer, silver source and drain electrodes (thickness ~100-200 nm), and SWCNT network semiconducting layer.

Flexographic printing of silver electrodes was achieved with nanoporous stamps comprising vertically aligned carbon nanotubes (CNTs) which are conformally coated with polymer via initiated chemical vapor deposition (iCVD, Fig.1B). We inked the stamp via spin-coating, and the high porosity (~90%) of the prepared stamp allows to retain the liquid ink within their volume. Using the inked stamp designed according to the device, the source and drain electrode pattern (Fig. 1C) was printed directly onto the oxide-coated silicon wafer. For successful printing, control of contact pressure was essential, and must lie

within a range determined by the stiffness of the CNTs, CNT-CNT spacing, and the standard deviation of the lengths of CNTs.[9,15] In a prior work, we estimate the pressure range where the area ratio (ratio of area of stamp pattern to printed pattern) is ~ 1 using experiments and analytical modeling. The thickness of the printed layer can be controlled via the speed at which the stamp is retracted away from the substrate after contact. During printing, in a custom-built plate-to-plate printing apparatus[9], we brought the stamp into contact with the wafer and apply a contact pressure of ~50 to 100 kPa using a weight. After maintaining contact for ~15 s, we retracted the stamp quasi-statically (~1 mm/s) enabling printing of layers with thickness > 200nm after solvent evaporation.

The liquid ink (736511, Sigma Aldrich) contained <10 nm silver nanoparticles dispersed in tetradecane with ~50-60% weight concentration. After drying for 2 mins in ambient conditions, the substrate with the printed ink pattern was annealed to retain the electrical conductivity by sintering the metal particles into a continuous film (Fig. 2A-C). Here, the annealing condition needs to be appropriately controlled considering the printed thickness, as excessive temperature and/or annealing time can cause dewetting and breakup of the Ag film. Annealing was performed in ambient conditions on a hot plate with a set temperature of 200-500 ^{0}C[17]. Higher annealing temperature and longer annealing time results in greater grain size therefore can enhance the electrical conductivity, yet voids may form once the local metal grain size exceed the layer thickness and therefore the conductivity reduces. At sintering temperatures below 300 ^{0}C coarsening and densification is insufficient and at temperatures above 300 ^{0}C, though continuous films with large grains form locally, several voids form and this can lead to large variations in the measured conductivity of the sintered films (Fig. 2D). At sintering temperature of 300 ^{0}C, it is possible to form continuous layers with few voids for printed layers of thicknesses varying from 50 to 250 nm (Fig. 2E). With appropriate annealing, the measured conductivity (Fig. 2F, 2G) of the annealed source and drain electrodes was 4.25 x 10^7 S/m, which is 70% of that of bulk silver.

The annealing condition should be adjusted according to the printing thickness. For experimental investigation, we printed electrodes with different thickness of ~50 nm, 110 nm, and 185 nm (Fig. 2C). We observed the SEM images of the annealed samples to assess the continuity of films qualitatively (Fig. 2E). For the thinnest layers (~50nm), dewetting leads to discontinuities in the sintered layers. The resistance of the sintered layers was measured by printing lines of length ~850 µm and width ~10 µm (Fig. 2G). The resistance decreases with increasing sintering temperature for lines of thicknesses >100nm. (Fig. 2G). At 250 ^{0}C sintering temperature, resistance is high and has the largest variation with thickness. At 350 ^{0}C sintering temperature, resistance is the lowest for all thicknesses but there is large variation with thickness. But, at 300 ^{0}C sintering temperature, for printed films of t_{av} ~50- 250nm, resistance has minimum variation with thickness. Therefore, 300 ^{0}C was determined to be the optimal sintering temperature, and good quality features with conductivity of 4.4 x 10^7S/m (~70% of bulk silver) and the minimum sintering time is ~ 1 min.

We selected SWCNTs as the semiconducting layer, owing to the compatibility of solution-based SWCNT deposition with non-lithographic fabrication. The performance of CNT network transistors strongly depends not only on the quality of individual CNTs but also the CNT density. We deposited the semiconducting layer on top of our printed S/D electrodes via spincoating, and the density was tunable by the droplet volume, spincoating speed and duration. Here, a 300 µl droplet of ink (NanoIntegris, IsoSol-S100, 99.9% purity) was pipetted onto the wafer and then the wafer was spun to 1500 rpm for 15 seconds in a spincoater (Specialty Coating Systems, G3P SPINCOAT). No surface pretreatment was used before deposition. The measured density of the network of SWNCTs is ~100 SWCNTs/µm^2 (Fig. 3A, Fig.S1) which is above the percolation threshold[18,19] (> 40 SWCNTs/µm^2) resulting in high on-conductance and mobility.

The transfer characteristics of the fabricated transistors were measured by varying V_g from -10V to +10V and measuring I_d for V_d =1V, 5V, 7V, 9V,10V. Fig.3B, Fig. S2 shows the transfer characteristics for the transistor with a channel length of 7 µm. The on-off ratio of the transistors exceeded 10^3 and the threshold voltage varied from 1 V to 8 V. The mobility is calculated based on the slope of the plot of $\sqrt{I_d}$ against V_g using the following equation (see Supporting Information)

$$\sqrt{I_d} = \sqrt{\frac{\mu C_{ox} W}{2L}}(V_g - V_T)$$

where μ, C_{ox}, and V_T are the mobility, oxide capacitance and threshold voltage respectively. Fig. S3 compares the transfer characteristics at V_d =1V for three transistors with channel lengths of 6.6, 12.4, and 146 µm. The mobility increases from 13.8 cm^2/Vs for L = 12.4 µm to 39.5 cm^2/Vs for L = 146 µm (Table S1). The mobility variation with channel length is likely due to the variation in the SWCNT network density between the devices of different channel lengths. The extracted mobility is also likely affected by the contact resistance and its variations. The low on-off ratio is likely due to high contact resistance. The output resistance calculated from the output characteristics (Fig. S4) does not vary significantly with the gate voltage, which is one of the indicators of high contact resistance in the device.

The on-off ratio and the mobility of our transistors were determined in the range of 10^3-10^4 and ~13-39, respectively, which are comparable to other printed transistors (Fig. 3C and 3D).[7,8,20–27]. The total thickness of the device excluding the gate (p-doped Si) layer is ~400-600nm which is thinner than other printed transistors reported in literature.[13,28] With nanoporous stamps, ultra-thin layers can be printed as the ink transfer volume per unit length is the lowest as compared to other printing processes[9]. Notably, nanoporous stamps can be adopted to continuous manufacturing by fabricating CNTs on a roller and using a continuous inking system. In prior work, we have shown also compatibility with continuous printing in a plate to roll format, and the combination of speed (>200 mm/s) and resolution (~ 3µm) surpasses published process capabilities for flexography, gravure, inkjet and screen printing processes[9].

We have demonstrated a TFT with good performance characteristics. To demonstrate a fully printed device on flexible substrates, printing of gate and dielectrics and optimization of sintering conditions are required and we expect these can be achieved. The printing of SWCNT networks can also be studied. By using layer to layer registration and achieving a designed overlap between the S/D electrodes and dielectric layer, leakage currents can be reduced to achieve even higher on-off ratios (>10^4) than what has been achieved in this work.

Supporting Information

Fabrication of transistor by printing silver nanoparticles and forming a continuous layer by sintering and deposition of SWCNT networks with organic solvent based ink, Transfer characteristics of the transistor (channel length 7 μm) for drain voltages varying from 1-10V, Transfer Characteristics of the transistors with channel lengths varying from 6.6 to 146 μm plotted as $\sqrt{I_d}$ against V_g for calculation of mobility and on-off ratio, Output characteristics of the transistor (channel length 7 μm) for gate voltages varying from -3V to -0.5V, On-off ratio and mobility values for the transistors calculated from the transfer characteristics, Mobility calculation using model for linear region.

Acknowledgements

Financial support was provided by the National Science Foundation (CMMI-1463344, CMMI-1826216), the MIT Energy Initiative Seed Fund, the MIT-Skoltech Next Generation Program (First Round, 2016-2019), and BAE Systems. We thank Ahmad Zubair, Elaine McVay, and Marek Hempel for assistance in measurements of transfer characteristics. CNT catalyst deposition and patterning were performed at the MIT Microsystems Technology Laboratory (MTL). Electron microscopy and profilometry were performed at the shared experimental facilities at the MIT Center for Materials Science and Engineering (CMSE) supported in part by the MRSEC Program of the National Science Foundation under award number DMR-1419807.

Methods

Stamp Fabrication The stamp consists of source and drain electrodes with different channel lengths (L=5-150μm) and fixed width (W=200μm). An exemplary stamp is shown in Fig. 1B. To fabricate the stamps[9], first vertically aligned CNT arrays (CNT 'forests') are grown on lithographically patterned silicon substrates by atmospheric pressure chemical vapor deposition (CVD). Then, the top entangled 'crust' layer (<1 μm thickness) is removed by a brief oxygen plasma etching (Diener, Femto Plasma System) and coated with a thin layer (~20 nm) of poly-perfluorodecylacrylate (pPFDA) using initiated CVD (iCVD).[9,29,30] The plasma etching is critical to remove the stiff and rough crust which is not desirable for high-resolution printing because it results in non-uniform contact against the target substrate. The pPFDA coating followed by second plasma treatment allow liquid infiltration and solvent evaporation without shrinkage or collapse of the CNT forest by elastocapillary densification. The final plasma-treated pPFDA-CNT microstructures are highly porous (>90 % porosity) with nanometer pore size (~100-200 nm), allow liquid infiltration without deformation due to capillary forces, and are mechanically compliant, enabling uniform contact with the target substrates.

Inking The ink used in this study is composed of silver nanoparticles dispersed in tetradecane (Sigma-Aldrich, 736511). The surface tension and viscosity of the ink are 27 mN/m and 10 mPa-s, respectively, and the ink exhibits good conductivity (30-60% of bulk silver) after annealing.[9] The particle concentration is 50-60 wt% with particle sizes less than 10 nm. A 100 μl droplet of ink is pipetted onto the stamp and then the stamp is spun to 1500 rpm for 1-3 minutes in a spincoater.

Annealing A hot plate was used to do rapid annealing of the silver nanoparticles after printing the silver ink. The hot plate was set to the 300 ^{0}C and the stamps were placed on the hotplate after it reached the setpoint. The stamps were left on the hot plate for 1 minute for annealing.

Device Characterization A DC probe station and semiconductor parameter analyzer (Agilent 4155C, Easy Expert software) were used for the measurement of conductivity of the annealed electrodes, and the transfer characteristics of the TFTs.

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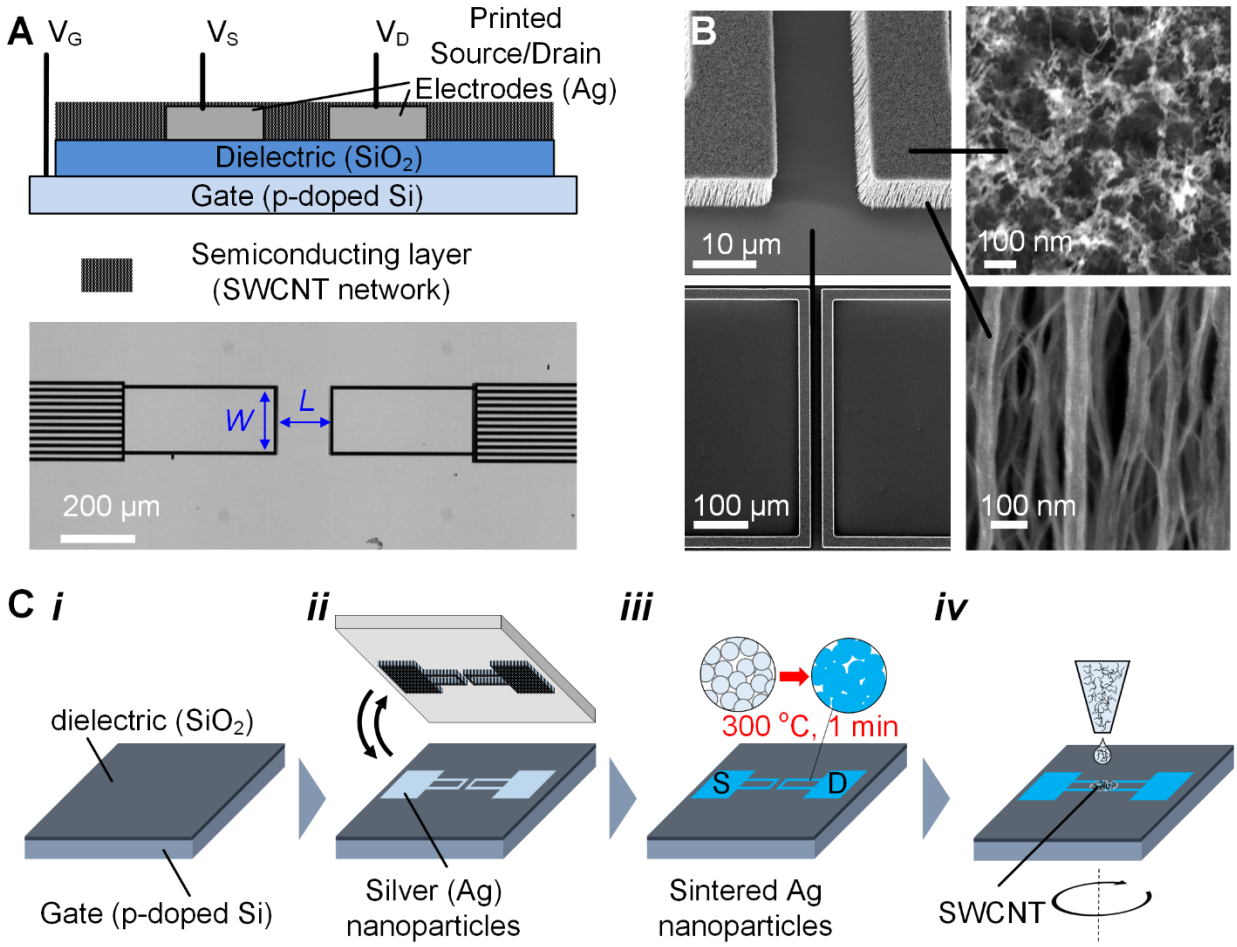

Figure 1. SWCNT transistors with electrodes printed using nanoporous stamps. A) Schematic of the device and top-view microscope image of the CNT-based printing stamp showing the channel geometry defined by the source and drain electrodes. B) SEM images of the stamp, showing the top and sidewall surfaces; channel has 10 µm length, defined by gap between stamp islands. C) Device fabrication steps showing i) p-doped silicon gate electrode with thermally grown silicon dioxide ii) printing of Ag nanoparticle ink to define source and drain electrodes, followed by iii) annealing to sinter the nanoparticles, and then iv) deposition of the semiconducting CNT solution which forms a thin film by spin-coating.

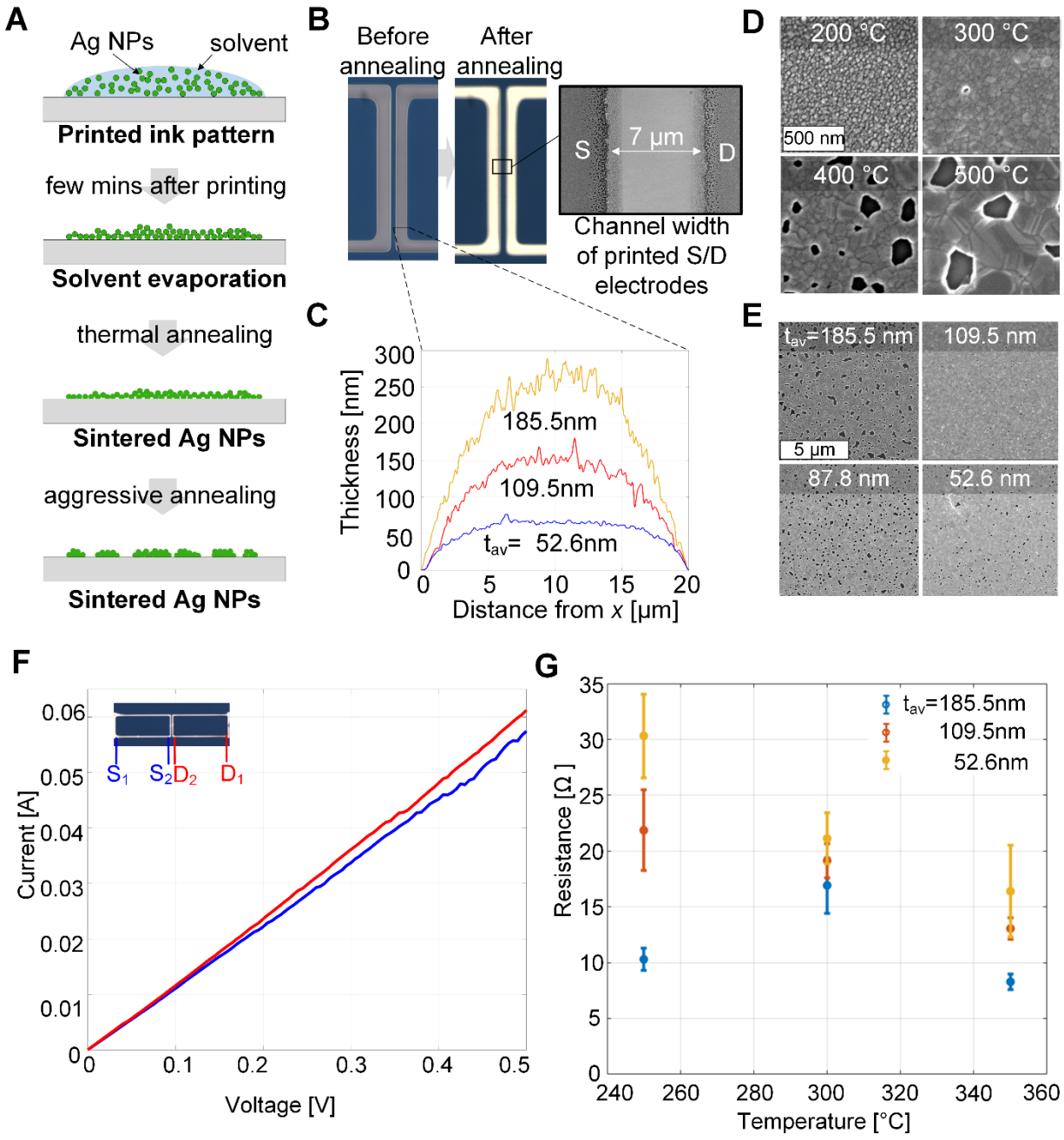

Figure 2. **Analysis of sintering of printed Ag nanoparticle inks to conductive electrodes.** (A) Schematic of transformation of thin ink film to continuous conductive layer after solvent evaporation and sintering. (B) Optical microscope and SEM images of printed source and drain electrodes. (C) Cross-sectional profiles of printed Ag ink lines before annealing having thicknesses 185.5 nm, 109.5 nm, and 52.6 nm. (D) Comparison of Ag film morphology after annealing at 200, 300, 400, 500 °C for 10 minutes. (E) Comparison of Ag film morphology after annealing at 300 °C for 10 minutes, for corresponding as-printed ink thicknesses. (F) IV characteristics of the source and drain electrodes exhibiting conductivity of ~70% of bulk silver after appropriate annealing. (G) Resistance of printed electrodes according to printed layer thickness and annealing temperature (times fixed to 10 minutes).

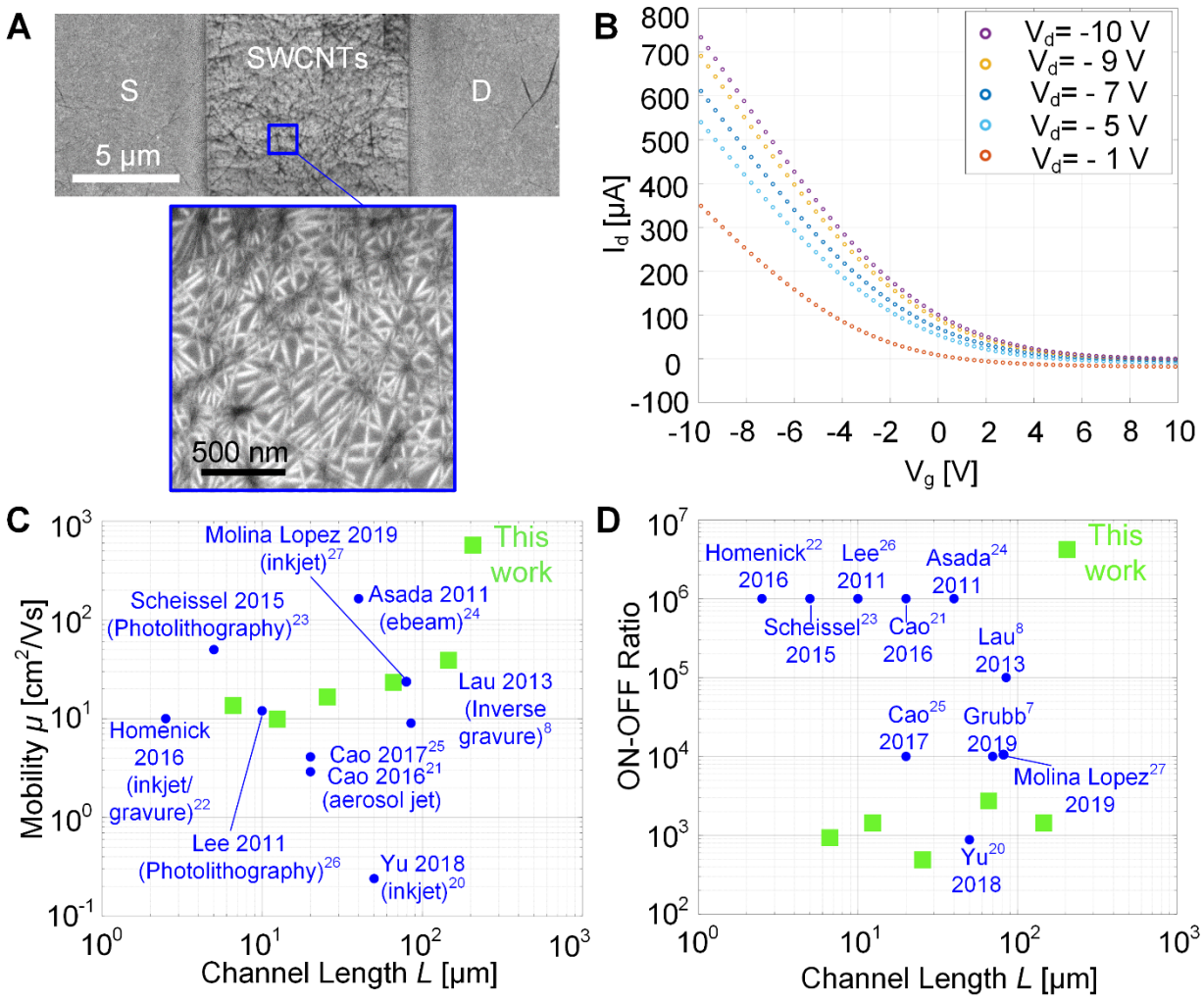

Figure 3. **Characteristics of SWCNT transistors fabricated using sintered Ag electrodes.** (A) SEM images of spincoated SWCNT film on top of Ag electrodes. (B) transfer characteristics of the transistor (channel length 7 µm) for drain voltages varying from -10V to -1V. (C) Mobility and (D) on-off ratio according to the channel length of the transistors reported in this work, and comparison with other previous SWCNT-based transistors.