2024 25th International Symposium on Quality Electronic Design (ISQED) | 979-8-3503-0927-0/24/$31.00 ©2024 IEEE | DOI: 10.1109/ISQED60706.2024.10528766

# GridVAE: Fast Power Grid EM-Aware IR Drop Prediction and Fixing Accelerated by Variational AutoEncoder

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***Abstract*—Electromigration (EM) remains the primary failure mechanism for copper-based interconnects in today's and future nanometer chip technologies. To ensure the longevity of on-chip power grids, effective EM-aware IR drop analysis is crucial. However, the existing power grid optimization approaches suffer high computational costs from the full-chip EM-aware IR drop analysis and sensitivity computation. This paper proposes a novel and efficient framework for full-chip power grid EM-aware IR drop prediction and fixing framework. We developed a conditional VAE-based framework, named *GridVAE*, for fast and accurate EM-aware IR drop prediction and full-chip power grid fixing. Compared to the state-of-the-art generative adversarial network (GAN)-based methods, our GridVAE model offers a remarkable 40% reduction in prediction RMSE on synthesized power grid benchmarks from ARM Cortex-M0 processor design. Building on the accurate EM-aware IR drop predictions and fast acquired sensitivities, we apply the sequence of linear programming-based optimizations to efficiently size the wires. Our proposed GridVAE method achieves up to an 140X speedup (at least one order of magnitude) compared to conventional SLP-based methods for power grid EM-aware IR drop fixing.**

## I. Introduction

Electromigration (EM) is a physical phenomenon in which metal atoms migrate in response to various driving forces, such as the applied electrical field. Due to EM, the hydrostatic stress within the metal wire can reach critical levels, leading to resistance variations during migration. In the context of modern very large-scale integration (VLSI) designs, EM remains the dominant reliability failure mechanism for copper-based interconnects, particularly in sub-nanometer technologies. And the challenges posed by EM are further exacerbated as technology advances toward nanometer manufacturing processes.

On-chip power distribution network (PDN), as the example shown in Fig.1, is a mesh-structured network that provides power from top metals. Due to the large and unidirectional current, PDNs are usually vulnerable to EM-induced failures. The wires' resistance may change over time due to the EM effect, resulting in the IR drops below the threshold voltage after years of aging effect, makes it difficult to design reliable PDN with area requirement.

Numerous past research works have investigated PDN sizing utilizing nonlinear or sequence of linear programming (SLP) methods [1], [2], [3], [4], [5], [6], [7], [8]. Zhou *et al.* [5], [9] proposed a power grid sizing approach based on multi-segment EM immortality check criteria. However, this EM immortality-constrained optimization proves too conservative, necessitating all interconnect trees to be immortal. In an effort to address this issue, Moudallal *et al.* [6] directly considers EM-induced IR drops in time-varying power grid networks. This method accounts for post-voiding resistance changes of wires through finite difference analysis of EM-induced stress in multi-segment wires, leading to a nonlinear problem solved via successive linear programming. Nonetheless, this method still incurs high computational costs, as the sensitivities of violating nodes must be computed by solving circuit matrices. More recently, Zhou [8], [10] presented a conjugate gradient-based localized EM-aware IR drop fix for power grid networks, using the generative adversarial networks (GAN)-based deep neural network (DNN) modeling method called *GridNet* to compute gradient sensitivities. Recently, a variational autoencoder (VAE) was proposed for generative applications [11]. Different than the standard autoencoder (AE) and GAN structure, which uses the same structure as AE for data generation, the VAE encodes the input into a predefined distribution in the latent space, and introduces additional regularization in the cost function to encourage the resulting latent distribution to closely approximate the predefined distribution, thereby enhancing the reliability of generating new data. VAE has found applications in various fields, including quantum circuit design for drug discovery [12], generative guided analog routing [13], and analog circuit sizing [14], underscoring its versatility and potential in different research areas.

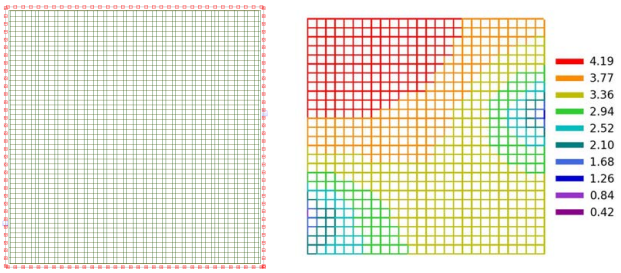


Fig. 1: (a) Power and ground networks of Cortex-M0 DesignStart; (b) IR drop map of the power network of (a).

Inspired by these works, we proposed a DNN framework, named *GridVAE*, to extend the VAE structure and incorporate with conditional information including the given aging time and current map. GridVAE can better predict the on-chip power grid IR drop and reduce the computational costs in power grid design and optimization while ensuring compliance with IR drop and EM lifetime targets. The key contributions of this study are summarized as follows:

- First, we propose *GridVAE*, a DNN framework designed

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This work is supported in part by NSF grants under No.CCF-2305437.

to model full-chip EM-aware IR drop data obtained from numerical EM-aware IR drop analysis tools. By comparing GridVAE with the state-of-the-art GAN-based model [8] on PDN EM-aware IR drop prediction, we achieved a significant 40% reduction in Root Mean Square Error (RMSE) based on synthesized power grid benchmark.
- Second, building upon the new *GridVAE* models, we leverage it to fast compute the sensitivity of cost functions to the wire width. This led to an accelerated power grid wire sizing method for ensuring the chip's EM lifetime based on the sequence of linear program optimization framework. Numerical results on a number of synthesized power grid benchmarks from ARM Cortex-M0 processor designs show that the *GridVAE* enabled optimization can provide up to over $140X$ speedup over the existing analytical matrix solving-based SLP method [6].

The rest of the paper is organized as follows: Section II reviews the related preliminary works on the EM-induced IR drop analysis and current EM-aware power grid optimization strategy. Section III introduces the detail of the proposed *GridVAE* framework and the fast full-chip IR drop fixing strategy accelerated by it. Experiment setup, numerical results, as long as analysis and discussions are summarized in Section IV. Section V concludes the paper .

## II. Preliminaries

In this section, we first summarize and review some related preliminary works of on-chip power grid EM-induced IR drop analysis and mitigation approaches.

### A. Full-chip EM-induced IR drop analysis

As mentioned in the previous section, EM is a physical phenomenon that can lead to resistance increase or even open-wire segments. The IR drop of the power grid wires may change due to the EM-induced aging effect. This means we have to consider the power girds IR drop as time-varying characters [15], [16], [17], [18]. On the other hand, the failed wire segments change the current distributions of all the interconnect wires, which may further accelerate the failure process. Hence, to emulate the on-chip power grid IR drop after the aging effect, one has to consider the interplay between the two physics: electrical characteristics and hydrostatic stress in the interconnect wires.

*EMspice* [15], [19] is an open source tool that conducts the full-chip power grid network coupled EM-IR drop simulation with the dynamic interplay between the hydrostatic stress and electronic current/voltage. It solves the coupled time-varying partial differential equations in the time domain to obtain the stress evolution, and finally reports resulted IR drop and EM failure hotspots at the target aging time, such as 10 years. The tool consists of a finite difference time domain (FDTD) solver for EM stress and a linear network DC solver for IR drop. The linear network IR drop solver passes time-dependent current densities and P/G layout information to the finite difference time domain FDTD EM solver, and the FDTD EM solver provides the IR drop solver with new resistance information. These two simulations are coupled together and must be solved together, which can be described as

$$\begin{aligned}
&\mathbf{C}\dot{\sigma}(t) = \mathbf{A}\sigma(t) + \mathbf{P}I(t),\\
&\mathcal{V}_v(t) = \int_{\Omega_L} \frac{\sigma(t)}{B} d\mathcal{V},\\
&\mathbf{M}(t) \times u(t) = \mathbf{P}I(t),\\
&\sigma(0) = [\sigma_1(0), \sigma_2(0), ..., \sigma_n(0)] \ , at \ t = 0
\end{aligned} \tag{1}$$

In the above equations, $\mathbf{M}(t)$ is the time-varying power grid conductance matrix, as the resistance changes due to the EM failure process. $\mathbf{P}$ is the input matrix, and I(t) represents the current sources from the chip. $\mathbf{C}$ is the identity matrix, and $\mathbf{A}$ is the coefficient matrix. $\sigma_n(0)$ denotes the initial stress at time step $t = 0$, for node $n$. The stress from the previous simulation step is used as the initial condition for each new time step. Such iterative coupled analysis on a long target lifetime can be extremely time-consuming for large power grid networks.

There are some research efforts to facilitate the IR drop/EM-aware IR drop analysis by leveraging machine learning-based approaches to build the surrogate models, including [20], [21], [22], [23], [24], [25] to reduce the evaluation time during the physical design process. Lin *et al.* [20] tried to extract power and physical features from cells and layouts to conduct the full-chip dynamic IR drop analysis. Fang *et al.* [21] proposed to train the models for the localized layout region to improve the scalability. A convolutional neural network (CNN) model which incorporates design-dependent features during pre-processing was proposed by Xie *et al.* [23]. Ho *et al.* [22] presented incremental IR drop prediction and mitigation by applying more electrical and physical features to train the gradient-boosting framework. Chhabria *et al.* [24] proposed *IREDGe*, a CNN-based generative network method to predict on-chip IR drop contours with image-to-image and sequence-to-sequence translation tasks. Recently Zhou *et al.* [8] considered more accurate physics-based EM effects into IR drop to build such surrogate models. It adopted the GAN-based structure to model the resulting EM-aware IR drops. This method regards the time, 2D power grid structure with input current and voltages as input images (series of images) and outputs the voltage map images. Such a surrogate model can help speed up wire sizing by fast EM-aware IR drop estimation and the sensitivity of objective functions concerning the wire geometries. It was initially applied to localized PDN optimization and then has been extended to full-chip optimization [10]. However, the GAN-based models suffer from the difficulties of training the generator and discriminator together. Also, the GAN model's deterministic latent variable encoding and decoding approach make the latent space lack of continuity and interpretability and less generative capability (due to non-regulated latent space), eventually affecting the prediction accuracy.

### B. Existing EM-aware PDN optimization

Besides the full-chip aging-aware IR drop estimation, one also needs to fix or alleviate the excessive IR drop to ensure a robust PDN design. Lots of past research applies nonlinear methods [1], [2], [3], [4], [5], [6] to size the PDN wires properly. These optimization strategies aim to meet the IR drop requirement at the target lifetime or extend the main time to failure (MTTF) with minimized metal routing area.

The SLP-based method was proposed first in [3] based on Black's equation. Then this method was extended to

consider multi-segment wires [26]. But this method can be too conservative as it requires all the wires to be immortal after optimization. Although, this method has been extended to consider a targeted lifetime by allowing some wires to fail and optimizing the rest of the wires [5]. Recently [6] proposed to directly optimize EM-induced IR drops on the time-varying power grid networks EM caused by EM-induced aging using the SLP method. However, the EM-induced IR drop is still computed by solving Korhonen equations, and the sensitivities of the IR drop with respect to the wires are calculated through the matrix-solving method. The solving process is severely time-consuming, especially when the power grid is enormous.

## III. Proposed VAE-accelerated EM-aware IR drop fixing method

### A. EM-Aware IR Drop Prediction

*1) AEs, VAEs, and CVAEs:* CNNs with an encoder-decoder structure are widely used in image generation tasks. This architecture forms the basis for several generative models, including the simplest form AE, GAN, and VAE [11]. GAN [27] model introduces an additional binary output CNN called *discriminator* only during the training stage to improve the result quality, and adopts the same AE structure for result generation. Fig. 2(a) shows AE (as well as GAN) will encode input $\mathbf{x}$ to low-dimensional latent variables $\boldsymbol{z}$ by the encoder and then decode the result by the decoder.

VAE, as shown in Fig. 2(b), is a unique generative model derived from the standard AE. Compared to the traditional AE structure, VAE does not encode the input into a discrete point, but a distribution over the latent space $Q(Z|X)$ with multivariate Gaussian prior. This enables the VAEs to have a better latent space interpretability.

Building upon the foundation of VAEs, we propose to adopt the CVAE as the backbone, which extends the VAE to incorporate the conditional information, including the given aging time and current map, so that our model can predict the EM-aware IR drop conditioned on the specified aging time and current distribution.

*2) GridVAE Framework:* The proposed GridVAE is shown in Fig. 3. Take an example power grid design with 60 rows and 60 columns, the GridVAE model input consists of four channels, which are the power grid topology splitted into vertical conductance $\mathbb{R}^{60\times60\times1}$ and horizontal conductance $\mathbb{R}^{60\times60\times1}$, the current source map $\mathbb{R}^{60\times60\times1}$ drawn to other circuit layers, and a target lifetime $t$ expanded into $\mathbb{R}^{64\times64\times1}$ by channel-wise duplication. Since size 60 x 60 is close to 64 x 64, we padded 2 zero entries on each side of the input so that the model input size becomes 64 x 64 x 4. In this example, the encoder consists of four convolutional layers followed by two fully-connected layers. if the power grid exceeds the size of 64 x 64 but is smaller than 128 x 128, we pad the input into the standard size of 128 x 128 and add one more convolutional layer in both the encoder and the decoder network. Similarly, if the input dimension is larger than 128 but smaller than 256, we further pad the input to size 256 x 256 and add another one more convolutional layer. Thus the GridVAE model is actually quite scalable for larger power grid.

The input $\boldsymbol{x}$ is encoded to a 20-dimensional multivariate Gaussian distribution in the latent space. We denote the mean of $Q(Z|X)$ as $\mu_x$ and the standard deviation as $\sigma_x$ . We use the reparameterization trick to ensure the model back propagation

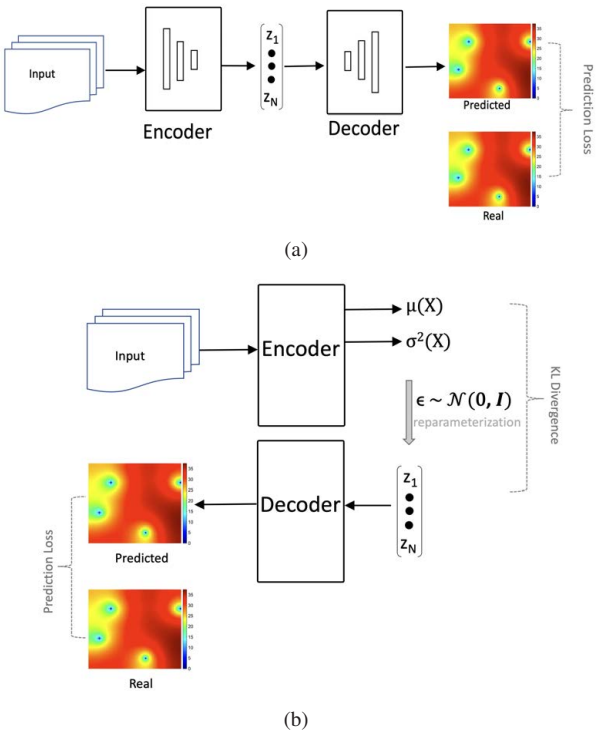


Fig. 2: (a) Architecture of an auto encoder (b)Architecture of a variational auto encoder

with gradient descent while sampling the latent variable, as shown in (2), which first samples from $\epsilon \sim \mathcal{N}(\mathbf{0}, \mathbf{I})$ and then computes the latent variable $\boldsymbol{z}$:

$$\mathbf{z} = \mu(X) + \sigma * \epsilon(X) \tag{2}$$

The decoder is designed to mirror the architecture of the encoder in a symmetric manner, except the output layer has only one channel. The output is $\mathbb{R}^{64\times64\times1}$ EM-aware IR drop at target aging year.

*3) Training and Data Preparation:* The total loss function consists two parts. The first part is the *reconstruction loss*, also called *prediction loss* when the input and output are expected to differ. The *prediction loss* measures the difference between the decoded result $\hat{y} = P(\hat{y}|z)$ and real data $y$, encouraging the decoded output data to be similar to the label. As our data is continuous, we allocate the mean squared error (MSE) for the *prediction loss evaluation* in (3), where N is the total number of output pixels.

$$MSE(y, \hat{y}) = \frac{1}{N}\sum_{1}^{N}(y - \hat{y})^2 \tag{3}$$

The second part is the *Kullback-Leibler (KL) divergence* between the encoder's latent variable distribution $Q(z|x)$ output and a chosen prior distribution, usually a standard multivariate Gaussian distribution $\mathcal{N}(\mathbf{0}, \mathbf{I})$. The *KL divergence* measures how one probability distribution differs from a second, which acts as a regularization term to force the encoded latent variable distribution from the given training dataset to be close to a standard normal distribution, and encourage the network to use the latent space efficiently. The *KL divergence* in VAE can be written as:

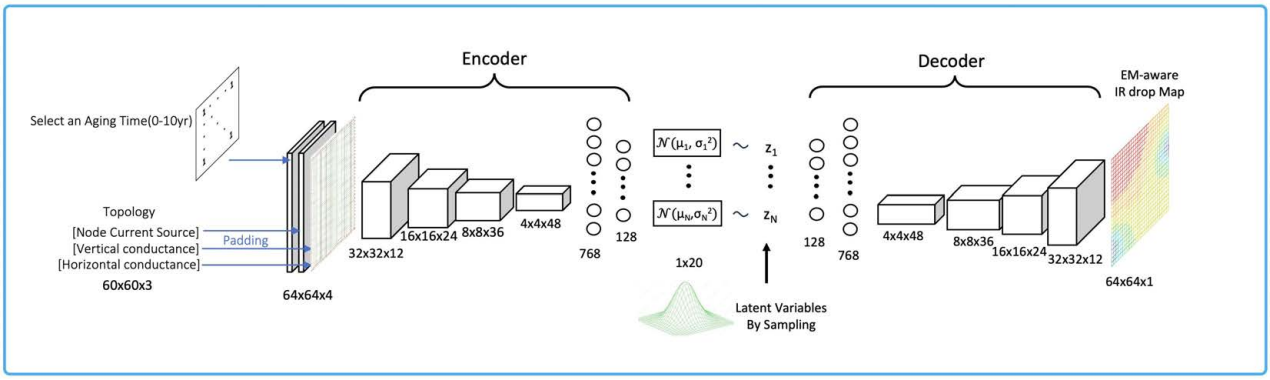


Fig. 3: The architecture of the proposed GridVAE for EM-aware IR drop prediction

$$D_{KL}(\mathcal{N}(\mu_x, \sigma_x^2) \,||\, \mathcal{N}(\mathbf{0}, \mathbf{I})) = \frac{1}{2}(-\log\sigma^2 + \mu^2 + \sigma^2 - 1) \quad (4)$$

Hence the training target is to minimize the total loss:

$$\min\{MSE(y, \hat{y}) \; + \; \lambda \cdot D_{KL}(\mathcal{N}(\mu_x, \sigma_x^2) \,||\, \mathcal{N}(\mathbf{0}, \mathbf{I}))\} \quad (5)$$

where $\lambda$ is the hyper parameter that adjusted similar to [28] to prevent KL vanishing.

We measure the prediction accuracy in RMSE (6), the unit is mV

$$RMSE = \sqrt{\frac{1}{N}\sum_{1}^{N}(y - \hat{y})^2} \quad (6)$$

The data preprocessing before the model training is as follows: First, the circuit layouts are automatically created by Synopsys IC compiler from a synthesized gate-level netlist and a standard cell library. Then IC Compiler output power grid information is sent to the power grid file parser, which reorganizes the information, including structure, wire layer, wire length, wire resistance values, node location, voltage, current source, etc. Next, the *EMspice* provides the EM-aware electrical information from the result above. Eventually, we parse these EM-aware electrical features and the topological information for the circuit layout and send it to our VAE-based model for training and testing. The inputs conductance and current are normalized

TABLE I: Power Grid Designs Detail

| circuit | # nodes | # Trees | # voltage sources | $V_{DD}$ (V) |
|---|---|---|---|---|
| Design1 | 1024 | 64 | 2 | 1.05 |
| Design2 | 4096 | 128 | 4 | 1.05 |
| Design3 | 16384 | 256 | 4 | 1.05 |
| Design4 | 65536 | 512 | 9 | 1.05 |

### *B. Fast Power Grid EM-Aware IR Drop Fixing Framework*

The workflow of the proposed GridVAE-accelerated IR drop fixing strategy is shown in Fig. 4.

*1) Problem formulation:* The proposed method intends to solve the following problem: Given the power grid information at T=0, the GridVAE has predicted the EM-aware IR drop at the target aging lifetime T = *t* and revealed that the power grid has EM-induced IR drop violations demand fixing. IR drop violation means the power grid has nodes whose voltage drop

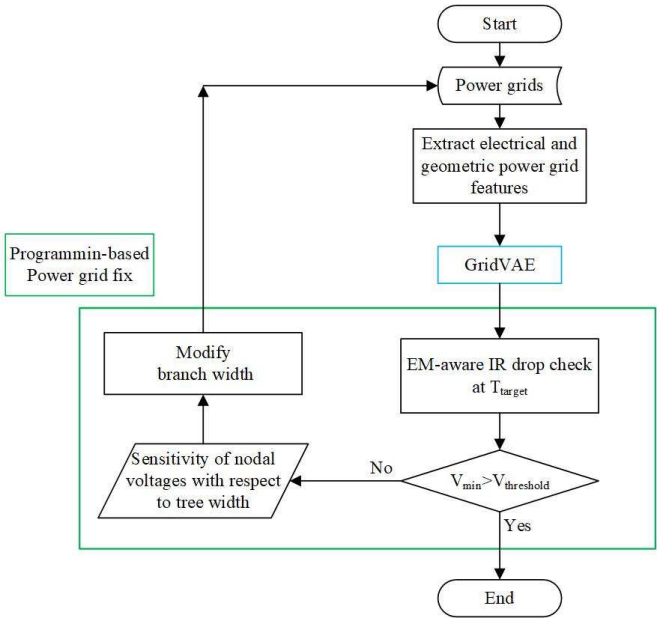


Fig. 4: Framework of power grid IR drop fixing method accelerated by the GridVAE.

$\boldsymbol{v}$ are above the threshold $V_{th}$. We wish to alleviate the above mentioned EM-aware IR drop failure by resizing the power grid interconnection trees' width with a minimum metal area increase.

The problem can be formulated as:

$$\begin{aligned} &\text{Minimize} && a^t s \\ &s.t. && v(t,s) \le V_{th} \quad (7) \\ & && s \in S \triangleq \{s \in R^{nt} : 1 \le s \le s_{up}\} \end{aligned}$$

In (7), $a = [a_1, a_2, \ldots, a_{nt}] = [w_1 l_1, w_2 l_2, \ldots, w_{nt} l_{nt}]$ refers to the metal areas of the power grid with $n_t$ trees, $w_i$ and $l_i$ are the $i_{th}$ tree's width and length separately. As for the constraint, $s = [s_1, s_2, \ldots, s_{nt}]$ is the resizing factor for the power grid trees. $S$ is the feasible region, where $s_{up}$ is the upper bound for $s$. Similar to [6], we assume the original power grid trees are already set to their minimum width. Hence we only increase the treewidth and $s \ge 1$. The feasible region reflects both the basic design rules and case-by-case user requirements, such as the criteria of minimum

interconnect treewidth, the minimum spacing to prevent the interconnect trees overlap, and the maximum metal area usage, etc. The node IR drop $v(t,s)$ is the voltage difference between the power grid interconnect node and the power supply, it is a nonlinear function to $s$ at aging time $t$. The maximum allowable voltage drop threshold $V_{th}$ is given by the user. We assumed it to be five percent of the power supply voltage.

*2) Programming-based optimization:* As we mentioned in III-B1, the EM-aware PG node voltage drop *v(t,s)* as the constraint is a nonlinear function to ***s*** at aging time ***t***. Hence (7) is a nonlinear optimization problem. We solve it by a stepping strategy, in which we linearize the voltage drop at the current latest solution point by Taylor's expansion (8) and solve (7) with linear programming (LP) solver. We repeat this operation until the power grid has no EM-aware IR drop violation.

$$v(t, s^{(i+1)}) \triangleq v(t, s^{(i)}) + \frac{\partial v(t, s^{(i)})}{\partial s} \cdot \delta s \tag{8}$$

where $s^{(i)}$ denotes the current power grid resizing vector and $s^{(i+1)}$ is defined as

$$s^{(i+1)} = s^{(i)} + \delta s \tag{9}$$

$\frac{\partial v(t,s)}{\partial s}$ is the $n \times n_t$ *Jacobian* matrix of $v(t,s)$ with respect to $s$, describes how the node voltage drops at target time $T = t$ respond to the corresponding treewidth rescaling, where n is the total number of nodes.

$$\frac{\partial v(t,s)}{\partial s} = \mathbf{J}_{n\times n_t}(s,t) = \begin{bmatrix} \frac{\partial v(1,t)}{\partial s_1} & \frac{\partial v(1,t)}{\partial s_2} & \cdots & \frac{\partial v(1,t)}{\partial s_{n_t}} \\ \frac{\partial v(2,t)}{\partial s_1} & \frac{\partial v(2,t)}{\partial s_2} & \cdots & \frac{\partial v(2,t)}{\partial s_{n_t}} \\ \vdots & \vdots & \ddots & \vdots \\ \frac{\partial v(n,t)}{\partial s_1} & \frac{\partial v(n,t)}{\partial s_2} & \cdots & \frac{\partial v(n,t)}{\partial s_{n_t}} \end{bmatrix} \tag{10}$$

*3) Fast sensitivity computation:* The sensitivity $\frac{\partial v(t,s)}{\partial s}$ in (8) describes how the nodes voltage ***v*** at $T = t$ will be affected by resizing the wires. We utilize the by-product of the GridVAE model to further accelerate the sensitivity computation. The GridVAE can provide the gradient of output node voltages to the input wire segment conductances by gradient back propagation after the GridVAE inference process, which is $\frac{\partial v(t,s)}{\partial g}$. Then we can quickly get (10) by chain rule, as each power grid tree $g_i$ has its resizing factor $s_i$ and will not be infected by other resizing factors:

$$\begin{aligned} \frac{\partial v}{\partial s} &= \frac{\partial v}{\partial g}\frac{\partial g}{\partial s}, \\ \frac{\partial g_i}{\partial s_k} &= \begin{cases} 0, & \text{if i} \neq \text{k} \\ g_i, & \text{if i = k} \end{cases} \end{aligned} \tag{11}$$

As a comparison to the conventional sensitivity acquisition by matrix solving method [6], we briefly review its main steps. For a power grid network represented by the node conductance matrix *G(t,s)*, it can be written in the following format (12):

$$G(t,s) \cdot v(t,s) = j(t) \tag{12}$$

where **j(t)** is an $n \times 1$ vector represents the power grid nodes current vector.

And the sensitivity is calculated as followed (13):

$$\frac{\partial v(t,s)}{\partial s_k} = -G^{-1} \cdot \frac{\partial G(t,s)}{\partial s_k} \cdot G^{-1} \cdot j(t) \tag{13}$$

To solve the above equation and obtain $\frac{\partial v(t,s)}{\partial s_k}$, one must first construct the sparse matrices *G* and $\frac{\partial G(t,s)}{\partial s_k}$ for all $k$, then perform matrix solving. Each column of the *Jacobian* matrix (10) has to be calculated through the process of (13) for the corresponding power grid tree. Hence building such a *Jacobian* matrix in the traditional method is computationally expensive.

## IV. Experimental results and discussions

### A. Experiment setup

The experiment is set up on a Linux server with 2 Xeon E5-2698v2 processors and Nvidia Titan X RTX GPU. The GridVAE is built with the PyTorch package. The linear programming-based power grid fixing part is implemented in Python. The test cases are randomly generated following the IBM format, based on the topology we extract from the real design and the constraints that the user defines. It comprises of VDD power nets, VSS ground nets, and two external supplies. The power grid file parser output is consistent with the IBM power grid benchmarks [29]. We have three different topology designs and generate large amounts of IBM format power grid networks to ensure different workloads can be tested and verified.

Design 1 comes from Cortex-M0 DesignStart processor, which implements ARMv6-M 32-bit architecture and is routed and placed using IC Compiler with 32/28nm Generic Library from Synopsys. The Cortex power grid consists of two layers and one thousand interconnect trees, as shown in Fig. 1(a). Fig. 1(b) shows the voltage drop from the same power grid, the unit is mV. Design 2 and Design 3 follow a similar pattern, the detailed information is in Table. I. To train the model, each topology dataset contains 10000 pairs of samples (workloads and aging time, EM-aware IR drop).Different current source maps are included in the dataset. The maximum allowable IR drop is set to 5% $V_{dd}$ and the target lifetime *T* is set from 0 to 10 years.

### B. The result and performance

We also implemented the GAN-based model [8] for EM-aware IR drop prediction comparison, and the excessive linear programming method in [6] for power grid fixing comparison.

TABLE II: Prediction accuracy of GridVAE vs state-of-the-art GAN-based model

| Circuit | PG Size (# nodes) | RMSE (mV) | |
|---|---|---|---|
| | | GAN-based model[8] | GridVAE |
| Design1 | 1024 | 5.697 | 3.144 |
| Design2 | 4096 | 6.100 | 3.519 |
| Design3 | 16384 | 3.922 | 3.462 |
| Design4 | 65536 | 7.583 | 4.371 |

The table II compares the EW-aware IR drop prediction accuracy between the proposed GridVAE and the state-of-the-art GAN-based model, the unit is mV. Results shows we can reduce up to 40% RMSE. The table III shows the comparison of our GridVAE-accelerated power grid IR drop fixing strategy versus the existing SLP-based method [6]. The last column

TABLE III: Comparison of the proposed VAE-accelerated SLP optimization method against the existing method

| Circuit | PG Size (# nodes) | naive SLP method [6] | | *GridVAE*-accelerated SLP | | Speed up |
|---|---|---|---|---|---|---|
| | | Area Increase | Time(s) | Area Increase | Time (s) | |
| Design1-PG1 | 1024 | 1.61% | 41.8 | 0.98% | 2.5 | 16.79 |
| Design2-PG2 | 4096 | 1.55% | 165.8 | 1.79% | 7.6 | 21.82 |
| Design2-PG3 | 4096 | 0.70% | 149 | 0.86% | 7.34 | 20.30 |
| Design3-PG4 | 16384 | 1.19 % | 1034 | 1.53 % | 12.3 | 84.06 |
| Design3-PG5 | 16384 | 2.85 % | 922 | 2.14% | 13.7 | 67.2 |
| Design4-PG6 | 65536 | 0.38 % | 5627 | 0.57 % | 40.45 | 139.1 |

indicate the proposed method has the speedup over [6]. As we can see that both SLP-based methods can lead to similar performance in terms of area, and can achieve more than 140X speedup. On the other hand, we see that our GridVAE-accelerated SLP method shows more speedup advantages as the sizes of the power grid increase.

## V. Conclusion

In conclusion, our work introduced a novel full-chip EM-aware IR drop estimation model, referred to as *GridVAE*, tailored specifically for on-chip power grid EM-aware IR drop prediction and rapid sensitivity computations, and accelerated the power grid fixing through a recently proposed linear programming-based optimization framework. The *GridVAE* reduced 40% RMSE over the recently proposed state-of-the-art GAN-based model on full-chip EM-aware IR drop prediction. Additionally, our GridVAE-accelerated method demonstrates an impressive up to 140X speedup (at least one order of magnitude) compared to conventional SLP-based approaches when applied to synthesized power grid benchmarks from ARM Cortex-M0 processor design. These findings underscore the potential of *GridVAE* as a promising tool for enhancing power grid optimization in modern nanometer-scale chip technologies, providing valuable insights into efficient and accurate solutions for addressing EM-related challenges in VLSI design.

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