Cross-Temperature Reliability of 3D NAND: Cell-to-Cell Variability Analysis and Countermeasure

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***Abstract*— Cross-temperature effect is a significant reliability concern for 3D NAND Flash memory. In this paper we explore the origin of cross-temperature reliability by measuring the cell threshold voltage (V_{th}) distribution at different temperatures. We observe significant cell-to-cell variability in the temperature coefficients causing distribution widening. We provide a conceptual picture to understand the distribution widening based on sub-threshold slope factor variation. We also discuss two system level countermeasures to minimize the cross-temperature effects.**

Keywords- 3D NAND Flash Memory, Cross Temperature, Variability

I. INTRODUCTION

3D NAND Flash memory technology is the predominant choice for large-scale data storage, owing to their remarkable attributes such as high chip density, three-dimensional integration, multi-bit storage capacity and low power consumption [1]-[3]. Despite being a mature technology, NAND Flash memories exhibit inherent reliability concerns [3]. Cross-temperature effects pose a significant challenge for NAND Flash memory, restricting their applicability in demanding environments like automotive systems and CubeSats [4]-[8]. Specifically, programming memory cells at one temperature and subsequently reading them at a different temperature leads to an increased occurrence of error bits, thereby constraining the permissible operating temperature range [4]-[10]. Temperature effects induce shifts in the cell threshold voltage (V_{th}), resulting in bit flips during read operations. To counteract the temperature-induced V_{th} shift, NAND manufacturers commonly employ an on-chip temperature sensor and a temperature compensation circuit. This circuit applies an offset voltage during read operations to compensate for the V_{th} shift due to temperature change. Unfortunately, even with the inclusion of a temperature compensation circuit, the state-of-the-art 3D NAND memory chips experience a significant amount of bit errors due to cross-temperature effects as reported in the recent literature [4], [5].

The illustrations in Fig. 1 conceptually depict the cross-temperature effects in the NAND Flash memory array through the cell V_{th} distributions. In Fig. 1(a), the red distribution represents the as programmed cell V_{th} distribution, assuming the programming was conducted at a high temperature (HT). When the same memory array is subsequently read at a low temperature (LT), the sensed cell V_{th} values turn out to be higher, causing an up-shift of the V_{th} distribution, as illustrated in black. Similarly, when the memory array is sensed at HT (red) after programming at LT (black), the distribution downshifts (Fig. 1(b)). It's noteworthy that cross-temperature sensing of the memory chip not only alters the mean value of the V_{th} distributions but also significantly broadens the distribution due to cell-to-cell variability in terms of temperature-induced V_{th} shift, referred to as the cell temperature coefficient or TCO.

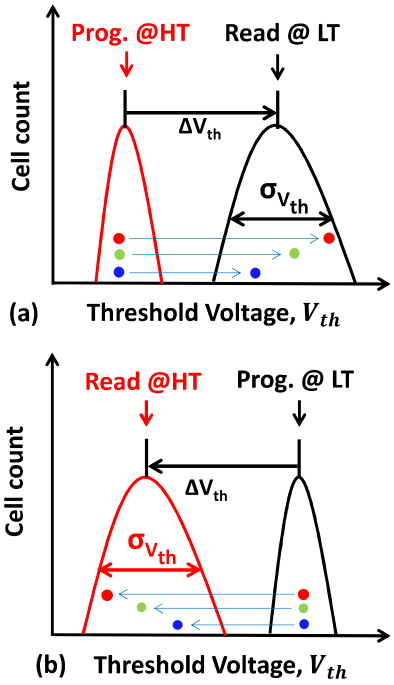

Fig. 1. (a) Illustration of cell V_{th} distribution when programmed at high temperature (HT) and read at low temperature (LT). The cell-to-cell variability in ΔV_{th} is illustrated with three types of cells. (b) Similar illustration of V_{th} distribution widening when programmed at LT and read at HT.

Temperature-sensitive cell-to-cell variability is exemplified through three distinct cells in Fig. 1. The blue cell signifies memory cells with a low temperature coefficient (TCO), the green cell with a median TCO, and the red cell with a high TCO. Essentially, the blue cell undergoes a lesser V_{th} shift compared to the green and red cells when subjected to the same temperature change. This variability in TCO among cells contributes to the broadening of the V_{th} distribution due to cross-temperature effects. The on-chip temperature compensation circuit may effectively account for the mean V_{th} shift by applying a DC offset to the read reference voltage, However, the distribution broadening remains uncompensated, leading to bit errors during read operations.

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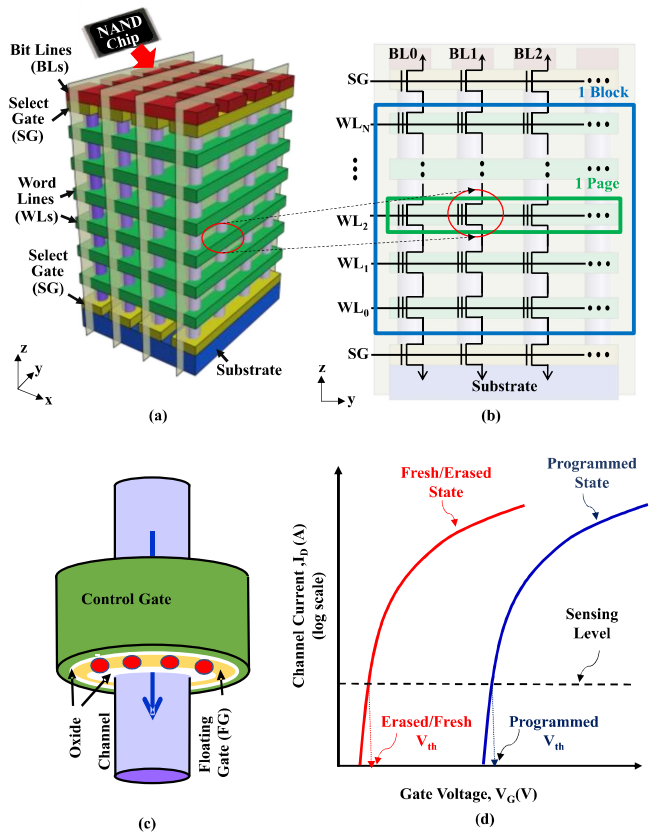

Fig. 2. (a) Schematic of a 3D NAND Flash memory block. (b) Circuit diagram of a 3D NAND memory array. (c) Structure of a single 3D GAA geometry Flash memory transistor. (d) Sensing of Programmed/ Erased cell's V_{th} from channel current (cell current/ string current).

In this paper, we measure cell V_{th} distributions at different temperatures from a commercial-off-the-shelf (COTS) 3D NAND memory chip. We carefully analyze the cell-by-cell V_{th}-shift variability and provide a conceptual framework to understand the origin of such variability. In addition, we identify two groups of cells: one having higher temperature coefficient (TCO) (red cells in Fig. 1) and the other with lower TCO (blue cells in Fig. 1) and carefully analyze their physical properties.

II. Background

The schematic of the 3D NAND Flash memory array is shown in Fig. 2(a). The green layers are the metallic word lines (WLs) of the memory array while the purple pillars are the poly-silicon channel. The blue bottom layer is the silicon substrate, and the red lines at the top are the bit lines (BLs). The yellow bars on the substrate represent the select gate (SG) transistors. Similar SG transistors are also present at the top near the bit lines. Fig. 2(b) shows the circuit diagram of a NAND Flash memory structure. A 3D NAND Flash memory chip typically contains thousands of Flash blocks while each Flash block consists of a fixed number of logical pages. Each logical page contains multiple Flash cells. A 3D NAND Flash memory cell is essentially a floating gate (FG)/charge-trap (CT) metal-oxide-semiconductor field-effect transistor (MOSFET) with gate-all-around (GAA) geometry [11]. The structure of a single 3D GAA FG Flash memory cell is shown in Fig. 2(c). Cell V_{th} is determined through the channel current at a specific read voltage applied to the control gates. Usually, a sensing current level is used for all cells as a reference to determine the V_{th}. The V_{th} is a strong function of temperature which is quantified as TCO and defined as follows:

$$TCO = \frac{\Delta V_{th}}{\Delta T} \quad (1)$$

The specific TCO values exhibit variation based on channel materials and transistor geometry. Typically, TCO values range within a few millivolts per degree Celsius with a negative sign, indicating that the threshold voltage (V_{th}) decreases as the temperature increases. Several factors contribute to the variability in cell TCO values within a 3D NAND array. For example, state-of-the-art 3D NAND transistors utilize granular poly-Si based channel material. The flow of cell current through the poly-Si channel is influenced by grain boundaries (GB) and local trap sites present in the conduction path [12]-[16]. Consequently, the statistical variation in GB positions, oxide-channel interface trap states, and GB-induced trap levels in the channel results in variability in cell current characteristics. Additionally, the tapered shape of the vertical channel in the 3D NAND string introduces another element of variability in current conduction. This variability induced by poly-Si significantly impacts the variation in TCO among memory cells in the 3D NAND array [15], [16].

III. Experimental Details

The experimental evaluation is performed on a COTS 3D TLC NAND Flash memory chip from a major manufacturer. To interface the raw NAND chip with the computer, we used a custom-designed hardware board, as illustrated in Fig. 3. The board includes a Ball-Grid-Array (BGA) socket to insert the NAND Flash memory chip and an FT2232H mini module from Future Technology Devices International (FTDI) [17] to

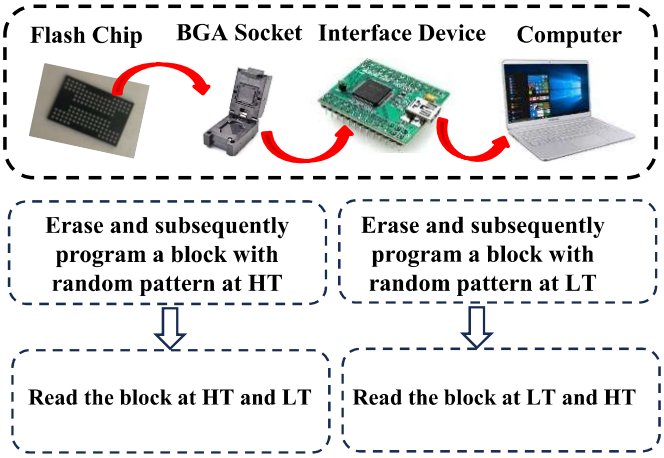

Fig. 3. Experimental set-up and workflow of the cross-temperature experiment.

interface the memory chip with a computer through Universal Serial Bus (USB) connection. We followed the command sets defined by the Open NAND Flash Interface (ONFI) [18] to perform basic memory operations such as read, write, and erase. The hardware setup allowed us to access the raw memory bits without any error correction. For the cross-temperature program/read experiment, we chose two temperatures: low temperature (LT = -15^{0}C), and high temperature (HT = 45^{0}C). We start by programming a block of the memory chip in TLC mode with random data pattern at LT and measure page V_{th} distributions at both LT and HT. To read the pages, we utilize the so-called read offset operations that allow the Flash controller to measure cell by cell V_{th} with high resolution. The read offset operation utilizes an internal digital-to-analog converter (DAC) to incrementally add an offset voltage (ΔV) to the read voltage based on the digital value given in the command. Thus, it sweeps the read voltage from the default level, V_{read0} to finally $V_{read} + \Delta V \times i$ where i indicates the number of points of this read reference sweep. For each shifted read voltage, we sense each cell's logical state from the corresponding pages. When at specific reference voltage point of the sweep, a cell's state flips, we denote that read voltage as the V_{th} of that cell. The exact process is repeated for the other cell states. This way, we can extract the cell V_{th} distributions of all memory cell states (TLC chips have eight memory states- $L_0 - L_7$). Subsequently, we program the memory chip at HT and measure V_{th} distributions at both HT and LT.

IV. Results and Discussion

A. Measurement of Cross-temperature V_{th} Broadening

In this section, we present the cross-temperature experiment results from the 3D NAND memory chip. Fig. 4 displays cell V_{th} distribution of the highest V_{th} state (L_7) from a memory page programmed with random data pattern. Different colors represent different sensing temperatures during distribution read operation. The temperature during page program operation was at -15 ^{0}C in Fig. 4(a). Note that even though the V_{th} distributions are read at different temperatures, the mean positions of the V_{th} distributions match, thanks to the on-chip analog temperature compensation circuit. However, the distribution sensed at HT is 72.6 mV broader than the distribution sensed at programming temperature, LT (distribution width measured from -3σ το +3σ level). Similar results are obtained when the chip is programmed at HT (45 ^{0}C) as shown in Fig. 4(b). Here the LT distribution is 68.8 mV broader than the HT (programming temperature) distribution (-3σ το +3σ). Similar trends are observed for the other programmed V_{th} states of the memory page. Since voltage margin between memory states is very low in TLC storage, the broadening of the distribution induced by the cross-temperature effects significantly increases the raw bit errors.

B. Cell-by-cell TCO Correlation

Next, we identify the high TCO and low TCO cells through cell-by-cell V_{th} -shift values. The V_{th} -shift values are calculated using the following equation: $\Delta V_{th} = V_{th}^{LT} - V_{th}^{HT}$, where V_{th}^{LT} indicates V_{th} measured at LT and V_{th}^{HT} indicates V_{th} measured at HT. We define ΔV_{th} in this way so that ΔV_{th} values remain positive for high TCO cells and negative for low TCO cells for any direction of temperature change, assuming on-chip temperature compensation circuit corrects for the median V_{th} shift. Since cell V_{th} values are higher when sensed at LT, positive ΔV_{th} values correspond to the high TCO cells whereas negative ΔV_{th} values stand for low TCO cells. Note that median ΔV_{th} value is very close to zero due to the correction made by the on-chip temperature compensation circuit during distribution read operation. Fig. 5(a) shows a scatter plot of cell-by-cell ΔV_{th} values when the chip is programmed at LT and read at HT. We observe a significant variability in the ΔV_{th} values. Similar scatter plot results are shown in Fig. 5(b) where the chip is programmed at HT and read at LT.

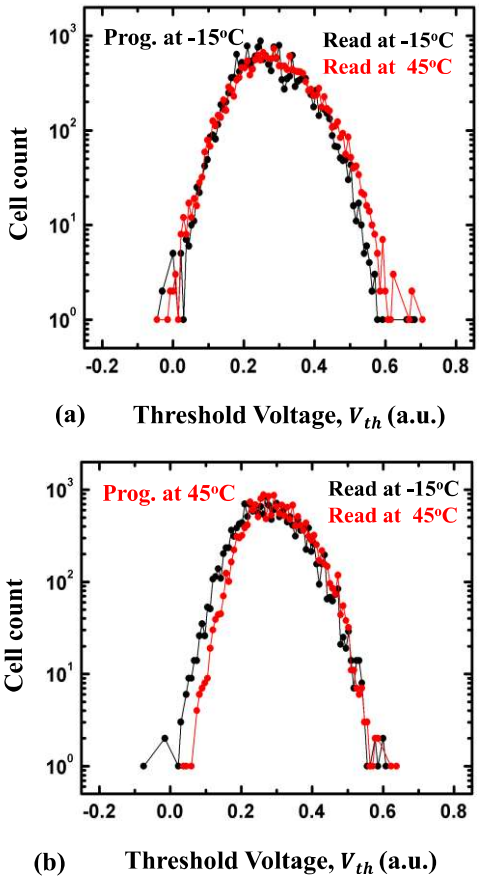

Fig. 4. (a) Measured V_{th} distribution (highest V_{th} state of the TLC memory) from a commercial 3D NAND chip when programmed at LT = -15°C and (b) at HT = 45°C.

Fig. 5(c) compares the cell-by-cell ΔV_{th} distribution obtained for the following two cases: (1) program at HT and read at LT; and (2) program at LT and read at HT. We find that ΔV_{th} distribution remains comparable in both direction of temperature change (ΔT). However, program at LT and read at HT results is slightly wider ΔV_{th} compared to the other direction. These results indicate that cell TCO may not be completely symmetric in both directions of temperature change. However, the median ΔV_{th} is around zero for both the cases due to the on-chip temperature compensation scheme.

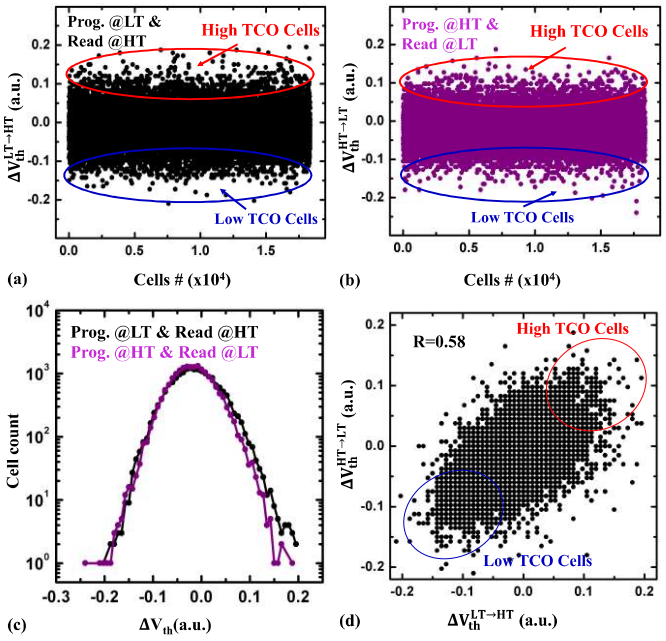

Fig. 5. (a) Scatter plot of cell-by-cell ΔV_{th} values of highest V_{th} state of a page when programmed at LT and read at HT and (b) programmed at HT and read at LT. (c) Distribution of ΔV_{th} due to cross-temperature sensing of L_7 state of a page. (d) Correlation plot of ΔV_{th} for the same state of the same page for both temperature change directions.

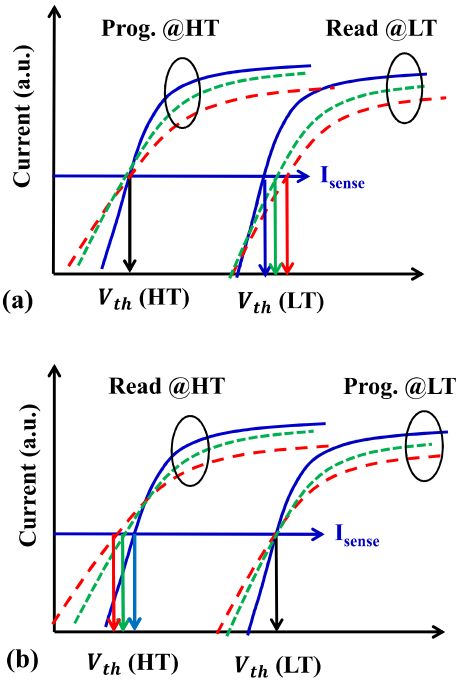

Fig. 6. Illustrative I-V characteristics of the three representative cells with different sub-threshold slope factor for two cases: (a) programmed at HT and read at LT and (b) programmed at LT and read at HT. I_{sense} is a sense current level at which V_{th} is measured.

To further consolidate the existence of two specific groups of cells that respond differently to temperature change, we present the correlation plot Fig. 5(d). Here we have shown the correlation of the ΔV_{th} values for both temperature change directions. We can find again a group of cells that always responds to sensing temperature change (either LT to HT or HT to LT) strongly (indicated by red circle). And there are another group of cells that undergoes weak ΔV_{th} for any direction of temperature change during sensing. Overall, we observe a good correlation indicating that ΔV_{th} for both ΔT directions are dictated by the same physical properties.

C. Root-cause Analysis

In this section, we discuss our hypothesis behind the cross-temperature V_{th} distribution brodening effects. Fig 6(a) provides an illustration of current-voltage characteristics of three different memory cells. We like to emphasize that these three representative cells have very different sub-threshold slope factors. Note that the I-V curve for these cells is crossing near the sense current level after program operation irrespective of their sub-threshold properties. This is due to the Incremental Step Pulse Programming (ISPP) scheme that NAND Flash memory employ to counter the effects of inherent cell-to-cell V_{th} variability and thereby narrowing the programmed V_{th} distribution. In other words, all the three cells are programmed at the similar V_{th} level, irrespective of the intrinsic variability, by ISPP scheme.

Despite the suppression of intrinsic cell variability during program operation, it re-emerges and negatively impacts the cell distribution during cross-temperature read operations. Fig. 6 illustrates the effects of cell variability on distribution broadening through variable shifts in the I-V characteristics. It's essential to note that when cells are read at different temperatures, their I-V curves shift by varying amounts, depending on the sub-threshold swing factor (m). This is governed by the following equation of sub-threshold current: $I_d \propto e^{q(V_{gs}-V_{th})/mkT}$. Typically, cells with a steeper sub-threshold swing exhibit less V_{th} shift during cross-temperature read operations, as depicted by the solid blue I-V curve in Fig. 6(a). Conversely, cells with a poor sub-threshold swing (or less steep) may induce a higher V_{th} shift, illustrated by the red dashed lines in the same figure. Similar trends in cell V_{th} shift is observed when program operation is conducted at low temperature (LT), and read operation is carried out at high temperature (HT), as shown in Fig. 6(b).

Variation of m-factor results from variation of poly-Si properties in the channel of the cells. The discrete grain boundaries (GBs) of the undoped poly-Si act as random dopants along the channel. Random placement and varying sizes of GBs create statistically varying local potential barriers. Moreover, GB locations can also act like active trap sites which can capture and emit electrons. In essence, variation in GB profile is one of the dominant reasons for the variation in subthreshold slope of the individual cell currents [15].

We verify this hypothesis with additional measurements shown in Fig. 7. We calculate the read noise magnitudes of the memory cells utilizing the read reference sweep scheme [19]. During the read operation of a page, for every step of the sweep voltage, we get the digital state (0/1) of each cell of the page with respect to the applied sweep voltage. The noisy behavior

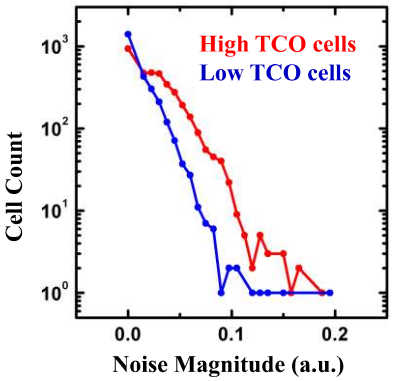

Fig. 7. Comparison of read noise magnitude for high TCO (red) and low TCO (blue) cells.

of the cells is indicated by random flips of cell states during the sweep until the cell state stabilizes at a final value. A stable cell state indicates that the sweep voltage has crossed the analog noise amplitude of the cell. This noisy behavior arises mainly from the random scattering of electrons by the GBs along poly-Si channel, or the traps located in the oxide-channel interface [15], [20]-[22]. We define the noise magnitude of the cells from the difference between the sweep voltage value when the first time the bit state shows a flip and voltage value when the bit state flips for the last time and stabilizes. Fig. 7 compares read-noise magnitudes of high TCO cells (red) and low TCO cells (blue) in terms of distributions. The high and low TCO cells are identified and tracked from Fig. 5(a) and (b). Fig. 7 clearly demonstrates that high TCO cells have higher noise amplitude. According to our hypothesis, high TCO cells have higher m-factor, and hence their read-noise have higher magnitudes.

V. Potential Countermeasures

Given that cell-to-cell variability is the root-cause for cross-temperature V_{th} distribution broadening, improvement in channel materials and process conditions [6], [16] are crucial to minimize the impact of cross-temperature effects on 3D NAND reliability. In addition to process improvements, system-level countermeasures can also contribute to mitigating cross-temperature effects, as illustrated in the following.

A. Temperature-dependent Sensing Scheme

The first proposed solution involves the application of a temperature-aware dynamic I_{sense} level to narrow the V_{th} distribution during cross-temperature read operations. This concept is illustrated in Fig. 8 using three representative I-V characteristics. We assume that the memory is programmed at room temperature (RT), and consequently, all three I-V curves intersect at the sense current level. It is important to note that when the same cells are sensed at a lower temperature, the crossing point in the I-V plot is lowered due to differential I-V shift based on their sub-threshold slope factors. By sensing the cells at this new crossing level, we anticipate a minimal spread in the sensed V_{th} values of these three cells. Similar mechanism is observed in the case of read operation at high temperature where we observe the I-V crossing point is moved to a high I_{sense} value.

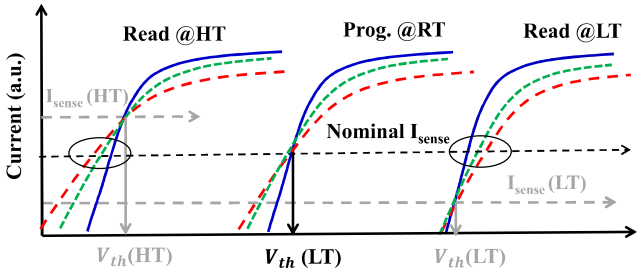

Fig. 8. Temperature aware dynamic V_{th} sensing scheme

In essence, rather than maintaining a fixed sense current across different temperatures, adjusting its value based on the temperature during read operations can minimize distribution broadening. Specifically, lowering the sense current level when reading at low temperatures and increasing it when reading at high temperatures can achieve this goal. While the concept of dynamic I_{sense} holds the promise of reducing cross-temperature V_{th} distribution broadening, successful implementation might necessitate a significant redesign of the cell sensing circuitry [23]. Moreover, the potential effects of varying the sense current, such as increased read noise at lower current values, need careful evaluation for a successful deployment.

B. Temperature-dependent Programming Scheme

The second proposal involves a variability-aware programming scheme, illustrated in Fig. 9(a) and (b). Fig. 9 demonstrates the concept using two extreme groups of cells-high TCO (red) and low TCO (blue). The selective programming of these two cell groups based on the program temperature has the potential to minimize cross-temperature distribution broadening. For instance, Fig. 9(a) shows that red cells are selectively positioned at the lower tail, while blue cells are placed at the upper tail within the programmed distribution at HT. Consequently, red cells, being the high TCO ones, will experience a higher V_{th} increase, while the blue cells, being the low TCO ones, will undergo a smaller V_{th} increase during LT sensing. However, since the red cells are placed in the lower tail of the distribution and the blue cells are in the upper tail, they will ultimately achieve similar V_{th} levels at LT, effectively reducing the V_{th} distribution broadening. Note that the relative positioning of the high and low TCO cells within the programmed V_{th} distribution at LT is reversed as shown in Fig 9(b). At LT, high TCO cells need to be placed at the upper tail and low TCO cells need to be programmed at lower tail to minimize the cross-temperature distribution broadening.

To implement the cell TCO-aware programming scheme, the initial step involves identifying high TCO and low TCO cells within the targeted page through preliminary cell characterization [24]. Once these cells are identified, a modified cell programming scheme must be employed to specifically program them to predefined locations within the V_{th} distribution. For instance, utilizing a partial program operation can position a group of cells in the lower tail of the distribution. Alternatively, different program verify levels can be applied, depending on cell TCO, to selectively place cells within the V_{th} distribution. It is critical to note that identifying cell TCO in a memory page and placing them in desired locations within the

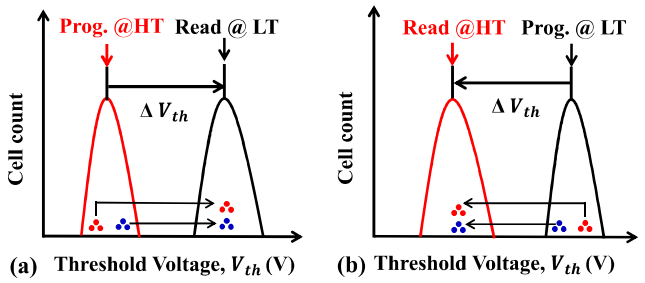

Fig. 9. Cell TCO aware programming scheme at (a) HT and (b) LT. Red dots are cell with high TCO and blue dots are low TCO cells.

programmed distribution will necessitate significant modifications to the traditional page programming algorithm. Consequently, this approach may increase the nominal page program time. Nevertheless, the proposed method presents an intriguing trade-off for enhancing cross-temperature reliability at the expense of programming time.

VI. Conclusions

In conclusion, this paper presents experimental evidence showcasing cross-temperature V_{th} distribution broadening effects in commercial 3D NAND Flash memory. We identify two groups of cells having very high TCO and low TCO and analyze their properties. We posit that sub-threshold slope variation of memory cells plays a pivotal role in causing the V_{th} distribution broadening during cross temperature read. Moreover, we propose two system-level countermeasures—one applicable during read operation and the other during program operation—to effectively mitigate the impact of cross-temperature effects on memory reliability.

Acknowledgment

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