Origin of Post-Irradiation V_{th}-Shift Variability in 3-D NAND Memory Array

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***Abstract*— In this article, we report total-ionizing-dose (TID)-induced threshold-voltage (V_{th}) shift characteristics of commercial-off-the-shelf (COTS) 64-layer 3-D NAND flash memory chips. Our measurements of cell V_{th} distributions after irradiation up to 50 krad(Si) indicate that significant V_{th}-shift variability exists among the memory cells of the chip. We find that a certain fraction of cells is very responsive to ionizing irradiation while a significant amount of the cells stays surprisingly resilient. We model the TID-tolerance behavior of these cells using pre-existing trap states in the tunnel oxide and provide three independent supporting evidence.**

***Index Terms*— 3-D NAND, threshold voltage distribution, total ionizing dose (TID).**

I. Introduction

NAND flash memory has been the primary choice for permanent storage of data and code in a wide range of computing systems found in consumer electronics, automotive, military, nuclear, and space applications. Two-dimensional NAND flash memories served the electronics systems for more than two decades by continuously scaling down the dimensions [1], but over the last few years, the flash memory industry has moved into 3-D NAND flash technologies as the 2-D NAND flash memories faced inevitable technology scaling saturation and unavoidable reliability issues fueled by the smaller dimensions in planar technology [1]. The unique cylindrical structure of 3-D NAND memories and the growth in the vertical direction revitalized the memory capacity growth and improved the reliability characteristics significantly [2].

Besides being an integral part of high-density data storage application in consumer electronics, NAND flash memories are the most promising candidate for space applications because of its lightweight, fast read/write speed, massive bit density, and low operating power consumption [3]. However, flash technology is vulnerable to total-ionizing-dose (TID) effects [3], [4], [5], [6], [7], [8]. When exposed to ionizing radiation, NAND flash memory can experience data corruption, primarily through the loss of threshold voltage (V_{th}) and the creation of defect states in the oxide layers of flash cells. These radiation-induced effects ultimately lead to a degradation in both the reliability and overall performance of the NAND flash memory [9], [10], [11]. Therefore, understanding and mitigating the impact of TID effects on NAND flash memory are critical for ensuring its reliability and suitability for use in space applications, where exposure to ionizing radiation is a significant concern.

Previous research has primarily focused on investigating the TID effects on the V_{th} distribution of commercial-off-the-shelf (COTS) memory chips [3], [4]. However, the proprietary nature of V_{th} measurement procedures has hindered the availability of precise V_{th} shift values as a function of TID in the published literature. Additionally, there is an absence of published reports regarding cell-by-cell V_{th} shift analysis, which is crucial for understanding the variability of cell response to TID effects. Interestingly, the latest generation of 3-D NAND memory chips offers several additional commands to end users, facilitating cell V_{th} measurements without requiring any privileged or proprietary information from the NAND vendors [12]. This presents a valuable opportunity to gain deeper insights into the effects of TID on individual cells, enhancing our understanding of the underlying mechanisms and enabling better strategies to counteract TID-induced degradation in NAND flash memory.

In this article, we utilize the recently released user-mode NAND commands to perform cell V_{th} measurement from 64-layer COTS 3-D NAND memory chips. We perform irradiation experiment using Co-60 source on the COTS 3-D NAND parts and measure V_{th} shift of the memory array due to irradiation. Our measurement not only computes V_{th} shift values as a function of TID but also quantifies cell-by-cell V_{th} shift variability. Interestingly, we find that a certain fraction of memory cells of the 3-D NAND array is relatively tolerant to TID effects, even though they are programmed to the highest V_{th} state of triple-level cell (TLC) memory before irradiation. We systematically analyze the properties of the

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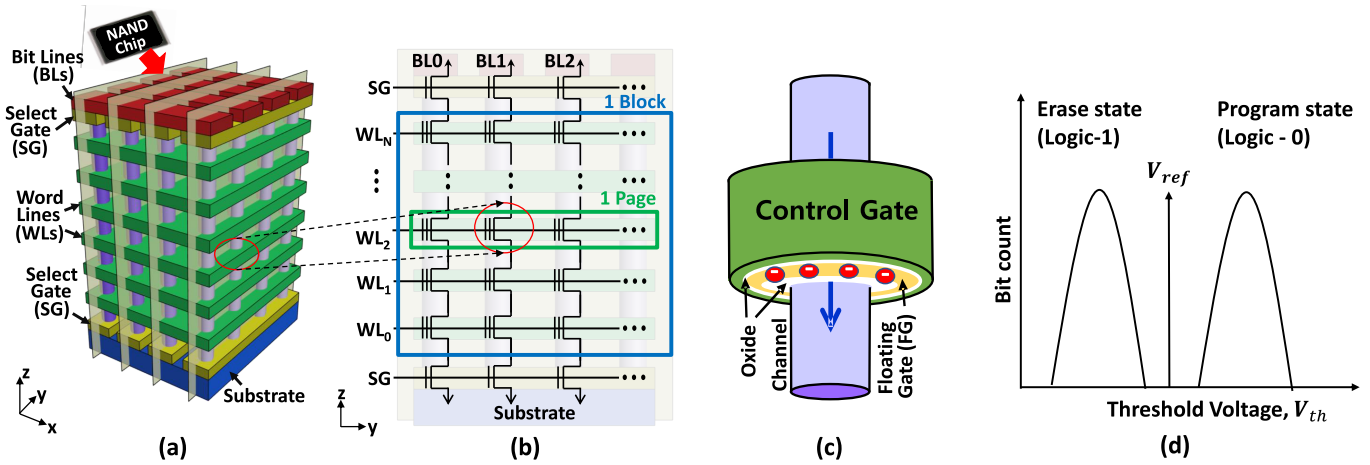

Fig. 1. (a) Schematic of a 3-D NAND flash memory block. (b) Circuit diagram of a physical subblock structure. (c) Schematic of a 3-D NAND memory cell. (d) Cell V_{th} distribution in SLC memory.

so-called "TID-tolerant" cells and provide a physical model to explain their TID tolerance. Our findings have a far-reaching implication for understanding the TID-induced V_{th} variability in the 3-D NAND memory array. Additionally, they offer valuable insights that can inform the design of future radiation-tolerant 3-D NAND memory systems.

This article is organized as follows. Section II discusses the background. Section III shows the experimental setup for the measurements. Section IV shows the experimental results and discusses the findings. Finally, Section V concludes this article.

II. Background

Three-dimensional NAND flash memory is designed to vertically stack multiple layers containing flash memory cells on top of each other to achieve higher bit density [2]. Fig. 1(a) illustrates the physical organization of a 3-D NAND flash memory block. The green layers represent the word lines (WLs) of the memory array. The red bars at the top of the schematic represent the bit lines (BLs), while the purple pillars are the poly-silicon (poly-Si) channels. The blue region at the bottom represents the Si substrate, whereas the yellow bars on top of it are the source select gate (SSG) transistors. A similar yellow bar is shown near the BLs, which are called drain select gate (DSG) transistors. Select transistors are used to select a particular block during read, write, and erase operations.

Fig. 1(b) illustrates the circuit schematic of a physical block of a NAND flash memory array. Each block contains a certain number of flash pages, while each flash page consists of a number of flash cells. The page size generally varies from 2 to 16 kB, depending on the manufacturer. All cells in the same row share the same WL. The cells in a vertical column connect to a metal BL via DSG and to the ground via SSG at the bottom. Thus, the BL can be pulled down to the ground only if all flash transistors in the column are active (resembling the operation of the NAND gate).

The structure of a 3-D NAND cell is shown in Fig. 1(c). It is a gate-all-around (GAA) transistor with a floating gate (FG) or charge trap (CT) layer. Data are stored in the form of the electronic charge in the FG/CT layer. Electrons on the FG will increase the cell's V_{th}, and such a cell is in a programmed state representing logic "0." Removing electrons from the FG lowers the cell's V_{th}, and such a cell is in an erased state representing logic "1." Traditional flash memory cells store one bit of information [single-level cell (SLC)], and they can be in two different V_{th} states, as shown in Fig. 1(d). The read reference voltage (V_{ref}) is set in between the erased state and programmed state distributions, so that there is enough noise margin to correctly identify the cells' states. Recent advances in controlling the amount of charge on the FG and in sensing the charge during a read operation, allowed for logical scaling, further increasing bit density. Thus, modern flash memories store 2 bits [multi-level cell (MLC)], 3 bits (TLC), and even 4 bits [quad-level cell (QLC)] [1].

III. Experimental Setup

The experimental evaluation was performed on two COTS 3-D NAND memory chips from Micrometer Technologies. The part number of the chips is MT29F256G08EBHAFJ4 (256 Giga bit). Each chip contains 1008 logical blocks, where each block consists of 2304 logical pages of size 18 592 B (16 384 B of user data with 2208 B of error correction codes or ECC). The chips are fabricated with FG technology. It consists of 64 vertical layers manufactured using monolithic 3-D fabrication process. The flash memory chips are irradiated using Co-60 sources to evaluate their TID response at a dose rate of 11.7 krad(Si)/h. All doses are expressed as absorbed dose in Si. The irradiation experiment is performed at Ohio State University Nuclear Reactor Laboratory using an underwater Co-60 irradiator [13]. The gamma irradiator consists of a vertically extending 6-in diameter dry tube positioned within a light water pool. Twenty-five Co-60 pins were placed around the tube to ensure a uniform radiation field featuring gamma rays at energies of 1.173 and 1.332 MeV. Gamma irradiation was performed on packaged devices with all pins grounded. The direction of gamma rays during irradiation was perpendicular to the top surface of the chip. To interface the raw NAND chip with the computer, we used a custom-designed hardware board. The hardware setup [Fig. 2(a)] allows us to

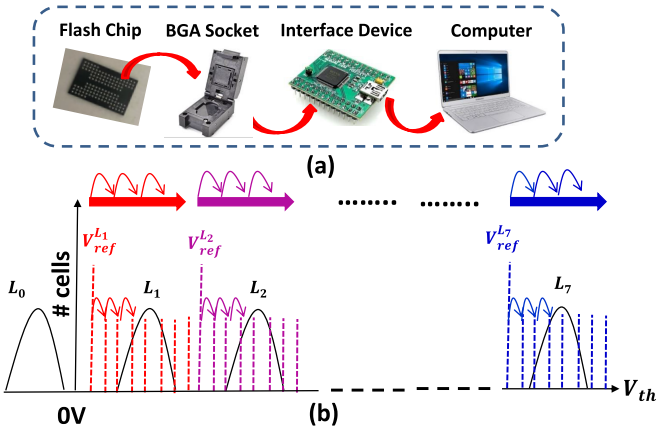

Fig. 2. (a) Experimental setup. (b) Illustration of V_{th} distribution measurement method using read-offset commands.

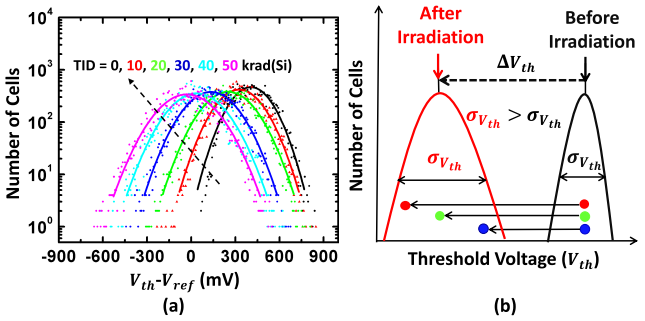

Fig. 3. (a) Measured data on cell V_{th} distribution as a function of TID, with mean shifting from 405 mV [0 krad(Si)] to −30 mV [50 krad(Si)] and standard deviation increasing from 121 to 166 mV. (b) Illustration of V_{th} distribution widening.

access raw memory bits without error correction. There was a time gap of approximately 1hr between irradiation and data readout.

The chip under test supports the so-called read offset operations that allow the flash controller to measure cell-by-cell V_{th} with 7.5-mV resolution. Fig. 2(b) illustrates the read offset method. For a TLC memory, there are seven distinct read reference voltages as follows: $V_{\text{ref}}^{L_1}, \ldots, V_{\text{ref}}^{L_7}$. Here, $V_{\text{ref}}^{L_i}$ is the default read reference voltage for the corresponding program state L_i. The read offset operation utilizes an internal digital-to-analog converter to incrementally add an offset voltage to the read reference voltage based on the digital value given in the command. Thus, it shifts the reference voltage from the default level to $V_{\text{ref}}^{L_i} + \Delta V \times i$, where $i = 0, \pm1, \pm2, \ldots, \pm127$. For the chip under investigation, $\Delta V = 7.5$ mV. For each shifted $V_{\text{ref}}^{L_i}$, we read data from the corresponding pages. For example, by shifting $V_{\text{ref}}^{L_7}$ from its default value to the right by ∼952 mV in steps of 7.5 mV, we can extract the distribution of the L_7 state. The same process is repeated for the other cell states. The exact process is repeated for the other cell states. This way, we can extract the V_{th} distributions of all memory cell states. The detailed instructions to retrieve V_{th} values from the chips under test are available in corresponding datasheet accessible on manufacturer's website. The command sequence to implement read offset operation for open NAND flash interface (ONFI [14])-compliant memory is as follows.

1) Send command SET FEATURES (0xEF).
2) Send address for read offset levels (0xA0-0xAC).
3) Send parameter for offset voltages (0x00.0xFF).
4) Send page address.
5) Send command PAGE READ.

Please be aware that we have examined the impact of irradiation on the V_{th} measurement circuit of the chip as follows. We freshly programmed a new memory block on the irradiated chip and subsequently measured the V_{th} distribution, which we refer to as the "as-programmed V_{th} distribution." The as-programmed V_{th} distribution of the irradiated chip aligns well with the as-programmed V_{th} distribution of the same chip before irradiation, indicating negligible degradation of the V_{th} measurement circuit.

IV. Results and Discussion

A. TID Effects on Cell V_{th} Distributions

Fig. 3(a) shows the measured cell V_{th} distribution for different TIDs. The dots in the figure represent measured data points, whereas solid lines stand for fitted Gaussian curve for each distribution. The black curve represents V_{th} distribution before irradiation or TID = 0 krad(Si). The cell V_{th} distribution is measured from a TLC memory page. The plotted distribution represents the highest program level (L_7) in the TLC memory. For clarity of the discussion, we will limit our analysis based on the L_7 state. However, a similar conclusion can be derived based on any other programmed state. Cell V_{th} distribution measured after irradiation is shown with different colors corresponding to different TID values. We note that V_{th} distribution shifts down with increasing TID. In addition, V_{th} distribution significantly widens with higher TID. The root cause of TID-induced V_{th} downshift is typically explained through trapped holes in the oxide layer after irradiation [3], [4], [15], [16], [17]. However, the origin of V_{th} distribution widening is less explored in the published literature [4], [15], [18].

Fig. 3(b) provides a simplified schematic that illustrates the origin of V_{th} distribution widening. To enhance the clarity of our discussion, we have selected three representative cells with varying degrees of V_{th} shift after irradiation. Among these cells, the one with the least V_{th} shift is referred to as the so-called "TID-tolerant" and it is visually represented in blue color in the figure. The cell whose V_{th} is shifted the most is termed as "TID-prone" cell shown with red dot in the figure. The other cells that experience median V_{th} shift is termed as median cells (green). This cell-to-cell variability in TID-induced V_{th} shift widens the V_{th} distribution after irradiation. In the following, we further analyze these three groups of cells with more experimental evaluation.

B. Cell-by-Cell Analysis of TID-Induced V_{th} Shift

Fig. 4(a) shows a scatter plot of cell-by-cell V_{th} shift (or ΔV_{th}) values measured after irradiation. Here, ΔV_{th} is defined as follows: $\Delta V_{\text{th}} = V_{\text{th}}$ [50 krad(Si)]$-V_{\text{th}}$ [0 krad(Si)]. Thus, negative ΔV_{th} values indicate V_{th} loss. All the cells were programmed at the highest V_{th} state of a TLC memory before irradiation. Our analysis reveals a notable variation in V_{th}

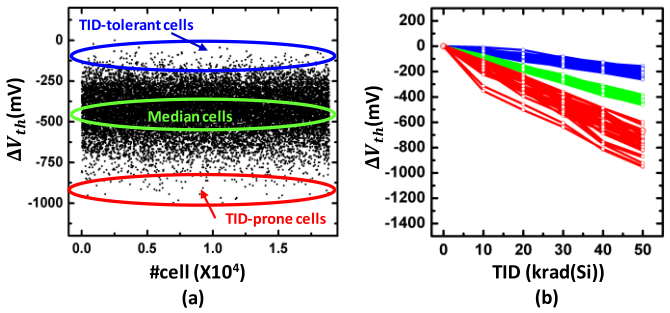

Fig. 4. (a) Cell-by-cell ΔV_{th} values after irradiation [TID = 50 krad (Si)]. (b) Cell-by-cell V_{th} loss trajectory for TID-tolerant (blue), median (green), and TID-prone (red) cells.

loss values among individual cells. Particularly interesting is the presence of a substantial number of cells that exhibit minimal V_{th} loss (<0.2 V), even after exposure to a TID of 50 krad(Si). We classify these cells as TID-tolerant cells (blue). On the other hand, there exists another group of cells that demonstrate significant V_{th} loss, surpassing 0.6 V, and these are referred to as TID-prone cells (red). In Fig. 4(b), we present a detailed representation of the V_{th} shift behavior for these two groups of cells, alongside the behavior of median cells, at each step of irradiation dose. To facilitate our subsequent discussion, we will establish clear definitions for the different cell types based on their V_{th} shifts after exposure to TID = 50 krad(Si). TID-tolerant cells, represented by blue cells, are those cells that experience a $\Delta V_{\text{th}} < 0.2$ V after TID exposure. Conversely, TID-prone cells, depicted by red cells, are defined as cells with $\Delta V_{\text{th}} > 0.7$ V after TID exposure. Finally, the remaining cells, characterized by a ΔV_{th} between 0.2 and 0.7 V after TID exposure, will be referred to as median cells or green cells. These clearly defined categories enable us to distinguish and study the distinct responses of individual cells to TID effects, providing valuable insights into the variability observed in the NAND flash memory array and shedding light on the origin of V_{th} distribution widening.

C. Hypothesis: Origin of TID-Tolerant Cells

The cell-to-cell variability of TID-induced V_{th} loss can be explained using the energy band diagrams of programmed flash memory cells, with all their terminals grounded, as shown in Fig. 5(a) and (b). Fig. 5(a) represents a memory cell with minimal oxide defects, and hence, we assume all the electrons are stored on the FG after program operation. On the other hand, Fig. 5(b) portrays our model of a TID-tolerant cell, which contains a significant density of defect states in the tunnel oxide layer, near the poly-Si channel interface. During the program operation, these defect states may capture electrons, leading to fewer electrons being stored on the FG after the program operation. It is important to note that both cells may have the same programmed V_{th}, but the location of stored electrons differs substantially. Since the program operation in NAND flash memory takes place through incremental step pulse programming (ISPP) sequence [19], it ensures that the targeted cells reach the same V_{th} distribution. The ISPP scheme, however, has no control on the exact placement of electrons within the gate-stack even though it aims to put all the electrons on the FG. Due to the inherent randomness in the charge injection process and the presence of oxide trap states, many electrons get trapped in the tunnel oxide instead of being stored on the FG. Thus, each cell can have a statistically different profile of stored electron distribution in the oxide but ultimately can have the same V_{th} distribution. Nevertheless, the location of electrons dictates the electric field distribution in the oxide layers, which critically affects the TID response of the cell. Next, we explain the role of electric field on the TID-induced charge yield in the oxide layers, which will clarify the higher TID tolerance of Fig. 5(b) cell.

Ionizing radiation within the insulating oxide layers creates electron–hole pairs. Some of these generated electrons escape recombination and are swept off the oxide due to the oxide field, while the remaining holes either become trapped in the oxide or drift toward the FG, where they annihilate stored electrons resulting in a net positive charge yield [15]. However, when the oxide field is weak, electron–hole recombination occurs in the oxide, leading to insignificant charge yield. Fig. 5(c) illustrates the field-dependent charge yield for SiO_2 material under gamma irradiation, which has been previously characterized and replotted [20], [21]. Remarkably, the electric field in the oxide layers of a flash memory cell during irradiation is a critical factor determining its TID response. Note that the blocking oxide thickness, being much greater than the tunnel oxide thickness, plays a crucial role in determining the net positive charge yield induced by irradiation. In the case of Fig. 5(b) cell, the electric field within the blocking oxide is significantly lower compared to that of Fig. 5(a) cell, leading to a considerably lower net positive charge yield. This explains the origin of TID tolerance of Fig. 5(b) cell.

Next, we provide a quantitative estimate of the reduction in charge yield due to electron trapping in the oxide. In general, TID-induced charge (hole) yield (n_h) in the oxide layers can be modeled by the following equation:

$$\boldsymbol{n_h} = \left(\boldsymbol{f(E_{ox})} \times \boldsymbol{g_{ox}} \times \boldsymbol{v_{ox}} + \boldsymbol{f(E_{box})} \times \boldsymbol{g_{box}} \times \boldsymbol{v_{box}}\right) \times \mathbf{TID} \quad (1)$$

where $f(E_{\text{ox}})$ is the probability of charge yield in tunnel oxide, $f(E_{\text{box}})$ is the probability of charge yield in blocking oxide, $\boldsymbol{g_{ox}}$ and $\boldsymbol{g_{box}}$ are the ionization constant values in the tunnel and blocking oxides, $\boldsymbol{v_{ox}}$ is the tunnel oxide volume, and $\boldsymbol{v_{box}}$ is the blocking oxide volume for a memory cell. Assuming typical values for the dimensions of the oxide layers (tunnel oxide thickness = 8 nm and blocking oxide thickness = 16 nm) from the published literature [22], we can estimate the field in the blocking oxide and tunnel oxide to be $E_{\text{box}} = 1.72$ MV/cm and $E_{\text{tox}} = 3.46$ MV/cm, respectively, when the cell is in the highest V_{th} state (L_7) of TLC distribution [assuming $V_{\text{th}}(L_7) = 7$ V]. The blocking oxide field on a typical cell is along the knee of the charge-yield plot, as shown in Fig. 5(c). The charge trapping along the oxide–channel interface will lower down the blocking oxide field, which will significantly lower charge yield. For example, if we assume that 50% of the electrons get trapped at the interface during program operation, the new field in the blocking oxide becomes $E_{\text{box}} = 0.6$ MV/cm, which will reduce the charge yield to be only

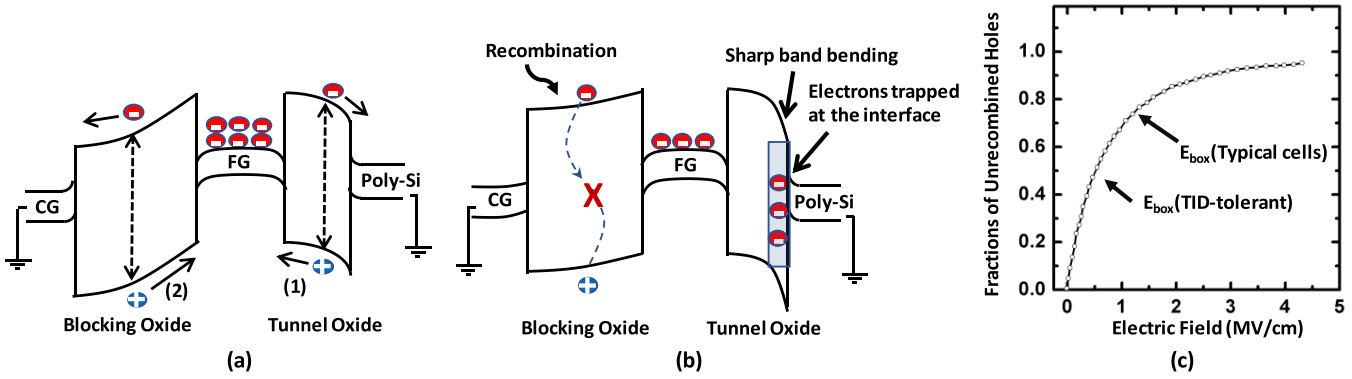

Fig. 5. (a) Energy band diagram of programmed memory with minimal oxide defects. (b) Energy band diagram of a TID-tolerant cell in the programmed state; because of weaker electric field recombination of irradiation-generated electrons and holes are dominant here in blocking oxide causing lower positive charge yield. (c) Fraction of TID-induced holes that remains unrecombined in SiO_2.

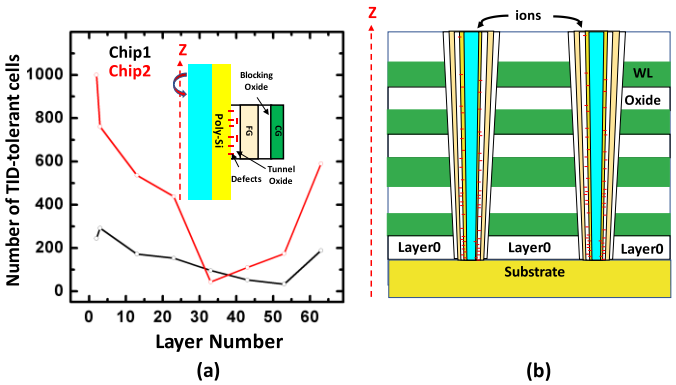

Fig. 6. (a) Measured TID-tolerant cell counts as a function of vertical layer number for two different 3-D NAND chips. A one-sided vertical cross section of a 3-D NAND cell with defects in the channel–tunnel interface is shown in the inset. (b) Illustration of the tapered shape geometry of the 3-D NAND channel. Due to inefficient RIE process, the bottom layers of the stack are intrinsically defect-prone.

50%. Please note that electron trapping can happen at any position of the tunnel oxide, such as in the border traps, poly-Si/tunnel oxide interface, as well as FG/tunnel oxide interface. A detailed simulation of electrostatic field distribution in the oxide with various possible positions of the trapped electrons, as described by Xiao et al. [23], is needed to accurately estimate the charge-yield factor in these devices.

D. Supporting Evidence for Our Hypothesis

In this section, we provide three independent supporting evidence behind the defect-induced TID tolerance of a flash memory cell. The first evidence is shown in Fig. 6(a), where we show the number of TID-tolerant blue cells as a function of layer number of the 3-D memory stack. We find that the bottom layers of the 3-D stack contain a greater number of TID tolerant cells. We explain this observation using Fig. 6(b), which shows the schematic cross section of the 3-D NAND array. Note that the 3-D NAND array possesses a tapered structure due to the reactive ion etching (RIE) process, which is a critical step during its fabrication [1], [2], [8], [24]. The RIE process is particularly inefficient in the bottom layers creating the tapered shape. The gate-stack, blocking oxide, charge storage layer, and the tunnel oxide layers are formed along the sidewall of the cylindrical trench. Due to this unique and not so perfect fabrication process [1], [2], [8], [24], cells in the bottom layers intrinsically possess a significant defect density, especially in the channel poly-Si–tunnel oxide interface region.

Fig. 6(b) shows a simplified vertical cross section of a 3-D NAND array with oxide–channel interfacial defects. According to our hypothesis, 3-D NAND cells with intrinsic defects in the channel–tunnel oxide interface region experience a weakening of the oxide fields and exhibit resilience to radiation-induced electron–hole pair creation. Consequently, one would anticipate a higher prevalence of TID-tolerant cells in the bottom oxide region of the 3-D NAND stack. Consequently, the measurement results depicted in Fig. 6(a) are consistent with our interpretation of TID-tolerant cells. In other words, our hypothesis regarding interface defects in flash cell provides a plausible explanation for the experimentally observed variable V_{th} shifts in memory cells after irradiation.

We designed a second experiment to consolidate our hypothesis by irradiating a 3-D NAND chip two times. At first, several blocks of a fresh 3-D NAND chip were programmed and irradiated up to 50 krad(Si). After the irradiation was complete, we performed one set of measurements, and the number of TID-tolerant cells was calculated. Afterward, the programmed blocks of the irradiated chip were erased completely and those blocks were reprogrammed with the same data pattern and another 50 krad(Si) dose of irradiation was applied. After the second round of irradiation, another set of measurements was performed to find out the number of TID-tolerant cells. In Fig. 7(a), the numbers of the TID-tolerant cells measured after the first round of irradiation and after the second round of irradiation are shown. Fig. 7(a) shows that the number of TID tolerant cells significantly increases during the second round of irradiation. This result, in fact, supports our hypothesis. When a 3-D NAND chip is irradiated in round1, some additional defects are created in the oxides (especially in the tunnel oxide). Fig. 7(b) shows a typical programmed 3-D NAND cell, which has few defects in the tunnel oxide. After one round of irradiation, newer defects are created in the tunnel oxide and along the tunnel–poly-Si interface. After round1

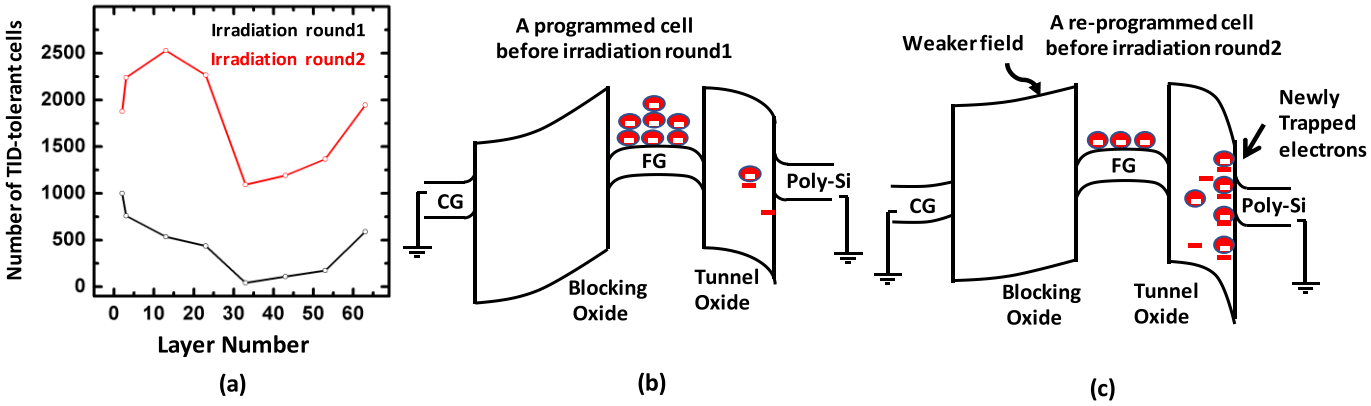

Fig. 7. (a) Number of TID-tolerant cells during two sets of irradiations [TID = 50 krad(Si)] on the same chip. A 3-D NAND cell. (b) Freshly programmed before irradiation round1. (c) Erased and reprogrammed before irradiation round2.

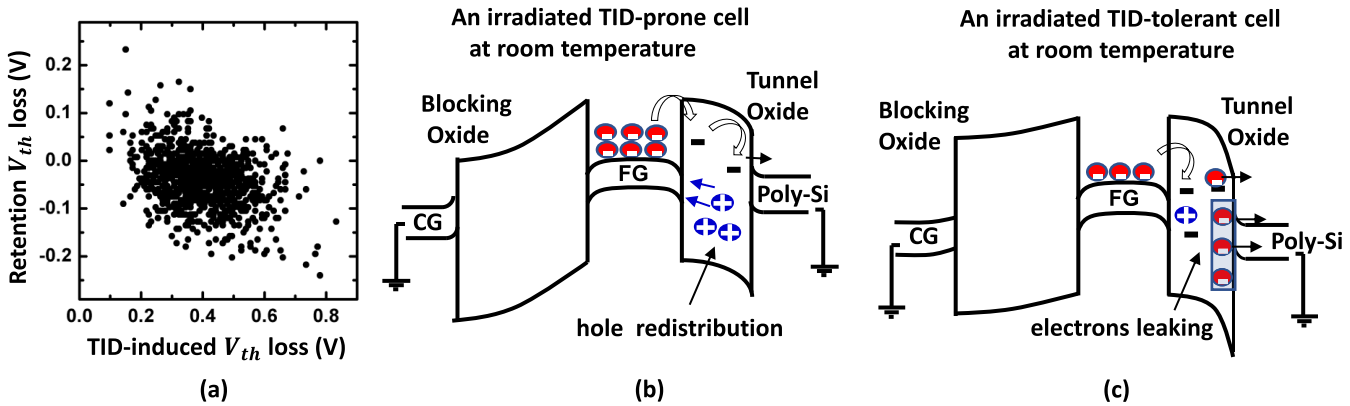

Fig. 8. (a) V_{th} shift of cells measured right after irradiation [TID = 50 krad(Si)] and after six months of room temperature retention. A 3-D NAND. (b) TID-prone cell idle at room temperature after being irradiated [TID = 50 krad(Si)]. (c) TID-tolerant cell idle at room temperature after being irradiated [TID = 50 krad(Si)].

irradiation, when the cell was erased and reprogrammed, these new traps along with the previously existing interface traps were filled with electrons making the blocking oxide field weaker [Fig. 7(c)] and this modified cell started to behave as a TID-tolerant cell. This is why, during the second round of irradiation, the number of TID-tolerant cells has increased significantly. This result strongly supports our hypothesis of TID-tolerant cells' origin.

As a final experiment to further bolster our argument for the TID-tolerant cells, we preserved the irradiated 3-D NAND chips at room temperature for six months. Fig. 8(a) shows the V_{th} shifts of 3-D NAND cells measured just after irradiation (x-axis) and after six months of room temperature retention (y-axis). Here, on the y-axis, negative V_{th} loss indicates V_{th} gain. Fig. 8(a) reveals that a significant number of memory cells that were typically immune to V_{th} loss during irradiation (TID-tolerant cells) lost some V_{th} over six months. On the flip side, another fraction of cells that were TID-prone during irradiation showed a surprising behavior. Those cells, in fact, gained some V_{th} over the six-month time. To explain this result, we present the band diagrams in Fig. 8(b) and (c). In case of a TID-tolerant cell [Fig. 8(c)], the electrons stored in the interface defects detrap relatively quickly causing significant V_{th} loss within a few months at room temperature. On the other hand, TID-prone cells do not have enough interface defects to facilitate fast charge loss. The holes that were trapped in blocking/tunnel oxide of TID-prone cells during irradiation slowly redistribute within the oxide layer causing slight V_{th} gain. However, the median cells do not show any significant change in V_{th} in the six-month time. The retention characteristics shown by the TID tolerant cells further strengthen our hypothesis on the origin of defect-induced V_{th} shift variability after irradiation.

V. Conclusion

In summary, we conclude that the variability in cell-to-cell V_{th} shifts most likely originate from the trap states present at the tunnel oxide and poly-Si interface. Depending on the density of interface traps, we observe two distinct groups of cells: TID-tolerant (more traps) and TID-prone (fewer traps). Our characterization results reveal three significant properties of TID-tolerant cells: 1) they are relatively more abundant in the lower layers of the 3-D stack; 2) their number increases after irradiation; and 3) they experience a notable reduction in V_{th} during room temperature retention. Hence, the findings of this study have profound implications for the design of TID-tolerant 3-D NAND flash memory, as they suggest the possibility of engineering interface trap states to strike a

balance between TID tolerance and long-term data retention characteristics.

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REFERENCES

[1] C. M. Compagnoni, A. Goda, A. S. Spinelli, P. Feeley, A. L. Lacaita, and A. Visconti, "Reviewing the evolution of the NAND flash technology," *Proc. IEEE*, vol. 105, no. 9, pp. 1609–1633, Sep. 2017.

[2] A. Goda, "3-D NAND technology achievements and future scaling perspectives," *IEEE Trans. Electron Devices*, vol. 67, no. 4, pp. 1373–1381, Apr. 2020.

[3] S. Gerardin et al., "Radiation effects in flash memories," *IEEE Trans. Nucl. Sci.*, vol. 60, no. 3, pp. 1953–1969, Jun. 2013.

[4] M. Bagatin et al., "Total ionizing dose effects in 3-D NAND flash memories," *IEEE Trans. Nucl. Sci.*, vol. 66, no. 1, pp. 48–53, Jan. 2019.

[5] M. J. Gadlage, M. J. Kay, J. D. Ingalls, A. R. Duncan, and S. A. Ashley, "Impact of X-ray exposure on a triple-level-cell NAND flash," *IEEE Trans. Nucl. Sci.*, vol. 60, no. 6, pp. 4533–4539, Dec. 2013.

[6] F. Irom, D. N. Nguyen, M. L. Underwood, and A. Virtanen, "Effects of scaling in SEE and TID response of high density NAND flash memories," *IEEE Trans. Nucl. Sci.*, vol. 57, no. 6, pp. 3329–3335, Dec. 2010.

[7] U. Surendranathan, P. Kumari, M. Wasiolek, K. Hattar, T. Boykin, and B. Ray, "Gamma-ray-induced error pattern analysis for MLC 3-D NAND flash memories," *IEEE Trans. Nucl. Sci.*, vol. 68, no. 5, pp. 733–739, May 2021.

[8] P. Kumari, S. Huang, M. Wasiolek, K. Hattar, and B. Ray, "Layer-dependent bit error variation in 3-D NAND flash under ionizing radiation," *IEEE Trans. Nucl. Sci.*, vol. 67, no. 9, pp. 2021–2027, Sep. 2020.

[9] M. Buddhanoy, P. Kumari, U. Surendranathan, M. Wasiolek, K. Hattar, and B. Ray, "Total ionizing dose effects on long-term data retention characteristics of commercial 3-D NAND memories," *IEEE Trans. Nucl. Sci.*, vol. 69, no. 3, pp. 390–396, Mar. 2022.

[10] U. Surendranathan, M. Wasiolek, K. Hattar, D. M. Fleetwood, and B. Ray, "Total ionizing dose effects on read noise of MLC 3-D NAND memories," *IEEE Trans. Nucl. Sci.*, vol. 69, no. 3, pp. 321–326, Mar. 2022.

[11] T. R. Oldham, D. Chen, M. Friendlich, M. A. Carts, C. M. Seidleck, and K. A. LaBel, "Effect of radiation exposure on the retention of commercial NAND flash memory," *IEEE Trans. Nucl. Sci.*, vol. 58, no. 6, pp. 2904–2910, Dec. 2011.

[12] M. A. Kumar et al., "Total-ionizing-dose effects on threshold voltage distribution of 64-layer 3D NAND memories," in *Proc. IEEE Radiat. Effects Data Workshop (REDW)*, Provo, UT, USA, Jul. 2022, pp. 1–5.

[13] C. Tan et al., "Ex-situ and in-situ observations of the effects of gamma radiation on lithium ion battery performance," *J. Power Sources*, vol. 357, pp. 19–25, Jul. 2017.

[14] *Home—ONFI*. Accessed: Oct. 9, 2023. [Online]. Available: http://www.onfi.org/

[15] E. S. Snyder, P. J. McWhorter, T. A. Dellin, and J. D. Sweetman, "Radiation response of floating gate EEPROM memory cells," *IEEE Trans. Nucl. Sci.*, vol. 36, no. 6, pp. 2131–2139, Dec. 1989.

[16] G. Cellere, A. Paccagnella, A. Visconti, M. Bonanomi, P. Caprara, and S. Lora, "A model for TID effects on floating gate memory cells," *IEEE Trans. Nucl. Sci.*, vol. 51, no. 6, pp. 3753–3758, Dec. 2004.

[17] J. Cao et al., "Total-ionizing-dose effects on polycrystalline-Si channel vertical-charge-trapping NAND devices," *IEEE Trans. Nucl. Sci.*, vol. 69, no. 3, pp. 314–320, Mar. 2022.

[18] P. Kumari, U. Surendranathan, M. Wasiolek, K. Hattar, N. Bhat, and B. Ray, "Analytical bit-error model of NAND flash memories for dosimetry application," *IEEE Trans. Nucl. Sci.*, vol. 69, no. 3, pp. 478–484, Mar. 2022.

[19] M. Raquibuzzaman, A. Milenkovic, and B. Ray, "EXPRESS: Exploiting energy–accuracy tradeoffs in 3D NAND flash memory for energy-efficient storage," *Electronics*, vol. 11, no. 3, p. 424, Jan. 2022.

[20] T. R. Oldham and F. B. McLean, "Total ionizing dose effects in MOS oxides and devices," *IEEE Trans. Nucl. Sci.*, vol. 50, no. 3, pp. 483–499, Jun. 2003.

[21] J. R. Schwank et al., "Radiation effects in MOS oxides," *IEEE Trans. Nucl. Sci.*, vol. 55, no. 4, pp. 1833–1853, Aug. 2008.

[22] S. Aritome, "Study of NAND flash memory cells," Ph.D. dissertation, Graduate School Adv. Sci. Matter, Hiroshima Univ., Higashihiroshima, Japan, 2013. [Online]. Available: https://ir.lib.hiroshima-u.ac.jp/files/public/3/35129/20141016204214520096/k6228_3.pdf

[23] T. P. Xiao et al., "Ionizing radiation effects in SONOS-based neuromorphic inference accelerators," *IEEE Trans. Nucl. Sci.*, vol. 68, no. 5, pp. 762–769, May 2021.

[24] A. Grossi, C. Zambelli, and P. Olivo, "Reliability of 3D NAND flash memories," in *3D Flash Memories*, R. Micheloni, Ed., Dordrecht, The Netherlands: Springer, 2016, pp. 29–62.