

2 kV, 0.7 mΩ·cm² Vertical Ga₂O₃ Superjunction Schottky Rectifier with Dynamic Robustness

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Abstract—We report the first experimental demonstration of a vertical superjunction device in ultra-wide bandgap (UWBG) Ga₂O₃. The device features 1.8 μm wide, 2×10¹⁷ cm⁻³ doped n-Ga₂O₃ pillars wrapped by the charge-balanced p-type nickel oxide (NiO). The sidewall NiO is sputtered through a novel self-align process. Benefitted from the high doping in Ga₂O₃, the superjunction Schottky barrier diode (SJ-SBD) achieves a ultra-low specific on-resistance ($R_{ON,SP}$) of 0.7 mΩ·cm² with a low turn-on voltage of 1 V and high breakdown voltage (BV) of 2000 V. The $R_{ON,SP} \sim BV$ trade-off is among the best in all WBG and UWBG power SBDs. The device also shows good thermal stability with $BV > 1.8$ kV at 175 °C. In the unclamped inductive switching tests, the device shows a dynamic BV of 2.2 kV and no degradation under 1.7 kV repetitive switching, verifying the fast acceptor depletion in NiO under dynamic switching. Such high-temperature and switching robustness are reported for the first time in a heterogeneous superjunction. These results show the great potential of UWBG superjunction power devices.

I. INTRODUCTION

Superjunction is arguably one of the most innovative device concepts in power electronics [1]. It comprises alternate n- and p-type regions with relatively high doping and balanced charge. Benefitted from the multidimensional electrostatic engineering [2], vertical superjunction device allows a linear $R_{ON,SP}$ increase with BV , while $R_{ON,SP}$ scales with the square of BV in 1D unipolar devices. Note that the lateral superjunction is superior to the 1D counterpart but still possesses a $R_{ON,SP} \propto BV^2$ limit [2].

Vertical superjunction has achieved a commercial success in Si and has been recently demonstrated in SiC [3,4] and GaN [5]. The $R_{ON,SP} \sim BV$ trade-off of Si and WBG superjunction has surpassed their respective 1D material limits. The theoretical limits of UWBG superjunctions are even superior. However, no vertical UWBG superjunction device has been experimentally reported to date, mainly due to the difficulties in achieving the intrinsic bipolar doping in UWBG semiconductors.

A promising solution to this challenge is the heterogeneous superjunction. Recently, p-type NiO (bandgap 3.4~4 eV) was deployed to construct the vertical superjunction in GaN [5] and lateral superjunction in Ga₂O₃ [6]. Despite the report of the superjunction functionality in DC tests, its effectiveness at high temperature and in dynamic switching remain two critical gaps, particularly considering the possible hetero-interface traps and NiO's deep acceptor level (0.26~0.4 eV for the Ni vacancy [7]). These gaps have to be addressed for any power application.

This work demonstrates experimentally the first vertical Ga₂O₃ superjunction device with high performance. The Ga₂O₃ drift region is doped at least 10X higher than conventional 1D devices to aggressively reduce $R_{ON,SP}$. The charge balance with p-NiO ensures the uniform vertical electric field (E-field) and high BV . In addition to high $R_{ON,SP} \sim BV$ performance, we present three key novelties: a) a bi-layer Ga₂O₃ epi design to realize a superjunction Schottky barrier diode (SJ-SBD) with lower turn-on voltage (V_{ON}) than prior SJ-PN diodes [5]; b) a new self-align process to sputter NiO onto the deep trench sidewall while exposing the top surface of Ga₂O₃ pillars for contact formation; c) demonstration of a high BV (the major signature of charge balance) in the dynamic switching test and at high temperature, unveiling the overvoltage robustness of hetero-superjunction.

II. EPITAXY AND DEVICE DESIGNS

Fig. 1 shows the 3D schematic of our Ga₂O₃ SJ-SBD. The n-Ga₂O₃ pillars are wrapped around by p-NiO. The acceptor concentration (N_A) in NiO is designed to be larger than donor concentration (N_D) in Ga₂O₃. This makes the NiO thickness (w_p) much smaller than the Ga₂O₃ pillar width (w_n) at charge balance ($w_p N_A = w_n N_D / 2$). This small w_p and a sufficient pillar spacing ($S > 2w_p$) can ease the NiO deposition into deep trenches and avoid the early coalescence at the top of the trench [5]. In each Ga₂O₃ pillar, in addition to n-Ga₂O₃ layer, a top n'-Ga₂O₃ layer is designed to boost BV by 1) lowering the tunneling leakage current of the Schottky contact and 2) moving the peak E-field from the Schottky contact into the bulk superjunction region.

Fig. 2 shows the bi-layer Ga₂O₃ epitaxy on 2-inch (001) n⁺-Ga₂O₃ substrate by HVPE. After the growth of a n-Ga₂O₃ layer, it is polished to 10 μm, followed by the second growth of a n'-Ga₂O₃ layer, which is polished to a thickness of 0.5 μm. The electrochemical C-V tests reveal a $N_D \sim N_A$ of $\sim 1 \times 10^{16}$ cm⁻³ and 2×10^{17} cm⁻³ in the n'-Ga₂O₃ and n-Ga₂O₃ layers, respectively.

Recent work revealed that the N_A of NiO can be tailored by the O₂ partial pressure in sputtering [5]. In this work, NiO is sputtered in an Ar/O₂ (60/3 sccm) atmosphere and annealed at 275 °C in N₂. As shown in Fig. 3, from C-V characteristics of a NiO/Ga₂O₃ p-n⁺ diode fabricated on the n⁺-Ga₂O₃ substrate, N_A is extracted as 1.5×10^{18} cm⁻³ with only < 5% increase at 150 °C.

Fig. 4 shows the superjunction optimization based on the N_D and N_A determined above and a constant $S = 1.5$ μm. Here we consider the superjunction breakdown to be limited by NiO, due to its lower critical E-field than Ga₂O₃. As w_n increases, device $R_{ON,SP}$ reduces; meanwhile, the lateral E-field increases and

vertical E-field reduces, leading to a lower BV . From the vertical superjunction figure of merit ($FOM=BV/R_{ON,SP}$), an optimal w_n window of about 1.2–2 μm is identified.

Fig. 5 shows the simulated E-field and potential contours of the NiO/Ga₂O₃ SJ-SBD. The peak E-field is at the n-Ga₂O₃/NiO interface with low E-field in the top n-Ga₂O₃ or near Schottky contact. The nearly isometric equipotential contours in the drift region verify a uniform vertical E-field in the superjunction.

III. DEVICE FABRICATION

Fig. 6 shows the main fabrication steps. As NiO is difficult to etch, a novel self-align process is developed, which uses a SiO₂ mask with undercut to enable an etch-free, lithography-free NiO cap removal after the NiO sputtering. An additional Ni mask is deposited on top of SiO₂ for the deep Ga₂O₃ etch using the BCl₃ gas. The Ga₂O₃ pillar height is ~ 6.5 μm with w_n ranging from 1 to 2 μm . After the NiO cap removal, trenches are filled with photoresist (PR), followed by a O₂ planarization etch. The Ni/Au/Ti/Ag Schottky contact is finally formed on the exposed Ga₂O₃ surface. The self-align and the PR filling & planarization processes greatly simplify the device fabrication.

Fig. 7 shows SEM images of the etched Ga₂O₃ pillars, the SiO₂ mask with undercut, the NiO-wrapped Ga₂O₃ pillars after NiO cap removal, and the SJ region after anode formation. The self-align process naturally leaves a NiO ledge on the Ga₂O₃ surface, allowing the anode (Ni) to form an Ohmic contact with NiO. This favors the charge supply/extraction in NiO.

IV. DEVICE STATIC CHARACTERISTICS

Fig. 8 shows the reverse I-V characteristics of Ga₂O₃ SJ-SBDs with w_n of 1–2 μm and an identical w_p of 120 nm. BV increases with the increasing w_n , reaching ~ 2 kV at $w_n=1.8$ μm , and starts to decrease at larger w_n . This behavior manifests the critical role of charge balance. The box plot of the BV of six SJ-SBDs with $w_n=1.8$ μm reveal an average BV of ~ 2 kV with the highest BV near 2.2 kV. All BV are destructive and the leakage currents at BV are low (in the 10^{-4} – 10^{-5} A/cm² range). At 2 kV, simulation reveals the peak E-fields in Ga₂O₃ and NiO are 5 and 4.8 MV/cm, respectively; the average vertical E-fields in Ga₂O₃ and NiO are 3 and 3.1 MV/cm, respectively. All these E-fields are much higher than the counterparts in WBG superjunctions [5], manifesting one advantage of UWBG semiconductors.

Fig. 9 plots the BV as a function of the charge imbalance percentage for SJ-SBDs with various w_n and two sets of w_p . The inverted U-shape curve shows the determining impact of charge balance on BV and validates the superjunction functionality. Fig. 10 shows the reverse I-V characteristics of Ga₂O₃ SJ-SBDs with $w_n=1.8$ μm at 25, 100 and 175 $^{\circ}\text{C}$, revealing a $BV>1.8$ kV at 175 $^{\circ}\text{C}$. This high BV at 175 $^{\circ}\text{C}$ suggests the charge balance is largely preserved at high temperatures. The BV 's negative temperature coefficient implies a trap-mediated breakdown.

Figs. 11 and 12 show the forward I-V characteristics of the SJ-SBD with $w_n=1.8$ μm at 25 $^{\circ}\text{C}$ and 50–175 $^{\circ}\text{C}$, respectively. The current density is normalized to the total anode area (pillar spacing area included). The V_{ON} , on/off ratio, and differential $R_{ON,SP}$ is 1 V, 10^9 , and 0.7 m $\Omega\cdot\text{cm}^2$, respectively, at 25 $^{\circ}\text{C}$; at 175 $^{\circ}\text{C}$, they are 0.8 V, 10^8 , and 1.3 m $\Omega\cdot\text{cm}^2$, respectively.

V. SWITCHING CIRCUIT TEST

A critical concern for hetero-superjunction is the device BV (representative of superjunction functionality) under dynamic

conditions. In device turn-OFF, acceptors are ionized in NiO and holes are removed via anode. If these processes cannot keep up with the bias ramp-up or a serious carrier trapping occurs, charge balance will be impaired, resulting in a low dynamic BV .

Unclamped inductive switching (UIS) test is widely used to evaluate the dynamic BV and overvoltage robustness of a non-avalanche power device [8]. We develop an on-wafer UIS test setup, in which the UIS circuit board is connected to the probes in contact with devices (Fig. 13). In the UIS test, the inductive energy produces a capacitive voltage overshoot in the device. Fig. 14 shows the UIS waveforms of Ga₂O₃ SJ-SBDs ($w_n=1.8$ μm) under the increased inductive energy. The device survives the 2 kV UIS test and fails at a dynamic BV of 2.2 kV. This slightly higher dynamic BV than static BV is also reported in GaN HEMTs [8] and maybe due to the reduced trap ionization in short pulses (which may lead to the more precise charge balance if slight mismatch exists in DC conditions). Practically, this suggests a higher device overvoltage margin in switching.

Finally, the SJ-SBD is stressed under the repetitive UIS tests with a 1.7 kV peak voltage for hundreds of cycles (Fig. 15). No parametric shift is observed after the stress, verifying the robust superjunction functionality under the continuous switching.

VI. BENCHMARK AND SUMMARY

Fig. 16 benchmarks the differential $R_{ON,SP}$ vs. BV of our Ga₂O₃ SJ-SBDs with the 0.6–4 kV SBDs or JBS diodes based on SiC [9], GaN, and Ga₂O₃. Our Ga₂O₃ SJ-SBDs show the best $R_{ON,SP}$ vs. BV trade-off. Table I compares our vertical Ga₂O₃ SJ-SBDs with other superjunction diodes reported in WBG and UWBG materials [4, 5], [10–14]. Our Ga₂O₃ SJ-SBD shows the best combinations of low V_{ON} , high forward current, dynamic and high-temperature robustness, and high superjunction FOM.

In summary, we demonstrate the first functional vertical superjunction device in Ga₂O₃. A bi-layer epi enables the low Schottky leakage current and E-field migration into the bulk Ga₂O₃. A novel self-align process obviates the NiO etch and greatly simplifies the device fabrication. The device's $R_{ON,SP}$ vs. BV trade-off is among the best in all power SBDs. The hetero-superjunction retains high BV at high temperature and in dynamic switching. These results mark the arrival of UWBG superjunctions and show their promise for power electronics.

ACKNOWLEDGEMENT

We thank the support from NSF (ECCS-2230412 and 2036915), ONR monitored by Lynn Petersen (N00014-21-1-2183), and CPES Industry Consortium. Device fabrication was conducted as part of a user project at the Center for Nanophase Materials Sciences, which is a US DOE, Office of Science User Facility at Oak Ridge National Laboratory.

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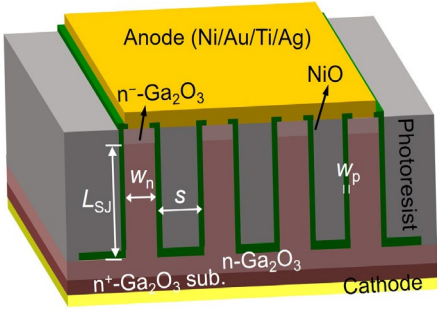


Fig. 1. Schematic of vertical Ga₂O₃ superjunction Schottky barrier diode (SJ-SBD). The Ga₂O₃ pillar width (w_n) and spacing (S), sidewall NiO thickness (w_p), and SJ length (L_{sj}) are illustrated.

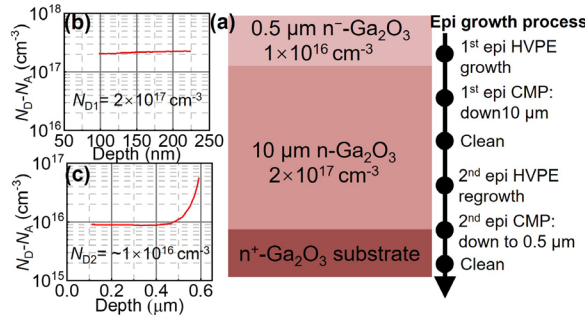


Fig. 2. (a) Schematic of the bi-layer epitaxy structure and two-step growth process. ECV data of the as-grown (b) n-Ga₂O₃ layer and (c) n-Ga₂O₃ layer. The missing N_D data close to the surface is due to the initial depletion of the Schottky tip in the ECV measurement.

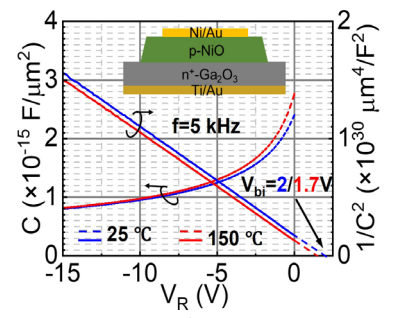


Fig. 3. C-V and $1/C^2$ -V characteristics of a vertical p-NiO/n-Ga₂O₃ diode at 25 °C and 150 °C, enabling the N_A extraction in NiO. N_D of n-Ga₂O₃ substrate is $8.3 \times 10^{18} \text{ cm}^{-3}$.

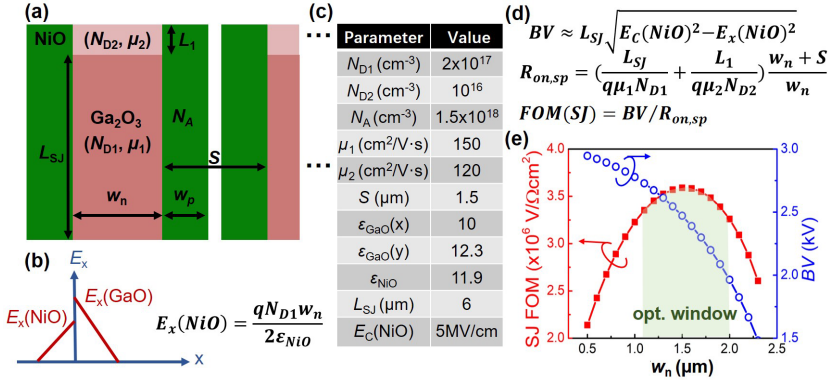


Fig. 4. w_n optimization in the hetero-superjunction. (a) Schematic of the SJ unit-cell and (b) lateral E-field (E_x) distribution. (c) Material properties in the modeling, e.g., doping, mobility, dielectric constant, and NiO's critical E-field [estimated from the bandgap; it is usually lower in practical devices (e.g., $\sim 4.8 \text{ MV/cm}$ at our device BV)]. (d) Main model equations. (e) Modeled SJ FOM and BV as a function of w_n . To maximize the SJ FOM, a w_n window of about 1.2–2 μm is derived.

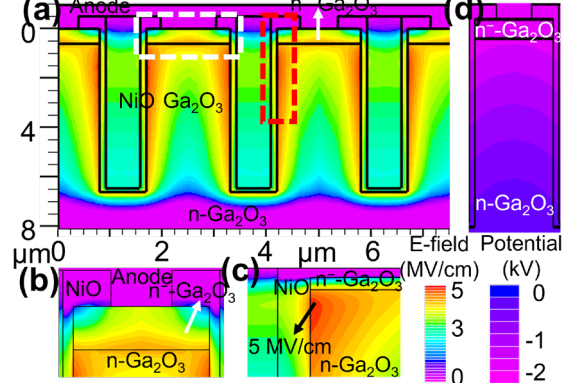


Fig. 5. Simulated E-field contours in (a) Ga₂O₃ SJ-SBD at 2 kV and zoom-in views of the (b) white- and (c) red-dashed regions. The peak E-field is located at the n-Ga₂O₃/NiO junction; low E-field is in n-Ga₂O₃ or at the Schottky contact. (d) simulated potential contours in n-Ga₂O₃, suggesting the uniform vertical E-field in the superjunction.

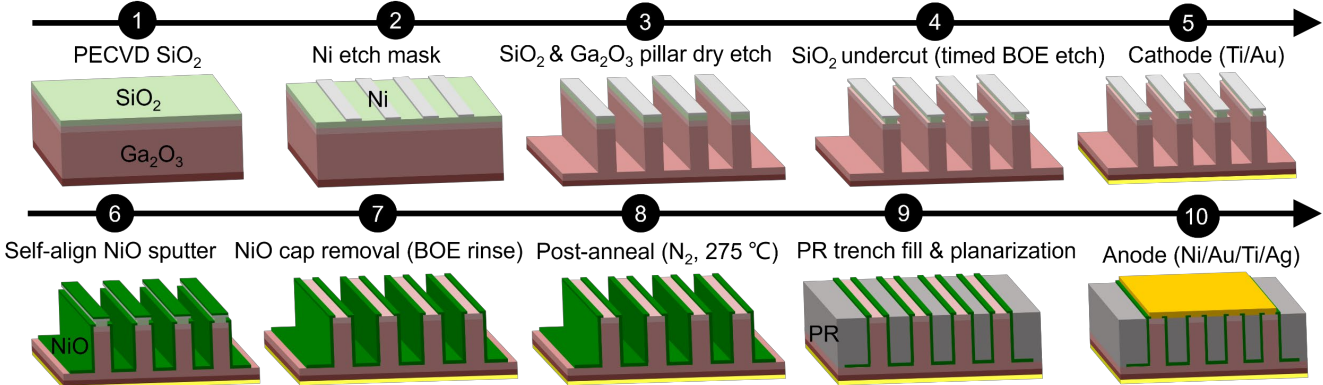


Fig. 6. Main steps in the fabrication process for Ga₂O₃ SJ-SBDs. The process highlights a self-aligned, etch-free, lithography-free NiO cap removal (step #7) using the SiO₂ mask with undercut (produced in step #4). The NiO sputter condition in step #6 is: 60/3 sccm Ar/O₂ atmosphere, 3 mTorr pressure, 100 W RF power, room temperature, and the NiO target. The PR used in step #9 is the AZ nLOF 2020. Its breakdown field is tested to be 7.1 MV/cm using a separate test structure.

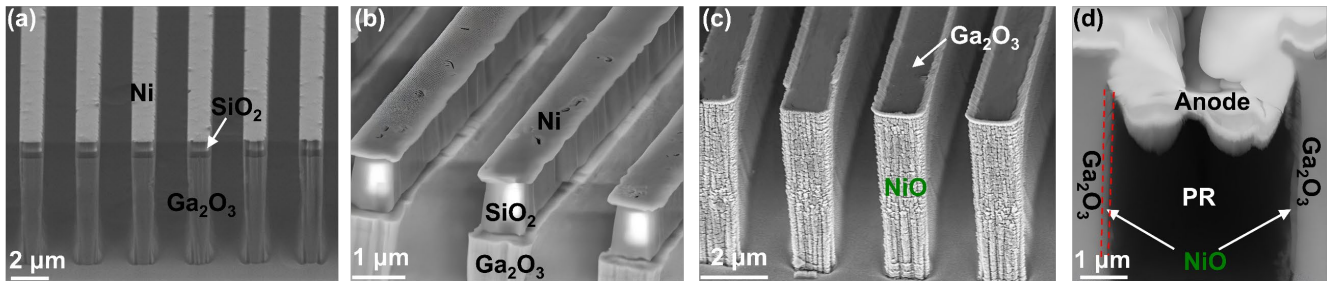


Fig. 7. SEM images of the (a) Ga₂O₃ pillars after etch (step #3), (b) Ni etch mask and SiO₂ undercut (step #4), and (c) self-aligned NiO sputter and cap removal (step #7), showing the exposed Ga₂O₃ surface. (d) Cross-sectional FIB-SEM image of a SJ unit-cell, showing the sidewall NiO, inter-pillar PR, and top anode metals.

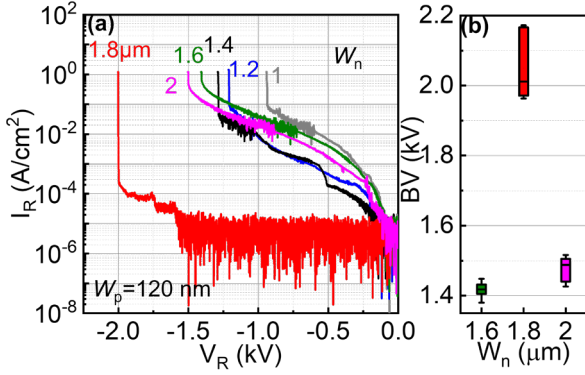


Fig. 8. (a) Reverse I-V characteristics of the Ga₂O₃ SJ-SBDs with w_n of 1-2 μm and an identical $w_p=120$ nm. (b) BV box plot of three types of devices ($w_n=1.6, 1.8$ and 2 μm) with 6 devices in each type.

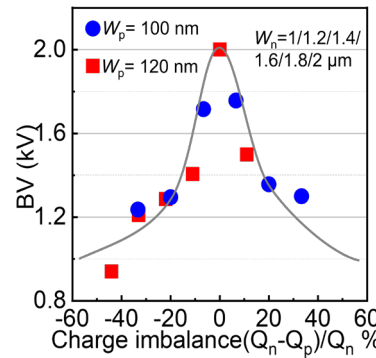


Fig. 9. The BV as a function of charge imbalance percentage for the SJ-SBDs with six w_n (1~2 μm) and two sets of w_p (100 nm and 120 nm).

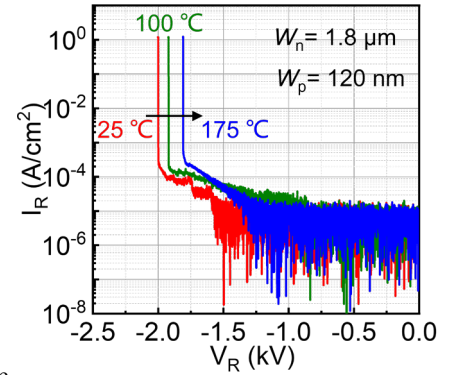


Fig. 10. Reverse I-V characteristics of the charge-balanced SJ-SBDs at 25 °C, 100 °C and 175 °C.

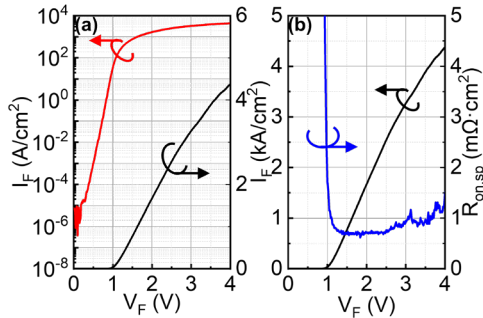


Fig. 11. (a) Forward I-V characteristics (semi-log and linear scales) and (b) extracted differential $R_{ON,SP}$ of the Ga₂O₃ SJ-SBD with w_n of 1.8 μm and w_p of 120 nm.

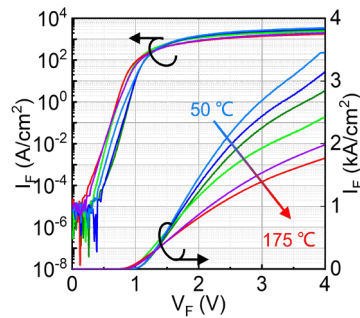


Fig. 12. Forward I-V characteristics of the charge-balanced Ga₂O₃ SJ-SBD from 50 °C to 175 °C at a step of 25 °C.

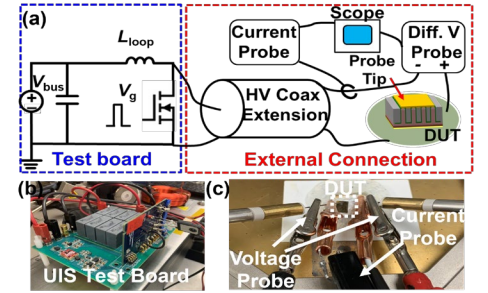


Fig. 13. (a) Schematic of the on-wafer UIS test setup. Photograph of the (b) UIS circuit board and (c) probes on the device under test (DUT). The loop inductance (L_{loop}) is 47 mH, the switch FET is a 3.3 kV SiC MOSFET (#MSC080SMA330), the Ga₂O₃ DUT is in parallel with the SiC FET, the differential voltage probe is Tektronic THDP0100, and the bus voltage (V_{BUS}) is 30 V.

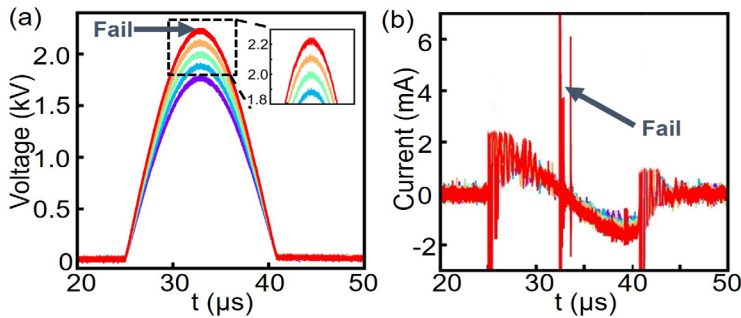


Fig. 14. The (a) voltage and (b) current waveforms of the Ga₂O₃ SJ-SBD ($w_n=1.8$ μm) in the UIS tests with increased inductive energy. The device fails at a dynamic BV of 2.2 kV. The failure current waveform confirms that the failure transient is when device voltage reaches the peak value.

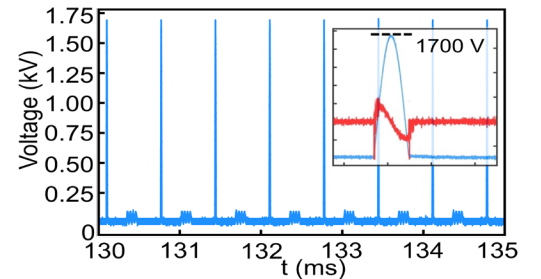


Fig. 15. Repetitive UIS waveforms with 1.7 kV peak voltage. Inset: voltage (blue) and current (red) waveforms in one cycle. The peak voltage is stable. Device shows no parametric shifts after this stress.

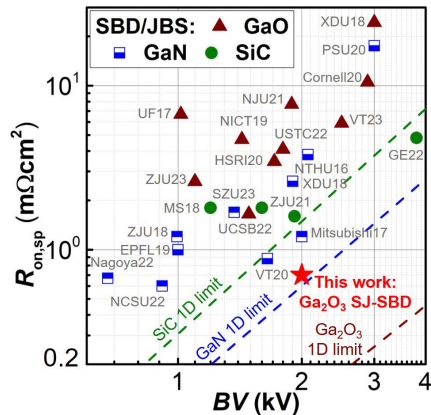


Fig. 16. Differential $R_{ON,SP}$ vs. BV of our Ga₂O₃ SJ-SBD and state-of-the-art 600-4000V Ga₂O₃, SiC and GaN SBDs or junction barrier Schottky (JBS) diodes.

TABLE I. Comparison of superjunction power diodes reported in WBG and UWBG semiconductors, including BV, differential $R_{ON,SP}$, V_{ON} , forward current density at 1.6 V, dynamic test, high-temperature data, and FOMs.

Device	Ref.	BV (V)	$R_{ON,SP}$ (mΩ·cm²)	V_{ON} (V)	I_F @ 1.6V (A/cm²)	Dyn. Test	High-T	V-SJ FOM ¹⁾ (BV/ $R_{ON,SP}$)	L-SJ FOM ²⁾ (BV ² / $R_{ON,SP}$)
Vertical Ga ₂ O ₃ SJ SBD	This work	2000	0.7	1	1000	Yes	175°C	2.86 MV/Qcm²	5.71 GW/cm²
Lateral Ga ₂ O ₃ high-k SBD ³⁾	UCSB[10]	1487	1.65	1.3	180	N/A	N/A	0.9	1.34
Vertical SiC SJ SBD	ZJU [11]	1920	1.6	1.3	150	N/A	N/A	1.2	2.3
Vertical SiC SJ/CB SBD ⁴⁾	GE [4]	3800	4.5	1.1	~100	Yes	175°C	0.84	3.2
Vertical GaN SJ PND	VT [5]	1100	0.3	3	N/A	N/A	N/A	3.67	4.03
Lateral GaN SJ SBD ⁵⁾	USheff., AIST [12]	2400	14	0.4	85	N/A	N/A	0.17	0.4
	PSU [13]	>3000	17.5	0.8	~75	Yes	N/A	>0.17	>0.52
Lateral GaN MC-SJ SBD ⁶⁾	VT [14]	1650	0.88	0.7	~1500	N/A	N/A	1.88	3.1

¹⁾Vertical SJ (V-SJ) and lateral SJ (L-SJ) are limited by $R_{ON,SP} \sim BV$ and $R_{ON,SP} \sim BV^2$, respectively; FOMs are defined accordingly; ²⁾This is also the Baliga's FOM for 1D devices; ³⁾charge balance induced by dielectric polarization; ⁴⁾both SJ and charge-balanced SBDs are reported; ⁵⁾AlGaIn/GaN SBD with balanced charge. ⁶⁾Multi-channel (MC) AlGaIn/GaN SBD with balanced charge.