# Switching figure-of-merit, optimal design, and power loss limit of (ultra-) wide bandgap power devices: a perspective

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Power semiconductor devices are utilized as solid-state switches in power electronics systems, and their overarching design target is to minimize the conduction and switching losses. However, the unipolar figure-of-merit (FOM) commonly used for power device optimization does not directly capture the switching loss. In this Perspective paper, we explore three interdependent open questions for unipolar power devices based on a variety of wide bandgap (WBG) and ultra-wide bandgap (UWBG) materials: 1) What is the appropriate switching FOM for device benchmarking and optimization? 2) What is the optimal drift layer design for total loss minimization? 3) How does the device power loss compare between WBG and UWBG materials? This paper starts from an overview of switching FOMs proposed in the literature. We then dive into the drift region optimization in 1-D vertical devices based on a hard-switching FOM. The punch-through design is found to be optimal for minimizing the hard-switching FOM, with reduced doping concentration and thickness compared to the conventional designs optimized for static FOM. Moreover, we analyze the minimal power loss density for target voltage and frequency, which provides an essential reference for developing device- and package-level thermal management. Overall, this paper underscores the importance of considering switching performance early in power device optimization and emphasizes the inevitable higher density of power loss in WBG and UWBG devices despite their superior performance. Knowledge gaps and research opportunities in the relevant field are also discussed.

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## Introduction

Power semiconductor devices, which have a market size over $40 billion, are key enablers for electric energy conversion in numerous applications such as mobile electronics, electric vehicles, data centers, renewable energy processing, and grids.[1] Power devices are used as solid-state switches, and the generic design target of power devices is to minimize their total loss under switching operations, as the device loss determines the efficiency, power density, and form factor of power electronics systems. For a power transistor, its power loss usually consists of (a) conduction loss when passing a load current, (b) switching loss in the turn-on/off transitions, and (c) driver loss incurred at the device gate or base. The conduction loss and switching loss of unipolar transistors, which switch faster than the similarly-rated bipolar devices, are usually determined by the device's on-resistance ($R_{on}$) and the device's output capacitance ($C_{OSS}$), output charge ($Q_{OSS}$), and output stored energy ($E_{OSS}$), respectively.[2]

The last decade has witnessed a performance leap in power devices by adopting wide-bandgap (WBG) materials including silicon carbide (SiC) and gallium nitride (GaN).[3–7] Since the critical electric field ($E_C$) of a semiconductor roughly scales with the square of the bandgap, SiC and GaN can have an $E_C$ value 10 times higher than that of silicon (Si).[8] For the same breakdown voltage ($V_{br}$), the limit of device's specific on-resistance ($R_{on,sp} = R_{on} \cdot A$, where $A$ is the active device area) is proportional to $E_C^{-2}$ or $E_C^{-3}$.[1] Thus, for the same $V_{br}$ and current rating (or $R_{on}$), WBG devices allow for a smaller $A$, which can further lead to lower $C_{OSS}$, $Q_{OSS}$ and $E_{OSS}$. Beyond SiC and GaN, extensive research is exploring ultra-wide-bandgap (UWBG) materials including gallium oxide ($Ga_2O_3$), aluminum nitride (AlN), diamond and boron nitride (BN), which promise an $E_C$ at least twice that of SiC and GaN. UWBG devices hence possess a theoretical $R_{on,sp} \sim BV$ trade-off limit that is superior to WBG devices.[9–12]

In power device research, it has become a routine to rely on $R_{on,sp}$ for benchmarking devices with a similar $BV$ but different current levels. Minimization of $R_{on,sp}$ also becomes a major target when optimizing the drift layer doping and thickness of power devices. However, $R_{on,sp}$ benchmarking is difficult to implement for comparison of the performance of practical industrial devices, as their datasheets do not typically disclose $R_{on,sp}$ and instead give $R_{on}$. On the other hand, the correlation between $R_{on,sp}$ and the switching-related device parameters is fundamentally insufficient. While $R_{on,sp}$ can capture the $A$ information, the $C_{OSS}$, $Q_{OSS}$ and $E_{OSS}$ are not only related to $A$ but also doping concentrations and device structures.

In circuit design, the selection of power devices rely on a group of switching figure-of-merits (FOMs) tailored for various application scenarios.[2] In addition to $R_{on}$, such FOMs often contain an additional datasheet parameter related

to capacitance, charge, or energy. The difference between the FOM used in the device/material design and the one in the device selection in circuit application has become an elephant in the room that could hinder the development of emerging power device technologies. A device optimized for $R_{on,sp}$ may not provide competitive switching FOMs and slow down the device deployment at the circuit level. To address this challenge, switching loss should be a new dimension to be added in the material and device designs, which ultimately facilitates a material-device-circuit co-optimization.

This Perspective paper starts by surveying the switching FOMs that are commonly used for device benchmarking in circuit applications, as well as those proposed in the literature that can guide the material and device designs. Subsequently, we dive into the optimization of the total conduction and switching loss of 1D vertical devices based on minimizing a hard-switching FOM. For an arbitrarily selected voltage class, the optimal doping concentration and thickness of the drift region are derived for WBG and UWBG devices, considering physical models such as incomplete ionization, avalanche breakdown, and doping-dependent mobility. The optimal drift region designs for total loss minimization are found to be differ from those for $R_{on,sp}$ minimization, underscoring the need for considering switching loss early in the material optimization. Finally, the limit of power loss density is calculated as a function of target voltage and frequency for WBG and UWBG devices. This provides pivotal information for device- and packaging-level thermal management.

**Switching Figure of Merits**

Table I summarizes the commonly-used switching FOMs of unipolar transistors and power diodes for device selection in circuit applications. These FOMs consider the trade-off between the conduction loss and the switching losses in two generic switching schemes, i.e., hard switching and soft-switching, which refers to the switching transition with and without considerable voltage-current overlap, respectively. Under ideal hard switching conditions, if circuit parasitics are minimized and the unipolar device switches sufficiently fast, the turn-off and turn-on losses should approach zero and $E_{OSS}$, repectively.[13–15] The underlying physics is illustrated in Fig. 1 for a vertical power MOSFET. Fig. 1(a) shows the schematics of drain-source voltage ($V_{DS}$), drain-source current ($I_{DS}$), and gate-source voltage ($V_{GS}$) in the hard turn-on process. Figs. 1(b)-(d) show the internal dynamics within a device unit-cell in the off-state, turn-on transient, and on-state, respectively. In the turn-off process, $E_{OSS}$ is charged by capacitive current, which ideally is a lossless process.[16] During the hard turn-on, the stored $E_{OSS}$ dissipates in the open channel as the

resistive loss, making $E_{OSS}$ the lower bound of the total hard-switching loss. In the on-state, $R_{on}$ determines the conduction loss. Accordingly, $R_{on}E_{OSS}$ is usually used as a device FOM for unipolar devices in hard-switching applications.

The device switching loss during an ideal soft switching transition is zero. However, in practical implementations of soft-switching, e.g., zero-voltage switching (ZVS), a deadtime is required at which the channels of both devices in a half-bridge are turned-off. In this deadtime, one device usually operates in the reverse conduction (i.e., third-quadrant). The third-quadrant loss of a transistor depends on the reverse-recovery charge ($Q_{rr}$) of its body diode (note the body diode could be bipolar in a unipolar transistor, e.g., power MOSFET). Thus, $R_{on}Q_{rr}$ is usually used as a device FOM for soft-switching applications. In hard-switching, $Q_{rr}$ can also induce loss in the complementary device of a half-bridge; however, this loss is usually negligibly small compared to $E_{OSS}$. Under ZVS conditions, besides deadtime loss, another factor limiting the switching frequency is the time to charge and discharge the $Q_{OSS}$. Therefore, $R_{on}Q_{OSS}$ is sometimes used as a FOM for high-frequency, soft-switching applications.

In addition to the power loop, loss is also produced in driving the gate/base of power transistors. For voltage-controlled devices, the driver loss is proportional to the gate charge ($Q_G$), making $R_{on}Q_G$ a switching FOM that measures the trade-off between conduction loss and driver loss. Such a FOM usually becomes relevant under high frequency, light load conditions when the driver loss is high but conduction and switching losses are low, as well as in soft-switching with minimal switching loss.

In power diodes, the forward I-V characteristics are non-Ohmic, so that the characteristic metric for conduction loss is forward voltage ($V_F$) which is defined as the voltage drop at a certain current (density) level. This $V_F$ captures both the turn-on voltage and differential $R_{on}$. The switching loss of diodes mainly occurs during reverse recovery, making $V_FQ_{rr}$ a loss-related FOM for diode benchmarking. On the other hand, in hard switching, the $Q_{OSS}$ discharged in diodes could produce a loss in the complementary transistor in the half bridge. As a result, $V_FQ_{OSS}$ becomes the other diode switching FOM in hard switching applications, particularly for those unipolar diodes with minimal $Q_{rr}$.

As an example of using these switching FOMs in device comparison, the $R_{on}E_{OSS}$ and $R_{on}Q_{rr}$ of various commercially-available unipolar transistors across the voltage ratings from 30 V to 3300 V are plotted in Fig. 2, based on the datasheet parameters. These devices include Si MOSFETs (5-200 V), Si superjunction MOSFETs (600-950 V), GaN high-electron mobility transistors (HEMTs) (15-650 V), and SiC MOSFETs (650-3300 V). In addition to material differences, these devices also have different device architectures (e.g., vertical and lateral) and device

physics (e.g., 1-D and multidimensional[1]). It is also important to note that the test conditions and circuit conditions used for evaluating the dynamic quantities of $R_{on}$, $E_{OSS}$ and $Q_{rr}$ differ between each surveyed device. $E_{OSS}$ and $Q_{rr}$ values are taken as given in each datasheet based upon the test conditions chosen by the manufacturer. Thus, the calculated FOMs do not necessarily represent the performance limit of the underlying device technology. The detailed information of the devices included in the plot is listed in Table S1 of Supplementary Material. It can be seen that WBG transistors show superior $R_{on}E_{OSS}$ and $R_{on}Q_{rr}$ over similarly-rated Si transistors, which align with their superiority in both hard-switching and soft-switching applications. The zero $Q_{rr}$ of GaN HEMTs make them particularly favorable to high-frequency, soft-switching applications.[17,18]

Another desirable property of some switching FOMs, such as $R_{on}E_{OSS}$ and $R_{on}Q_{OSS}$, is the weak dependence on $A$ (as $R_{on}$ downscales and $Q_{OSS}/E_{OSS}$ upscales with $A$), allowing the FOMs to be used to benchmark devices with various current levels. This current independence make their area-normalized forms, $R_{on,sp}E_{OSS,sp}$ and $R_{on,sp}Q_{OSS,sp}$ ($E_{OSS,sp}$ and $Q_{OSS,sp}$ are the specific $E_{OSS}$ and $Q_{OSS}$ normalized by the device area $A$), widely applicable to research and industry devices. Moreover, these area-insensitive FOMs can also be used to define the limit of device switching performance for a certain material, which will be explored later in this article. Conversely, the diodes' switching FOMs, $V_F Q_{rr}$ and $V_F Q_{OSS}$, are both $A$-dependent (as $V_F$ has little dependence on $A$ but both $Q_{rr}$ and $Q_{OSS}$ have strong $A$ dependence); thus, it is only meaningful to apply them to compare devices with similar current ratings.

For the purposes of device benchmarking and inter-material performance comparisons, several area-independent switching FOMs have been proposed in the literature. In 1995, Kim *et al*. deployed $R_{on,sp}C_{OSS,sp}$ for comparing the performance of low-voltage Si power MOSFETs in high-frequency applications.[19] In 2004, Huang utilized $R_{on,sp}Q_{GD,sp}$ to benchmark high-voltage power MOSFETs in hard-switching applications, where $Q_{GD,sp}$ is the specific gate-to-drain output charge.[20] In 2009, Nakajima *et al*. employed $R_{on,sp}E_{OSS,sp}$ for generic device selection in hard-switching applications.[21] In 2018, Shenai proposed a comprehensive switching FOM for power MOSFETs, which comprises $k_T E_C/R_{on,sp}$ ($k_T$ is the material's thermal conductivity) along with $Q_G$ and $T_{jmax}$ (maximum operational junction temperature).[22] The FOMs above are mainly proposed for 1-D vertical devices, which are the most widely deployed device architectures in the history of power device development. Meanwhile, there are also reports that probe the performance limit and FOMs of lateral devices[23] and multi-dimensional devices such as superjunction[24–26] and multi-channel devices.[1]

In the following two sections, we showcase the device optimization for a switching FOM and compare the switching performance limit of devices made of different materials. For this purpose, we apply $R_{on,sp}E_{OSS,sp}$, an area-independent hard-switching FOM, to derive the optimal drift region design and compare the minimum achievable switching losses between WBG and UWBG materials. As an exemplar case study, we only consider 1-D vertical devices in this work and assume that the switching FOM of the device is dominated by the drift region; the channel region and gate structure have marginal impact on the switching FOM. The revealed trade-offs can be applied to a variety of vertical power transistors like MOSFETs and JFETs with different channel form factors (e.g., planar, trench, fin[27]). Since only the drift region is considered, the results may be best applicable to high-voltage power transistors.

**Drift Layer Design for Switching FOM Optimization**

Fig. 3 shows the electric field profiles at breakdown in a generic drift region with thickness $t_d$ and doping concentration $N_d$. The peak electric field ($E_{pk}$) is typically located near the device channel/junction. The drift region design can be generally categorized as either non-punch-through (NPT) or punch-through (PT) depending on if field drops to zero at the other side of the drift region. Assuming that device breakdown is limited by impact ionization and that the field is nearly 1-D enabled by effective edge termination,[28] $V_{br}$ is determined by the ionization integral

$$1=\int_0^{W_d(V_{br})}\alpha(x)\exp\left[\int_x^{W_d(V_{br})}\left(\beta(y)-\alpha(y)\right)dy\right]dx \tag{1}$$

where $\alpha$ and $\beta$ are the electron and hole impact ionization coefficients. In the NPT design, $W_d(V_{br})$ is the depletion width within the drift layer at $V_{br}$; it is replaced by $t_d$ in the PT design. $\alpha$ and $\beta$ are strong functions of the electric field. The models used for the electric field dependence of $\alpha$ and $\beta$ will be discussed further in the next section. Note that the equivalent $E_C$ derived from (1) usually depends on $N_d$ and $t_d$ instead of being a constant value as assumed in many publications.

As a conventional static FOM, the $R_{on,sp}$ of the drift region is given by

$$R_{on,sp}=\frac{t_d}{qn\mu_n(N_d,T)} \tag{2}$$

where $\mu_n$ is the electron (or hole for p-type doped drift regions) mobility and $n$ is the free electron/hole concentration. The mobility $\mu_n$ is a function of $N_d$ and temperature $T$, and can be parametrized by various analytic models. We consider only low-field carrier mobility and neglect any geometry-dependent spreading resistance effects. The concentration $n$ depends on $N_d$, $T$ and the ionization energy $E_A$ of the dominant donor (or acceptor). In materials such as Si, 4H-SiC, GaN and $Ga_2O_3$, where the donor is shallow, it is acceptable to assume that $n$ is equal to $N_d$. However,

in some UWBG materials such as AlN, diamond and c-BN, where $E_A$ is deep, partial dopant ionization must be considered. From Eqns. (1) and (2) and accurate models of $\mu_n$, $n$, $\alpha$, and $\beta$, the $N_d$ and $t_d$ can be optimized to minimize $R_{on,sp}$. Work performed by Kimoto for the case of 4H-SiC[29] and Cooper for SiC and GaN[30] have shown that the $R_{on,sp}$ optimized drift layer is a PT design rather than a NPT design. Wang[15] further showed that, for UWBG materials, even if $E_C$ is approximated as a constant value, the PT design still leads to $R_{on,sp}$ minimization.

Next, we optimize the drift region for the hard switching FOM $R_{on,sp}E_{OSS,sp}$. This FOM is derived from the assumption that the total power loss ($P_{tot}$) of a unipolar device of area $A$ is dominated by the on-state loss and the limit of hard-switching loss, i.e., discharge of the $E_{OSS}$ stored within the drift region:

$$P_{tot}(A, N_d, t_d) = \frac{R_{on,sp} I_{RMS}^2}{A} + fAE_{OSS,sp} \tag{3}$$

where $I_{RMS}$ is the root mean square (RMS) on-state current, determined by the switching duty cycle and peak on-state current, and $f$ is the switching frequency. If $P_{tot}$ is minimized first by optimizing the device area $A$, the optimized $A$ ($A_{opt}$) and the minimized power loss ($P_{tot}$) is given by

$$A_{opt} = \frac{I_{RMS}}{\sqrt{f}} \sqrt{\frac{R_{on,sp}}{E_{OSS,sp}}} \tag{4}$$

$$P_{tot}(N_d, t_d) = 2 I_{RMS} \sqrt{f} \sqrt{R_{on,sp} E_{OSS,sp}} \tag{5}$$

This result was found by Nakajima[21] and is similar to work by Huang[20], who considered $Q_{GD}$ of a MOSFET instead of $E_{OSS}$ for the switching loss component. The first part of Eqn. (5) is application specific, depending only on $I_{RMS}$ and $f$, while the second part gives the hard-switching FOM $R_{on,sp}E_{OSS,sp}$, which depends solely on the drift layer design assuming a marginal impact of the channel region. By optimizing the $N_d$ and $t_d$ to minimize $R_{on,sp}E_{OSS,sp}$, the total loss of the device is optimized for fixed $I_{RMS}$, $f$ and $V_{br}$. If we consider a unipolar transistor in which the effect of the drift region coupling to gate oxide or channel has minimal effect on $E_{OSS,sp}$, $E_{OSS,sp}$ is given by[31,32]

$$E_{OSS,sp} = \int_0^{\alpha_{dr} V_{br}} V_{DS} C_{OSS,sp}(V_{DS}) dV_{DS} \tag{6}$$

where $\alpha_{dr}$ is a derating factor, which captures the fraction of $V_{br}$ used to block voltage in realistic switching applications. $\alpha_{dr}$ is usually 0.5~0.7 in circuit applications to ensure the long-term reliability and provide margin for overvoltage, surge-energy, and avalanche stresses commonly seen in power converters.[33,34] The voltage dependence of $C_{OSS,sp}$ at $V_{DS}$ depends upon whether the drift region is in a PT state:

$$C_{OSS,sp}(V_{DS}) = \begin{cases} \sqrt{\frac{qN_d\epsilon}{2V_{DS}}} & V_{DS} < V_{PT} \\ \frac{\epsilon}{t_d} & V_{DS} \geq V_{PT} \end{cases} \quad (7)$$

where $\epsilon$ is the permittivity of the drift region, and $V_{PT}$ is the punch-through voltage given by

$$V_{PT} = \frac{qN_d t_d^2}{2\epsilon} \quad (8)$$

By utilizing accurate models for carrier mobility, impact ionization coefficients and dopant ionization levels, Eqns. (2) and (6) can be used to numerically optimize the $N_d$ and $t_d$ to minimize $R_{on,sp}E_{OSS,sp}$ for a chosen $V_{br}$. Fig. 4 shows the numerical algorithm used to carry out this optimization. The target $V_{br}$ and $T$ are initially chosen. $N_d$ is constrained to be less than a value $N_{d,max}$ determined by the NPT design required for $V_{br}$. The algorithm begins by finding the required $N_{d,max}$ for the given $V_{br}$ based on Eqn. (1). The FOM minimization then proceeds by varying $N_d$. At each iteration, the required $t_d$ for the selected $N_d$, which should be uniquely determined by the $V_{br}$ requirement, is found by using a nonlinear root-finding algorithm. In this way, $R_{on,sp}$, $E_{OSS,sp}$ and the FOM become single variable functions of $N_d$. The $\alpha_{dr}$ is included in the calculation of $E_{OSS,sp}$ in Eqn. (6). Brent's method is used to minimize the FOM versus $N_d$, which returns the minimized FOM and optimized $t_d$ and $N_d$ once an acceptable tolerance is reached. More information on the numerical methods underlying the presented algorithm, as well as the relevant codes, are provided in Section SII of the Supplemental Material.

Fig. 5 shows the variance of $R_{on,sp}E_{OSS,sp}$ and $R_{on,sp}$, for comparison, versus $N_d$ for the design of an 1800 V drift layer in GaN. The material parameters used for GaN will be discussed in the following section. For both $R_{on,sp}E_{OSS,sp}$ and $R_{on,sp}$, the optimal $N_d$ is less than the NPT doping, demonstrating that the optimal drift layer design is PT. As the derating factor $\alpha_{dr}$ decreases from 1 to 0.5, the optimal $N_d$ for switching FOM decreases. This can be understood by considering the $E_{OSS,sp}$ calculation, as the lower bound in the voltage integration allows for tolerance of a lower $V_{PT}$. Reducing $\alpha_{dr}$ for a larger overvoltage margin is usually required for non-avalanche devices or emerging materials.[18] This will result in an switching-optimized drift layer design pushed towards the lower-$N_d$ PT solutions.

Fig. 6(a) and Fig. 6(b) show the calculated optimal FOM and drift layer design, respectively, versus $V_{br}$ for GaN. As expected, the FOM increases with $V_{br}$ and the NPT design results in a suboptimal FOM; the optimal $N_d$ and $t_d$ decrease and increase respectively as $V_{br}$ increases. Although it is possible to lower the FOM by reducing $\alpha_{dr}$, it is not economically desirable in practical applications due to the higher cost of high-voltage devices. Fig 6(c) gives the variation of the FOM optimized drift layer design as a continuous function of derating factor. It confirms that the

optimal drift layer should be an increasingly PT design if the device is designed to operate at realistic derating factors between 0.5 and 0.8, which can give guidance for material growth optimized for switching applications.

**WBG and UWBG Switching Performance Limits**

While numerous studies have examined the benefits of WBG and UWBG materials in reducing $R_{on,sp}$, no work exists to quantitatively compare the potential switching performance benefits of these materials. To this end, using the algorithm described in the previous section, we calculate the optimal drift layer design for the hard-switching FOM minimization for Si, 4H-SiC, GaN, β-$Ga_2O_3$, diamond, AlN and c-BN. A constant derating factor of 0.5 is assumed in this section, which is a realistic value for circuit applications.

Table II shows the material parameters and models used for the calculations, with the detailed discussions included in Section SIII of the Supplementary Material. For impact ionization coefficients, the models used are preferentially taken from work in which the coefficients are determined experimentally; such work is available for Si, 4H-SiC, GaN and β-$Ga_2O_3$.[35–38] For other UWBG materials, impact ionization fits found via Monte Carlo simulation are used;[39–42] for β-$Ga_2O_3$, theoretical calculations of the x-directed impact ionization coefficients are also used, for comparison with the experimentally determined values. The calculated NPT critical electric fields as a function of $N_d$ for WBG and UWBG materials using the impact ionization coefficients listed in Table II are shown in Fig. S3 of the Supplementary Material. Carrier mobility is modeled using doping and temperature dependent analytical fits.[35,43–47] The effects of carrier velocity saturation are not considered. We utilize doping and temperature-dependent mobility models which fit to the best possible mobility attainable by each material, so that the results of our calculations are unaffected by variations in material quality. For calculations of partial ionization, the donor or acceptor with the shallowest available level for each material is chosen[48–53]; consideration of a potential deep donor level (Si DX center) is made for AlN,[54] which will be discussed further below.

Fig. 7(a) shows the calculated material limits for the hard-switching FOM for $V_{br}$ between 200 V and 20 kV. The optimized $N_d$ and $t_d$ necessary to minimize the FOM are presented in Fig. 7(b). For comparison, the optimized $R_{on,sp}$ and $R_{on,sp}$-targeted drift layer design is shown for the same $V_{br}$ range in Fig. 7(c) and Fig. 7(d). Note that the Si lines in these figures are hypothetical and just for reference, as 1-D Si devices in this voltage range are bipolar instead of unipolar. As expected, the optimized switching FOM limits for 4H-SiC and GaN are lower than Si, which align with the comparison of commercial devices shown in Fig. 2. The results for β-$Ga_2O_3$ depend upon which set of impact

ionization coefficients are used. Based upon the experimental values reported by Zhou,[38] β-$Ga_2O_3$ fails to outperform 4H-SiC and GaN for the switching FOM and $R_{on,sp}$. However, using the theoretically predicted *x*-directed impact ionization coefficients (which result in highest breakdown voltage among different crystal orientations), $R_{on,sp}$ for β-$Ga_2O_3$ is reduced by up to 6 times below GaN. Interestingly, even when using these theoretical coefficients, β-$Ga_2O_3$ gives little improvement over GaN in switching FOM; GaN even outperforms β-$Ga_2O_3$ at $V_{br}$ greater than 10 kV. This result is due to the lower electron mobility in β-$Ga_2O_3$ and the overall higher $E_{OSS,sp}$ resulting from the high $N_d$ in β-$Ga_2O_3$ for $V_{br}$ greater than 10 kV.

For other UWBG semiconductors, the performance for both metrics depends heavily upon the dopant ionization energy. For AlN, a major question is whether the dominant donor, Si, is shallow. While the hydrogenic model for n-doping with Si in AlN predicts an ionization energy of 70 meV,[51] Si is predicted to become a DX level in $Al_xGa_{1-x}N$ for mole fraction x greater than 0.7, shifting the effective ionization energy to 210 meV.[54] However, recent work by Breckenridge has shown that implanted Si in AlN results in donor activation with a near hydrogenic ionization energy of 74 meV.[51] Similarly, p-type doping of AlN during growth with Be achieved an ionization energy of 37 meV.[55] These results suggest that it may be possible to achieve shallow-level doping in AlN drift regions; for this reason, we calculate the optimized $R_{on,sp}$ and switching FOM of an n-type AlN drift region for both the hydrogenic energy and the Si DX-state ionization energy. If a shallow donor is assumed, AlN achieves a reduction in $R_{on,sp}$ by an order of magnitude and in the switching FOM of over 4 times beneath that of GaN. If instead a Si DX state is assumed, then the partial ionization results in a degraded $R_{on,sp}$ and inferior switching FOM over GaN for $V_{br}$ lower than 8 kV. At 20 kV, conversely, the DX-AlN can enable a 4x and 2x reduction in $R_{on,sp}$ and switching FOM, respectively, over GaN.

Diamond has much deeper hydrogenic donor and acceptor levels than AlN, with the shallowest dopant being B (382 meV) in p-type doped diamond.[52] As a result, at 300 K, diamond is outperformed by 4H-SiC for both metrics for all $V_{br}$ up to 20 kV. Due to the positive temperature coefficient of dopant ionization and impact ionization, diamond can improve device performance at high temperatures. The switching FOM and $R_{on,sp}$ performance of diamond at 600 K is still inferior to the 300 K 4H-SiC limit but could outperform 4H-SiC at 600 K. These results are similar to prior $R_{on,sp}$ analysis for diamond devices,[56] with the added finding that the same trend holds true for switching performance.

For the final UWBG material, we examine the potential $R_{on,sp}$ and switching FOM of c-BN. While major challenges remain in the large area growth of doped c-BN, recent theoretical work by Sanders on carrier transport in c-BN provides a doping-parametrized estimate of electron mobility.[47] Along with theoretical estimates of impact ionization

coefficients, optimal switching FOM of c-BN devices can be calculated. DFT simulations of the Si dopant in c-BN predict a deep ionization energy of 211 meV.[53] However, due to the low impact ionization coefficients, c-BN outperforms both GaN and DX-AlN in $R_{on,sp}$ and switching FOM over all $V_{br}$ ranges studied; for $V_{br}$ greater than 10 kV, c-BN outperforms the shallower donor AlN.

Fig. 8 compares the optimized switching FOM and the $R_{on,sp}$- and switching-optimized drift region designs for each material at two technologically important $V_{br}$ ratings of 3.3 kV and 10 kV. In general, drift region design using UWBG materials enable higher $N_d$ and lower $t_d$ for high voltage ratings. WBG materials are found to be competitive with UWBG materials for switching performance at 3.3 kV, with only AlN assuming a shallow donor outperforming GaN. Notwithstanding diamond, as $V_{br}$ increases to 10 kV, UWBG materials become more competitive for total loss reduction, with the switching FOM of shallow-donor AlN outperforming GaN by 2.5 times and c-BN outperforming GaN by 3.5 times. At the same $I_{RMS}$ and $f$, this implies a reduction in the total power loss in the device using c-BN over GaN for a 10 kV device of 47 %.

For the purpose of informing drift region design to minimize total power loss, it is instructive to look further into the differences between the designs for optimizing $R_{on,sp}$ and hard-switching FOM. Fig. 9(a) shows the ratio of $N_d$ and $t_d$ between two designs. As $V_{br}$ increases, the $N_d$ of the FOM-optimized drift layer design ($N_{d,FOM}$) converges to a ratio of 0.9 of the $N_d$ of the $R_{on,sp}$ optimized design ($N_{d,Ron,sp}$), while the $t_d$ ratio between two designs (i.e., $t_{d,FOM}$/ $t_{d,Ron,sp}$) converges to 0.95. For designs with $V_{br}$ greater than 10 kV, the reduction in $t_{d,FOM}$ over $t_{d,Ron,sp}$ may reach several microns, which is significant for material growth. Fig. 9(b) compares the $N_d$ and $t_d$ in the switching FOM-optimized design and the conventional NPT design ($N_{d,NPT}$ and $t_{d,NPT}$). At high breakdown voltage, the ratio of $N_d$ of the FOM-optimized design to $N_{d,NPT}$ for each material converges to a value of 0.83, while the ratio $t_{d,FOM}/t_{d,NPT}$ ranges between 0.7 and 0.75.

In contrast, the values of $N_{d,FOM}$ for UWBG materials at low breakdown voltages below 1 kV is reduced to between 0.45 and 0.6 of the NPT drift region doping; this reduction is especially pronounced for UWBG materials with deep dopants, such as c-BN, diamond at 300 K, and AlN assuming Si as a DX center. The effective "push" of the drift layer towards PT designs at low $V_{br}$, represented by the decrease of the $N_{d,FOM}$/ $N_{d,NPT}$ ratio, can be explained by considering the variation of the FOM optimized magnitudes of $R_{on,sp}$ and $E_{OSS,sp}$ as a function of $V_{br}$. At low $V_{br}$ targets, $N_d$ is relatively high, and $R_{on,sp}$ can be much smaller than $E_{OSS,sp}$. As $E_{OSS,sp}$ dominates the switching FOM and can be effectively lowered by reducing $N_d$, the optimal design becomes more PT. In comparison, when the targeted $V_{br}$ is

high, $N_d$ is low, and the $R_{on,sp}$ component dominates over $E_{OSS,sp}$. As a result, the FOM-optimized design is closer to the $R_{on,sp}$-optimized drift layer design, as shown in Fig. 9(a).

For materials with deep dopant ionization energies, the ionization ratio increases with the reduced $N_d$. As $R_{on,sp}$ and $E_{OSS,sp}$ is dependent on the ionized free carrier and the $N_d$, respectively, lowering the $N_d$ to a certain degree can benefit both parameters. Hence, the switching FOM-optimized designs for these materials move towards more PT as compared to those for materials with shallow dopants, as can be seen from the lower $N_{d,FOM}$/ $N_{d,NPT}$ ratio in Fig. 9(b). A more detailed discussion using several materials as examples is included in Section SIV of the Supplementary Material.

**WBG and UWBG Power Loss Limits**

While the calculations above demonstrate how the use of WBG and UWBG materials can reduce total power loss, the reduction in power loss comes with decreasing chip size to minimize the total energy $E_{OSS}$. Fig. 10(a) shows the $A_{opt}$ calculated by Eqn. (4) utilizing the $N_d$ and $t_d$ in the switching-optimized drift region for an arbitrarily-selected $I_{RMS}$ of 10 A and $f$ of 10 kHz. This reduction in chip size for WBG and UWBG materials implies an increase in total loss power density, the heat produced by which has to be effectively dissipated to maintain the device junction temperature below a certain limit (e.g., 175 °C) for long-term reliability operations.[57] The total power loss density is a critical parameter for guiding the design of device- and packaging-level thermal management, but it has not been quantified in the literature for WBG and UWBG materials.

Based on $A_{opt}$ and the minimized $P_{tot}$ in Eqns. (4) and (5), the minimized power loss density ($P_{tot,sp}$) in hard switching is given by

$$P_{tot,sp}=2E_{OSS,sp}f \tag{9}$$

For the switching-optimized drift regions, Fig. 10(b) shows the power loss density limit against $V_{br}$ between 200 V and 20 kV, normalized to switching frequency. This figure allows one to calculate the minimal power loss density of a device technology for an arbitrary frequency, and the corresponding power loss limit can be further calculated using the $A_{opt}$ from Eqn. (4). As shown in Fig. 10(b), due to the reduction in die area, the power loss density of UWBG materials increases significantly above WBG materials and Si, even as the total power loss is reduced. If we assume a switching frequency of 10 kHz, the power loss density of an optimized 10 kV β-$Ga_2O_3$ drift region is 92 W/cm$^2$, in

comparison with 34.7 W/cm$^2$ for SiC and 38.7 W/cm$^2$ for GaN. Note such power loss density is an intrinsic limit from electrical power loss and independent of the thermal properties of materials such as $k_T$.

To further illustrate the implications of this power loss limit, we derive the maximum specific junction-to-ambient thermal resistance ($R_{ja,sp}$) required for UWBG and WBG devices assuming a maximum operational junction temperature of 175 °C and ambient temperature of 25 °C. The upper limit of $R_{ja,sp}$ is given by

$$R_{ja,sp} \leq (175\ ^\circ\text{C} - 25\ ^\circ\text{C})/P_{tot,sp} \quad (10)$$

Figs. 10(c) and (d) show the calculated $R_{ja,sp}$ of UWBG and WBG devices as a function of $V_{br}$ at two exemplar frequencies 10 kHz and 500 kHz. At 500 kHz, for example, the maximum $R_{ja,sp}$ of 5 kV $Ga_2O_3$ devices is 3.5 times lower than that of similarly-rated SiC devices, suggesting a higher requirement on thermal management. Considering the low $k_T$ of $Ga_2O_3$, effective heat extraction to manage the high power loss density may be difficult merely relying on device-level thermal management such as substrate thinning and layout optimization. Work by multiple groups have showed the need for junction-side- and double-side-cooling packaging for thermal management of $Ga_2O_3$ devices.[58–60] A recent comprehensive review on thermal management and packaging of WBG and UWBG power devices is provided by Qin *et al*.[57]

If the thermal management is limited and cannot handle the intrinsic device power loss density shown in Fig. 10(b), device area $A$ has to be enlarged to boost the heat extraction at the price of higher total loss and slower switching speed in the device. Wang *et al* discussed the $A$ optimization in this scenario by considering the limited capability of packaging.[15] Note that, in practical device designs, it is possible to increase the chip size for heat extraction by enlarging the non-active device area such as metal pad and edge termination, which could minimize the impact on $C_{OSS}$ and $E_{OSS}$. This approach would still increase the device cost per die and may only apply to low-cost material platforms such as GaN-on-Si and GaN-on-sapphire.[61,62]

Finally, we emphasize that the calculated values of the optimal hard-switching FOM limits and associated drift layer designs for the WBG and UWBG materials surveyed in this work are highly dependent on the assumed models for impact ionization coefficients and carrier mobility as a function of field and doping, respectively. Substantial experimental characterization of impact ionization coefficients and bulk carrier mobility in SiC and GaN allows for a more confident prediction of device performance. For UWBG semiconductors such as AlN and c-BN, for which the ability to grow high quality single-crystal epilayers is still in early stages, experimental measurement of impact ionization coefficients is currently non-existent. Estimates of the impact ionization coefficients extracted from Monte

Carlo simulation are thus exclusively used in this work for calculations involving AlN, c-BN and diamond. While the most recent Monte Carlo simulations of impact ionization for these materials utilize full-band calculations, uncertainty remains in the calculation of the electron-phonon interactions at high energy[63]. Additionally, effects such as the interaction of anisotropy of the impact ionization coefficients in highly asymmetric materials such as β-$Ga_2O_3$ with edge field enhancement in real devices may result in a lower critical field than would be expected from theoretical calculations. Any increase in the impact ionization coefficients for the studied UWBG materials over the theoretically estimated values will result in an inferior switching FOM limit due to higher switching losses, accompanied by a larger die size and lower power loss density limit. This can be understood by comparing the results obtained with the experimental and theoretical impact ionization coefficients of β-$Ga_2O_3$ in Figs. 7-10. While our results predict superior hard-switching performance for the UWBG materials c-BN and AlN, especially for high $V_{br}$ designs, experimental demonstration of avalanche capability and measurement of the impact ionization coefficients will be needed before the true limit of the hard-switching performance of these materials can be evaluated.

**Conclusions and Outlook**

This Perspective article identifies the different FOMs used in device design and device applications to be an elephant in the room that can slow the development of emerging power semiconductor technologies. Subsequently, we survey the switching FOMs used for power device benchmarking in practical circuit applications and revisit the drift region design with a target to improve the switching FOM instead of the conventional static FOM $R_{on,sp}$. In addition, we derive the power loss density limit of WBG and UWBG devices for hard-switching applications, which allows one to calculate the minimal power loss of a device designed for arbitrary voltage and current ratings and operation frequency. This information can provide guidance for designing the device-level and packaging-level thermal management, which is particularly valuable for developing power modules. The key takeaways for material growers, device designers, and power electronics engineers include:

(1) Switching FOMs are essential for power device evaluation towards circuit applications; $R_{on,sp}E_{OSS,sp}$ or $R_{on}E_{OSS}$ could be area-insensitive device FOMs for hard-switching applications, and can be applied to both research grade devices and industrial devices for which no area information is available.

(2) The drift region design for switching FOM optimization differs from that for $R_{on,sp}$ optimization, though both optimized designs are PT instead of NPT in 1-D vertical devices. The switching-optimized design presents lower $N_d$ and $t_d$ and they also depend on the $V_{br}$ derating factor (or overvoltage margin).

(3) The availability of shallow dopants is essential to enable UWBG devices to achieve a lower limit of total loss in hard switching applications than WBG counterparts, and such superior limit primarily exist in high-voltage devices with a $V_{br}$ of at least multi-kilovolts.

(4) The density of power loss in hard-switching applications is inevitably higher in WBG and UWBG devices, which upscales with $f$ and $V_{br}$ for each device technology. Device- and packaging-level thermal management is critical to fulfill the full potential of the superior electrical performance of WBG/UWBG devices.

While this work explores the drift design of 1-D vertical devices for optimizing a hard-switching FOM, it could be merely a starting point to investigate the design of more complicated power devices targeted for a more diverse variety of switching applications. Some immediate research opportunities are listed as follows.

1) It is well known that multidimensional device architectures such as superjunction, multi-channel, and multi-gate can break the 1-D $R_{on,sp} \sim V_{br}$ tradeoff.[1] However, only a recent work by Kang and Udrea looked into the switching FOMs of multidimensional devices,[26] and there still lacks reporting on optimizing the geometry and doping of these devices based on switching FOMs. For some emerging devices like multi-channel lateral devices, even the $C_{OSS}$, $Q_{OSS}$ and $E_{OSS}$ models are lacking. The recent demonstrations of heterogenous multidimensional devices that comprise multiple materials[64–67] can introduce more variables and expand the device design space, making their switching-based optimization even more challenging.

2) Lateral power devices such as GaN HEMTs have reached commercial maturity, but only very few works have looked into their static and switching FOMs,[23,68–70] partly due to the significantly non-linear electric field in lateral devices. For UWBG materials, lateral devices are also under extensive research, e.g., the two-dimensional electron gas channels in AlGaO/GaO and AlGaN/AlN, as well as the two-dimensional hole gas channels in hydrogen-terminated diamond and AlN-based heterostructures.[71] The $C_{OSS}$, $Q_{OSS}$ and $E_{OSS}$ models as well as switching FOMs of these devices are largely unexplored.

3) While this work, and most prior reports, assume a constant doping concentration in the drift region, it may not be globally optimal for either static FOM or switching FOMs. Back in 1982, Xing-Bi Chen and Chenming Hu illustrated that a gradual doping profile could lead to lower $R_{on,sp}$.[72] Recently, Ohta *et al* utilized a varying-

doping drift region to demonstrate high-voltage GaN diodes over 4 kV.[73] The design of doping profiles to optimize various device switching FOMs could be a valuable research direction to explore in both 1-D and multidimensional devices based on either lateral or vertical architecture. Broadly speaking, many gaps remain in considering the circuit-operation early in the material design to engage a material-device-circuit co-optimization for power semiconductors and power electronics.

## Supplementary Material

The Supplementary Material contains the extended discussions on the commercial device comparison, the algorithms and material models in the analysis, and the difference between the switching-optimal devices and conventional devices. The link to the code of the optimization algorithm is also provided.

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## Author Contributions

**Matthew Porter**: Conceptualization (equal); Investigation (lead); Writing – original draft (lead). **Xin Yang**: Data curation (supporting), Writing – review & editing (supporting). **Hehe Gong**: Investigation (supporting); Writing – review & editing (supporting). **Bixuan Wang**: Data curation (supporting), Writing – review & editing (supporting). **Zineng Yang**: Investigation (supporting); Writing – review & editing (supporting). **Yuhao Zhang**: Conceptualization (equal); Supervision (lead); Investigation (supporting); Writing – review & editing (lead).

## Data Availability Statements

The data that supports the findings of this study are available within the article.

## Conflicts of Interest

The authors have no conflicts to disclose.

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TABLE I. SWITCHING FOM FOR POWER DEVICE BENCHMARKING.

| Device | Unipolar power transistors | | | | Power diodes | |
|---|---|---|---|---|---|---|
| Switching FOM | $R_{on}{\cdot}E_{OSS}$ | $R_{on}{\cdot}Q_{rr}$ | $R_{on}{\cdot}Q_{OSS}$ | $R_{on}{\cdot}Q_G$ | $V_F{\cdot}Q_{rr}$ | $V_F{\cdot}Q_{OSS}$ |
| Device metrics in circuit | Conduction loss, hard switching loss | Conduction loss, third-quadrant loss | Conduction loss, minimum dead time | Conduction loss, driver loss | Conduction loss, reverse recovery loss | Conduction loss, loss incurred in complementary transistor |
| Target application | Hard switching | Soft and hard switching | High-frequency soft switching | High-frequency or light load | Hard and soft switching | Hard switching in half bridge |

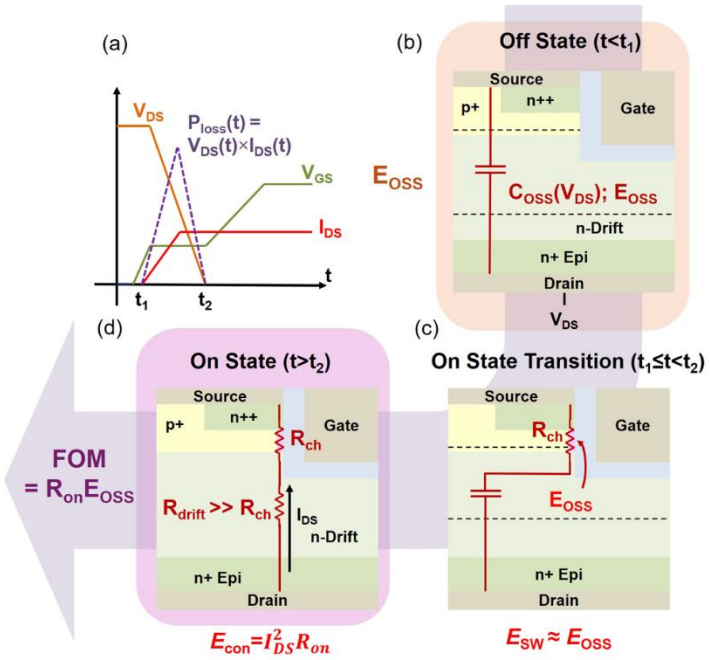


Fig. 1. (a) Schematic of $V_{DS}$, $I_{DS}$, $V_{GS}$ waveforms and power loss in the hard-switching turn-on transition. Main dynamics inside a power MOSFET during different states in a switching cycle: (b) the device stores energy electrostatically within the drift region in the turn-off transition and off-state; (c) the stored energy is dissipated through the open device channel during the turn-on transition; (d) conduction loss in the on-state is mainly determined by the drift region resistance. The major parameters for device conduction and switching losses determine the hard-switching FOM.

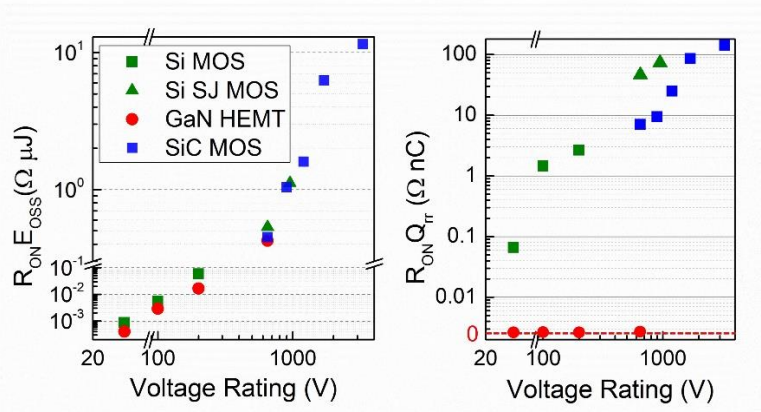


Fig. 2. The switching FOMs, $R_{ON}E_{OSS}$ and $R_{ON}Q_{rr}$, of representative unipolar power transistors calculated using their datasheet parameters. Devices include 30-200 V Si MOSFETs, 600-950 V Si superjunction (SJ) MOSFETs, 30-650 V GaN HEMTs, and 650-3300 V SiC MOSFETs. The detailed information of the benchmarked devices is in Supplementary Material.

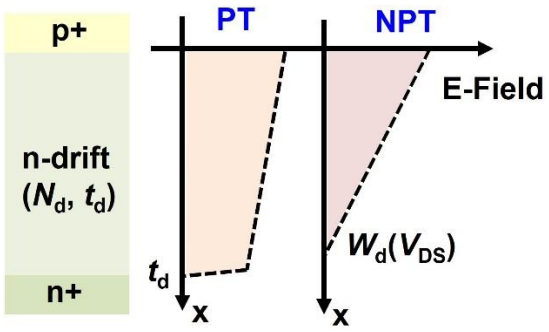


Fig. 3. Schematic of electric field (E-field) distribution in a drift region based on the punch-through (PT) and non-punch-through (NPT) designs.

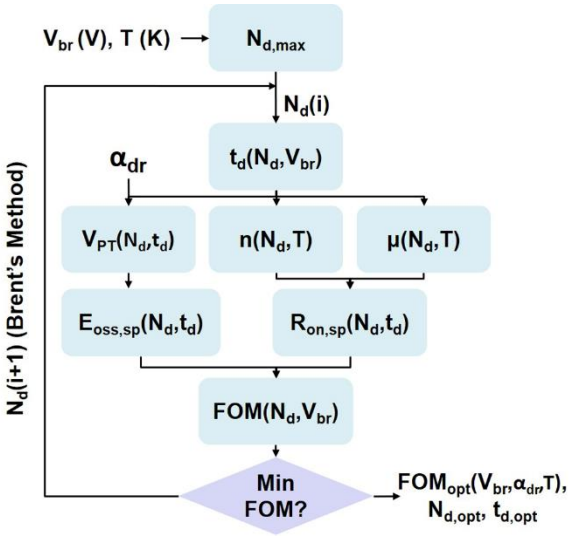


Fig. 4. Algorithm flowchart for drift layer optimization via switching FOM minimization.

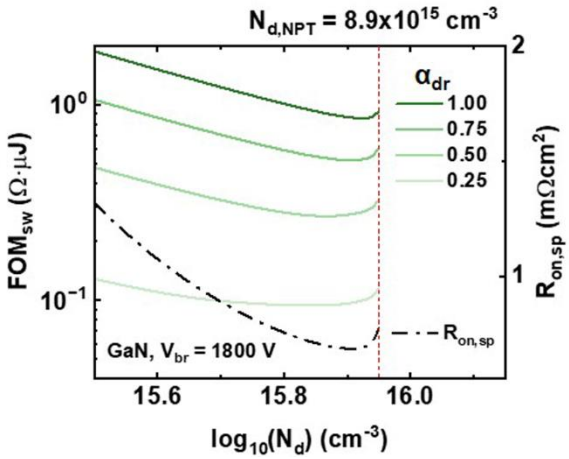


Fig. 5. Variation of switching FOM as a function of drift layer doping $N_d$ and derating factor $\alpha_{dr}$ for an 1800 V GaN drift region, up to $N_{d,NPT}$. $R_{on,sp}$ as a function of $N_d$ is presented for comparison, and is referenced to the right scale of the graph.

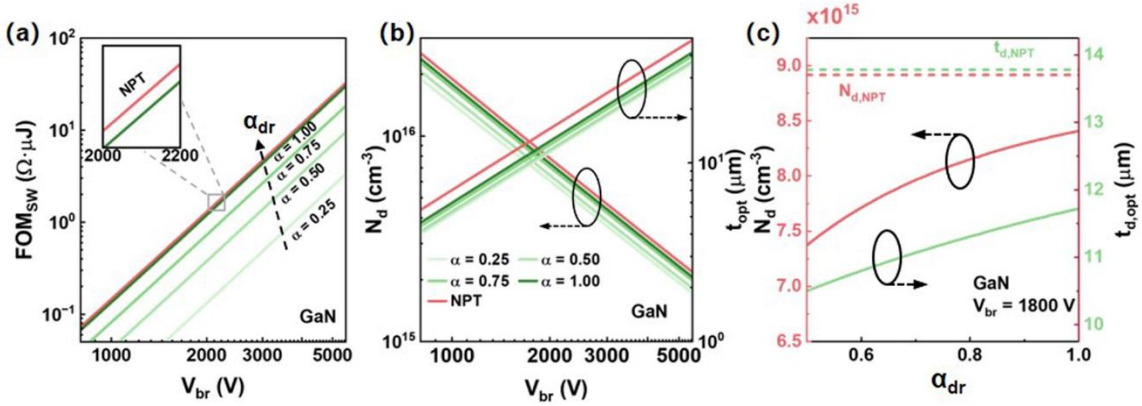


Fig. 6. Optimized GaN drift region FOM and design versus breakdown voltage, parametrized by derating factor. The variation of the optimal switching FOM versus breakdown voltage is shown in (a), and the optimized drift region design versus breakdown voltage is shown in (b). The variation of the drift region design as a function of derating factor for a breakdown voltage of 1800 V is shown in (c).

TABLE II. MATERIAL PARAMETERS AND MODELS OF SI, WBG AND UWBG SEMICONDUCTORS USED FOR THE OPTIMIZATIONS OF $R_{ON,SP}$ AND SWITCHING FOM.

| Material | Impact Ionization Model | e- Impact Ionization Parameters | h+ Impact Ionization Parameters | Mobility Model | Mobility Model Parameters | Donor/Acceptor Ionization Energy[g] |
|---|---|---|---|---|---|---|
| Si | Thornber[35,a] | $E_i$ = 2.51, $\lambda$ = 67.5×10$^{-8}$, $E_r$ = 0.106, $E_{th}$ = 0.0494 | $E_i$ = 3.06, $\lambda$ = 25.1×10$^{-8}$, $E_r$ = 0.021, $E_{th}$ = 0.012 | Caughey-Thomas[d] | $\mu_{min}$ = 55.24, $\mu_{max}$ = 1429.23 $N_{ref}$ = 1.07×10$^{17}$, $\gamma$ = 0.73 $\alpha$ = -2.3, $\beta$ = 3.8 | $P_{Si}$, $E_C - E_D$ = 45 meV |
| | $\alpha_{n/p}(E) = \frac{q\xi}{E_i}\exp\left(-\frac{1.5E_g}{q\xi\lambda + \left(\frac{q\xi\lambda}{E_r}\right)^2 + E_{th}}\right)$ | | | $\mu_n = \mu_{min} + \frac{\mu_{max}\left(\frac{T}{300}\right)^{\alpha} - \mu_{min}}{\left(1 + \left(\frac{T}{300}\right)^{\beta}\left(\frac{N_d}{N_{ref}}\right)^{\gamma}\right)}$ | | |
| 4H-SiC | Okuto-Crowell[36,b] | $a_n$ = 1.43×10$^5$, $b_n$ = 4.93×10$^6$ $\gamma$ = 2.37 | $a_p$ = 3.12×10$^6$, $b_p$ = 1.18×10$^7$, $\gamma$ = 1.02 | Caughey-Thomas[43] | $\mu_{min}$ = 27.87, $\mu_{max}$ = 950.0 $N_{ref}$ = 1.94×10$^{17}$, $\gamma$ = 1 $\alpha$ = -1.8, $\beta$ = 0.61 | $N_{Si}$, $E_C - E_D$ = 55 meV[48] |
| | $\alpha_{n/p}(E) = a_{n/p}\exp\left(-\left(\frac{b_{n/p}}{E}\right)^{\gamma}\right)$ | | | | | |
| GaN | Chynoweth[37,c] | $a_n$ = 2.77×10$^8$, $b_n$ = 3.2×10$^7$ | $a_p$ = 8.53×10$^6$, $b_p$ = 1.48×10$^7$ | Caughey-Thomas[44] | $\mu_{min}$ = 295.0, $\mu_{max}$ = 1250.0 $N_{ref}$ = 2×10$^{17}$, $\gamma$ = 0.66 $\alpha$ = -3.84, $\beta$ = 1.99 | $Si_{Ga}$, $E_C - E_D$ = 17 meV[49] |
| | $\alpha_{n/p}(E) = a_{n/p}\,exp\left(-\frac{b_{n/p}}{E}\right)$ | | | | | |
| $\beta$-$Ga_2O_3$ | Chynoweth (x)[39] | $a_n$ = 7.9×10$^5$, $b_n$ = 2.92×10$^7$ | $a_p$ = 7.9×10$^5$, $b_p$ = 2.92×10$^7$ | Ma, et al.[45,e] | $a$ = 56.0, $b$ = 508.0 $T_c$ = 278.0, $d$ = 0.68, $N_{ref}$ = 2.8×10$^{16}$ | Si, $E_C - E_D$ = 30 meV[50] |
| | Chynoweth (Measured)[38] | $a_n$ = 2.16×10$^6$, $b_n$ = 1.77×10$^7$ | $a_p$ = 5.75×10$^6$, $b_p$ = 1.77×10$^7$ | $\mu_n = \frac{a\left(exp\left(\frac{b}{T}\right) - 1\right)}{\left(1 + \left(\frac{N_d}{N_{ref}(T - T_c)^d}\right)\right)}$ | | |
| AlN | Chynoweth[40] | $a_n$ = 8.99×10$^6$, $b_n$ = 3.77×10$^7$Y | $a_p$ = 0, $b_p$ = 0 | Caughey-Thomas[44] | $\mu_{min}$ = 297.8, $\mu_{max}$ = 683.8 $N_{ref}$ = 10$^{17}$, $\gamma$ = 1.16 $\alpha$ = -3.43, $\beta$ = 4.38 | Si (Hydrogenic), $E_C - E_D$ = 70 meV[51] |
| | | | | | | Si (DX) , $E_C - E_D$ = 211 meV[54] |
| Diamond | Chynoweth[41] | $a_n$ = 3.7×10$^6$, $b_n$ = 5.8×10$^7$ | $a_p$ = 4.2×10$^6$, $b_p$ = 2.1×10$^7$ | Modified Caughey-Thomas[46,f] | $\mu_{min}$ = 0, $\mu_{max}$ = 2016.0 $N_{ref}$ = 3.25×10$^{17}$, $\gamma$ = 0.73 $\kappa$= 0.617, $\beta_1$ = 3.11, $N_\beta$ = 4.1×10$^{18}$ | B, $E_A - E_V$ = 382 meV[52] |
| | | | | $\mu_{n,300} = \mu_{min} + \frac{\mu_{max} - \mu_{min}}{\left(1 + \left(\frac{N_d}{N_{ref}}\right)^{\gamma}\right)}$ | | |
| | | | | $\mu_n = \mu_{n,300}(N_d)\left(\frac{T}{300}\right)^{\beta}$ | | |
| | | | | $\beta = -\frac{\beta_1}{\left(1 + \left(\frac{N_d}{N_\beta}\right)^{\kappa}\right)}$ | | |
| c-BN | Chynoweth[42] | $a_n$ = 1.2×10$^6$, $b_n$ = 5.184×10$^7$ | $a_p$ = 3.21×10$^6$, $b_p$ = 3.31×10$^7$ | Caughey-Thomas[47] | $\mu_{min}$ = 0, $\mu_{max}$ = 1464.7 $N_{ref}$ = 7.5×10$^{17}$, $\gamma$ = 0.825 $\alpha$ = 0, $\beta$ = 0 | Si, $E_C - E_D$ = 220 meV[53] |

[a]Units of Thornber fit parameters: $E_i$, $E_{th}$, $E_r$ (eV), $\lambda$ (cm); [b]Units of Okuto-Crowell fit parameters: $a_{n/p}$, $b_{n/p}$ (V/cm), $\gamma$ (unitless)
[c]Units of Chynoweth fit parameters: $a_{n/p}$, $b_{n/p}$ (V/cm); [d]Units of Caughey-Thomas fit parameters: $\mu_{min}$, $\mu_{max}$ (cm$^2$/Vs), $N_{ref}$ (cm$^{-3}$), $\alpha$, $\beta$, $\gamma$ (unitless)

[c]Units of parameters in Ma's fit to β-$Ga_2O_3$ electron mobility: $a$ ($cm^2$/Vs), $T_c$ (K), $N_{ref}$ ($cm^{-3}$), $b$, $d$ (unitless)
[f]Units of Modified Caughey-Thomas fit parameters: $\mu_{min}$, $\mu_{max}$ ($cm^2$/Vs), $N_{ref}$, $N_\beta$ ($cm^{-3}$), $\beta_1$, $\gamma$, $\kappa$ (unitless)
[g]$E_C - E_D$ is the donor energy level and $E_A - E_V$ is the acceptor energy level

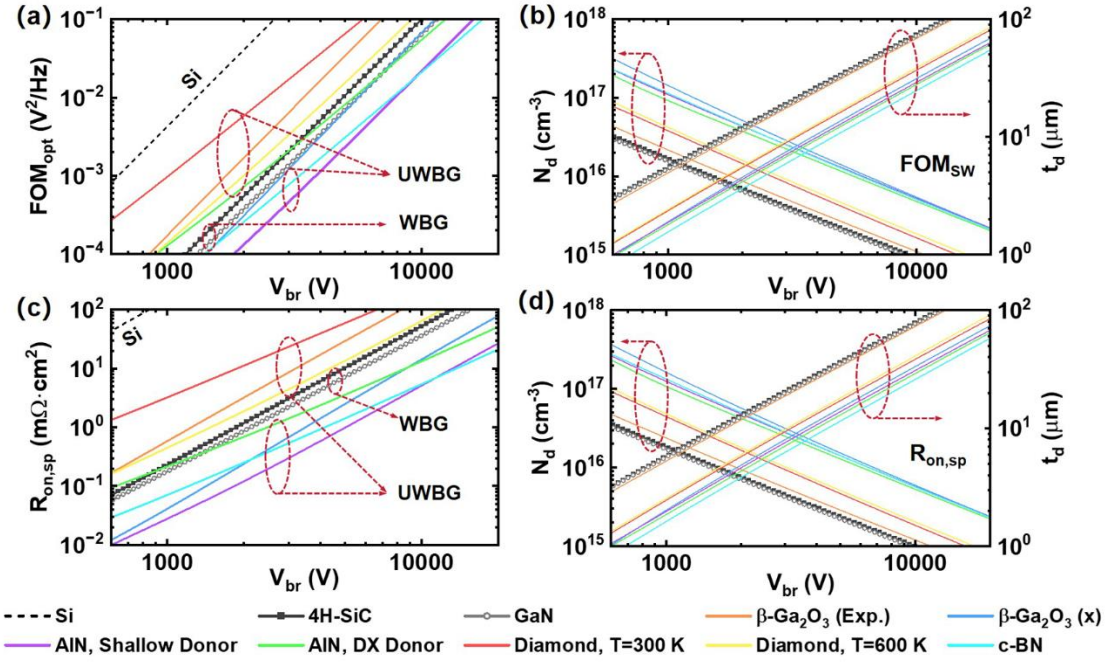


Fig. 7. (a) Optimal hard-switching FOM and (b) corresponding optimal drift layer design versus breakdown voltage for Si, WBG and UWBG materials from 200 V to 20 kV. (c) Optimal $R_{on,sp}$ and (b) corresponding drift regions versus breakdown voltage. Materials considered here include Si, 4H-SiC, GaN, β-$Ga_2O_3$ (based on experimental impact ionization coefficients and the theoretical values along the x-direction), AlN (based on shallow and DX donors), diamond (at temperatures of 300 K and 600 K), and c-BN.

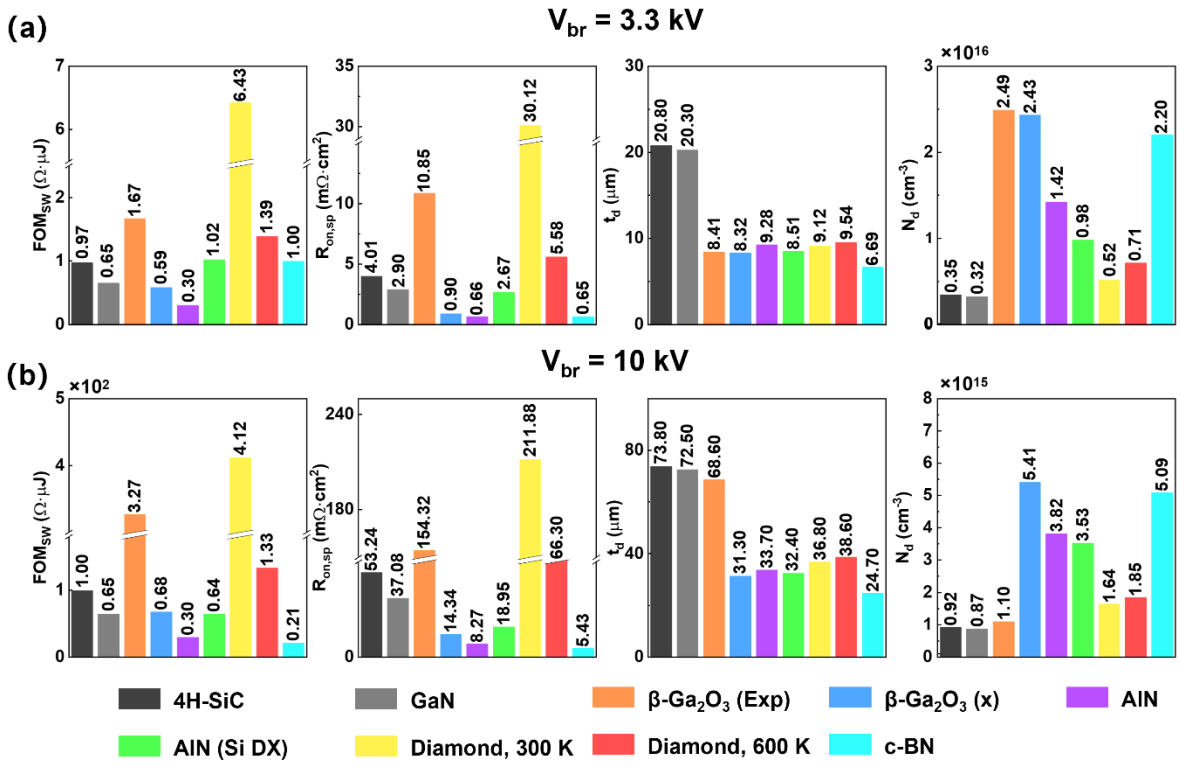


Fig. 8. Optimal switching FOM for WBG and UWBG materials, as well as the corresponding drift region designs, at the breakdown voltage of (a) 3300 V and (b) 10 kV. The calculated optimal $R_{on,sp}$ is shown for each material for comparison. Breakpoints in the y-axes are added for the switching FOM and $R_{on,sp}$ plots due to the high optimal values obtained for diamond and β-$Ga_2O_3$, and are indicated on the y-axis and the data-bars accordingly.

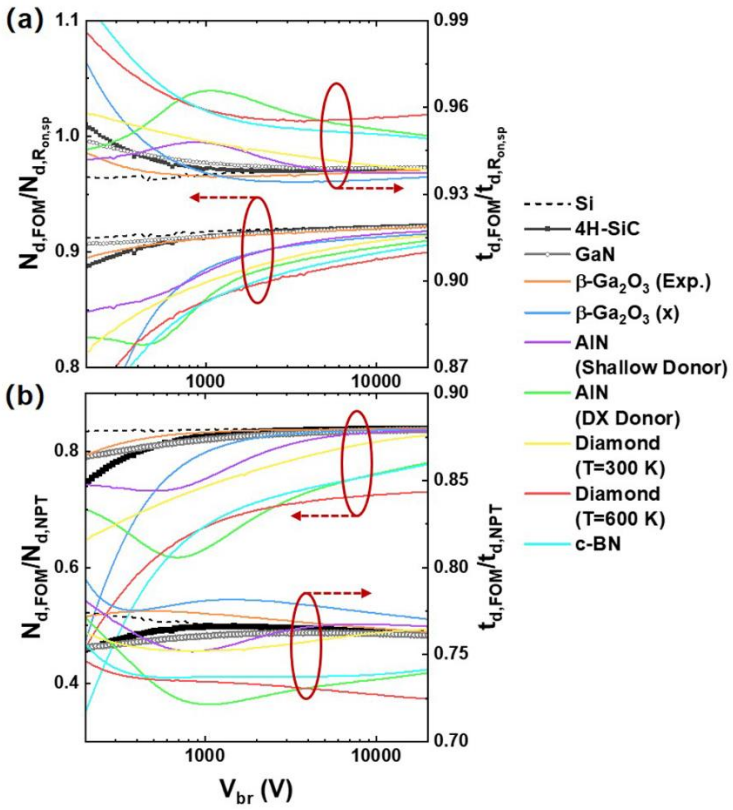


Fig. 9. Ratio of the FOM-optimized drift layer design parameters $N_d$ and $t_d$ to the (a) $R_{on,sp}$ optimized parameters and to the (b) NPT drift layer parameters, both versus breakdown voltage.

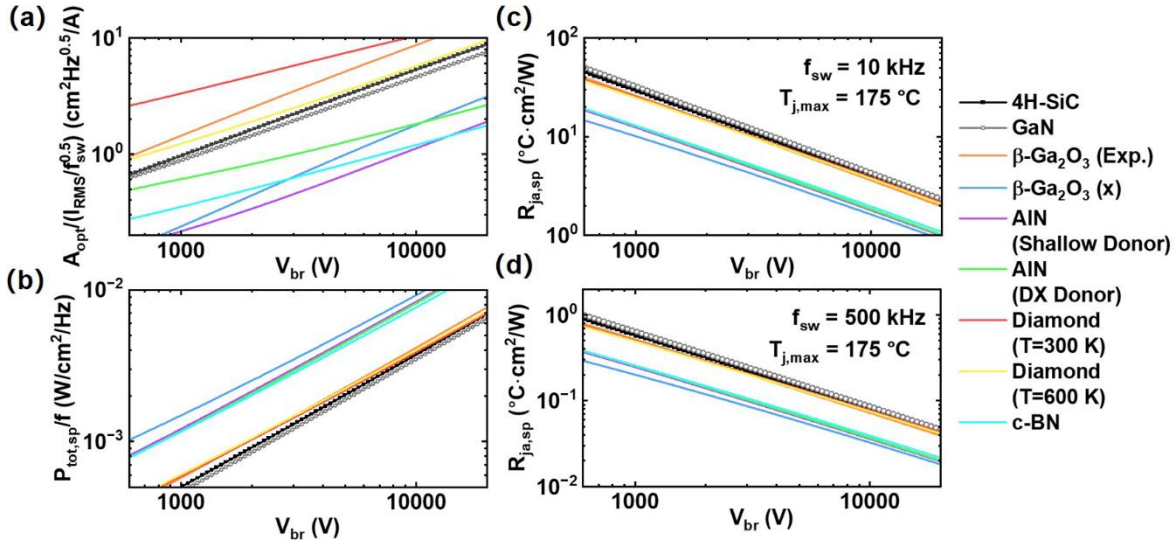


Fig. 10. (a) Switching FOM optimal area of WBG and UWBG devices versus breakdown voltage, for $I_{RMS}$ = 10 A and $f_{SW}$ = 10 kHz and (b) Frequency-normalized limit of power loss densities versus breakdown voltage from 200 V to 20 kV for WBG and UWBG devices. The upper limit of $R_{ja,sp}$ of UWBG and WBG devices versus breakdown voltage at two exemplar frequencies (c) 10 kHz and (d) 500 kHz.