Ultra-low I_Q Fully Integrated NMOS LDO with Enhanced Load Regulation and Startup for RF Energy Harvesting Sensors

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***Abstract*—NMOS low-dropout (LDO) voltage regulator architecture with an ultra-low quiescent current is proposed for integration in radio-frequency (RF) energy harvesting sensors. The transient enhanced inverter (TEI) is added to conventional architecture to improve the load transient response. TEI reduces the output voltage undershoot/overshoot by 60.73 % and settling time by 63.88 % compared to the conventional LDO architecture. The start-up assistant RC (SARC) improves the settling time by 340 μs for the step input voltage to LDO. The NMOS LDO regulator with 15 nA quiescent current is simulated in the 180 nm CMOS technology. The line and load regulations are respectively 0.012 mV/V and 60 mV/mA with 1 pF load capacitor and maximum 1 μA load current. The PSRR is -60 dB at the low frequencies and -7.7 dB at 1 MHz.**

***Index Terms*—NMOS LDO, backscattering system, ultra-low quiescent current, transient enhanced inverter, start-up assistant RC, small load current.**

I. Introduction

RF powered backscattering sensors that harvest energy from ambient wireless signals emitted by the communication infrastructure such as TV towers and WiFi access points, can have tremendous impact on a wide deployment of Internet of Things (IoTs) [1]. Critical to this goal is design of high-performance LDOs that provide a stable supply voltage when the harvested power is weak and intermittent. There are two types of linear voltage regulators depending on the chosen type of the pass transistor, NMOS and PMOS regulators. NMOS LDO, using the N-type pass transistor, has many advantages in order to accommodate full on-chip design. Firstly, this topology pushes the output pole of the LDO to higher frequencies avoiding the need for a complex compensation [2]. Thus, the dominate pole of the LDO can be placed at the output of the error amplifier rather than the output of the LDO, which in PMOS regulators results in a need for a large external capacitor. Second, the source follower structure is not able to amplify the ripple at the gate, leading to a better PSRR [3]. Moreover, the NMOS LDO is more area efficient than PMOS LDO due to higher mobility of electrons [4], and the line and load regulation are improved [5]. However, the power efficiency of NMOS LDO is lower than PMOS LDO due to the high output voltage required at the output error amplifier. In RF energy harvesting systems, a higher supply voltage for the error amplifier can be supplied with additional stage of voltage multiplier, without the need for a more complex DC-DC converter [6].

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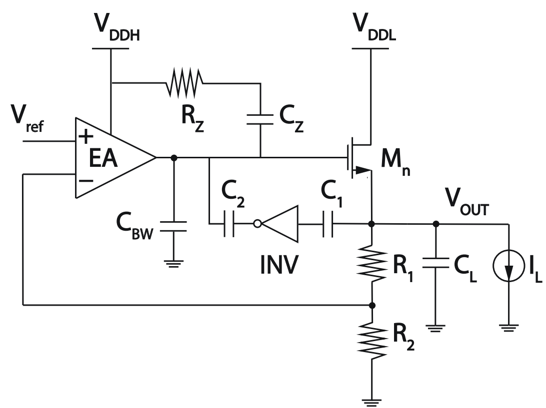


Fig. 1. Schematics of the proposed NMOS LDO with improved load regulation and start-up time.

A low quiescent current PMOS LDO with I_Q of 3.08 nA was introduced in [7]. However, the load transient response is poor, with high levels of the output voltage overshoot and undershoot. A sub-nA fully on-chip NMOS LDO is reported in [8]. It achieves a 970 pA quiescent current with a 13.6 ms settling time, which presents an issue in RF backscatter-based sensors. A detailed analysis of this type of NMOS LDO is presented in [6]. In this work, we propose a fully on-chip NMOS LDO with the TEI and the SARC to simultaneously match the requirements of the backscattering RF sensor with the low I_Q, improved settling time and fast start-up.

In Section II, the fully integrated NMOS LDO regulator, with the transient enhanced inverter and the start-up assistant RC, is presented. Simulation results and analysis are shown in Section III, with the conclusions outlined in Section IV.

II. Proposed NMOS LDO Implementations

The proposed implementation of LDO with NMOS pass transistor is shown in Fig. 1, with the transient enhanced inverter and the start-up assistant added to the conventional architecture with two supply voltages [6]. The TEI as a negative feedback circuit is connected between the output of LDO and output of EA to improve the load transient response. It comprises an inverter for phase change and two coupling capacitors C_1 and C_2. A series connected capacitor C_Z and resistor R_Z, placed between the output of EA and V_{DDH}, improve the start-up of the LDO.

The corresponding transistor level regulator design is depicted in Fig. 2. The voltage difference between V_{DDH} and V_{DDL} is nominally 200 mV to secure a high gain of the EA, which is critical for the high loop gain in NMOS pass transitor based LDO. The size of NMOS pass transistor is $W/L = 512\mu m/500nm$ and the transistor is operating in the weak inversion region under the maximum 1 μA load current I_L. The folded cascode structure is used for the error amplifier design. All transistors operate in the weak inversion region due to the low quiescent current. The very large output resistance offers a high DC gain that can be obtained from only one stage, avoiding complex compensation. The dominant pole of the system is at the EA output rather than the LDO output, which enables a fully on-chip design of the regulator. The tail current from M_{11} is set at 2 nA, with M_3 and M_4 having the same drain current as M_{11}.

Based on the small signal model in Fig. 3, poles and zeros of the LDO open-loop are estimated. The output resistance of the EA R_{outA}, the bandwidth capacitor C_{BW}, and the R_Z and C_Z of the SARC jointly contribute to the dominate pole, the second pole and a zero as follows [9]

$$\begin{aligned} w_{p1} &= \frac{1}{R_{outA}C_Z} \\ w_{p2} &= \frac{1}{R_Z C_{BW}} \\ w_{z1} &= \frac{1}{R_Z C_Z}. \end{aligned} \tag{1}$$

The pass NMOS transistor and the load capacitor C_L contribute to a pole and a zero as

$$\begin{aligned} w_{p3} &= \frac{g_{mn}}{C_L} = \frac{I_L}{nU_T C_L} \\ w_{z2} &= \frac{g_{mn}}{C_{gsn}}, \end{aligned} \tag{2}$$

where g_{mn} and C_{gsn} are the transconductance and gate-source capacitance of the pass NMOS, I_L is the load current of LDO, U_T is the thermal voltage, n is a factor related to source-to-substrate voltage [10]. Since the load resistor R_L is usually very large, it can be ignored in the equation.

The TEI generates 2 poles and 2 zeros

$$\begin{aligned} w_{p4} &= \frac{1}{RC_1} \\ w_{p5} &= \frac{1}{R_o C_2} \\ w_{z3} &= \frac{C_1 R + C_2 R_o + C_{gd} R g_{m1} R_o + K}{2C_1 C_2 R R_o} \\ w_{z4} &= \frac{C_1 R + C_2 R_o + C_{gd} R g_{m1} R_o - K}{2C_1 C_2 R R_o}, \end{aligned} \tag{3}$$

where

$$\begin{aligned} K = [&(C_1 R - C_2 R)^2 + g_{m1} R R_o C_{gd} \\ &\times (2C_1 R + 2C_2 R_o + g_{m1} R R_o C_{gd})]^{\frac{1}{2}}, \end{aligned} \tag{4}$$

and g_{m1}, R_o, C_{gs} and C_{gd} are the transconductance, output resistance, gate-source capacitance and gate-drain capacitance of M_{30} (or M_{32}). R is the total resistance at the drain of M_{31} (or M_{33}), which equals $\frac{1}{g_{mT}}||r_o||\frac{R_T}{2}$, where g_{mT} and r_o are related transconductance and output resistance.

A. Transient Enhanced Inverter

Different feedback structures have been proposed for analog-assisted digital LDOs to attain faster transient response [11]. In the proposed TEI, capacitors C_1(=$2C_{1a}$=$2C_{1b}$) and C_2 sense and feedback the signal change from the load and cut off the path of the DC signal. For an NMOS regulator, an inverter comprising M_{30} and M_{32} has to be added for phase change. The inverter is biased by transistors M_{31} and M_{33}, and a resistor R_T. A 133 MΩ R_T is used to generate a 5 nA biasing current.

B. Start-up Assistant RC

This SARC structure comprises serially connected R_Z and C_Z as a high pass filter. When the regulator input voltage is applied at a start-up, the SARC provides a path from V_{DDH} to the gate of pass NMOS transistor. In the design, R_Z was realized by a diode connected PMOS. The value of C_Z can be properly chosen to cancel pole and zero based on (1).

III. Simulation Results

The proposed NMOS LDO voltage regulator is designed in 180 nm CMOS technology and simulated in Cadence simulation environment. The output voltage of the regulator, V_{out}, is set at 0.8 V and the regulator is designed to operate with the input voltage V_{DDL} of 1 V, thus the nominal dropout voltage is 200 mV. The simulated quiescent current I_Q is 15 nA. We first show the dependence of the output voltage on the input voltage of the regulator in Fig. 4, with the dropout voltage as low as 16 mV. For all values of the input voltage, the voltage V_{DDH} is 200 mV higher than V_{DDL}.

Fig. 5 compares the output voltages between the conventional and the proposed LDO with different Rz and Cz configurations when starting V_{ref}, V_{DDH} and V_{DDL} with 10 ns rise time. With the addition of SARC, the proposed LDO improves response when voltages start up, since V_{DDH} directly charges the gate of the pass NMOS during the transition. After the supply voltages settle, the gate voltage of the pass NMOS initially drops due to the charge loss before increasing again with reduced settling time.

The open-loop magnitude and phase are shown in Fig. 6 for different values of the capacitors C_1 and C_2 in the TEI. The C_1 was chosen as 500 fF, 1 pF and 10 pF, with the value of C_2 fixed at 1pF, and vice versa. From (3), poles at w_{p4} and w_{p5} become lower with the increase of the capacitance. The phase margins for the two cases are denoted in Fig. 6. With the increments of C_1, LDO response changes from overdamping

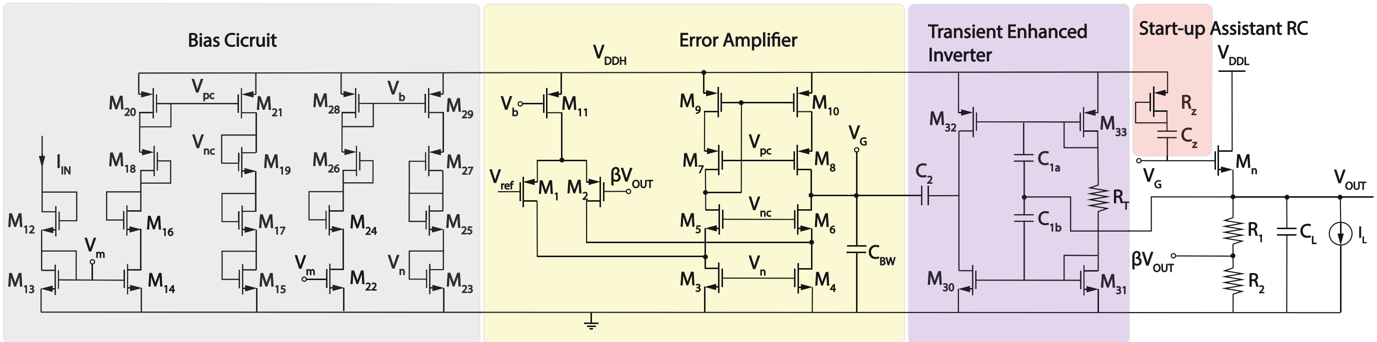


Fig. 2. Transistor-level schematic of the proposed NMOS LDO voltage regulator.

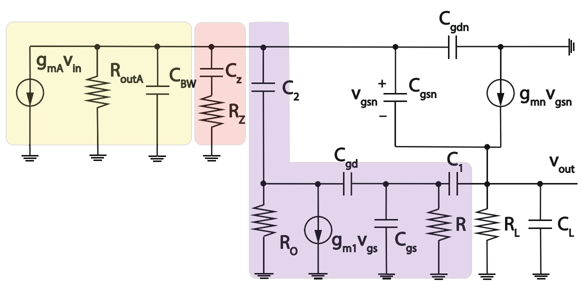
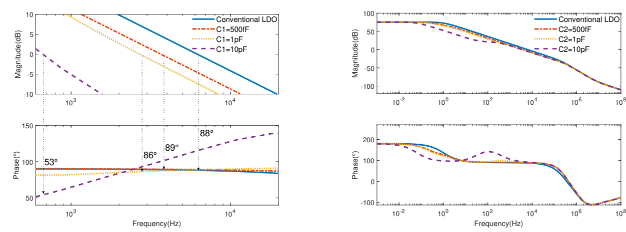


Fig. 3. Small signal model of implemented voltage regulator.



(a) (b)

Fig. 6. Open-loop magnitude and phase when sweeping (a) C_1 and (b) C_2.

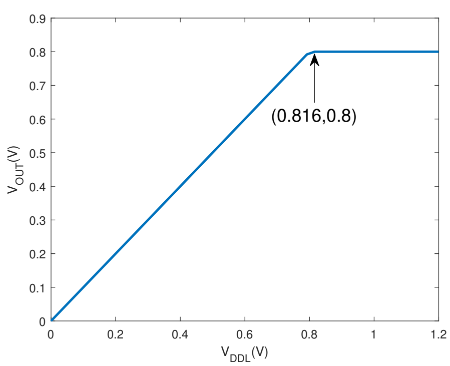


Fig. 4. Output voltage of LDO as a function of input voltage.

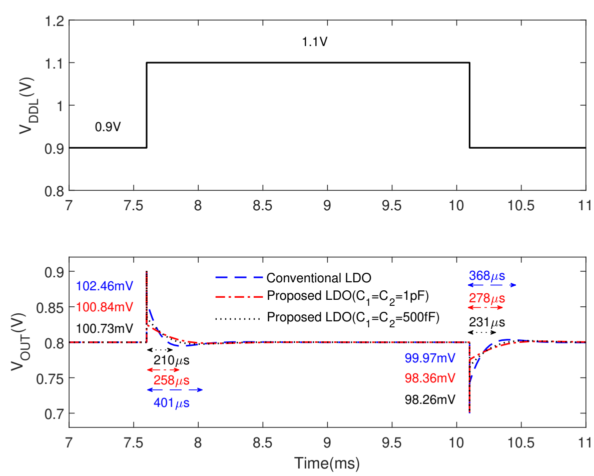


Fig. 7. Line transient response of conventional and proposed LDO.

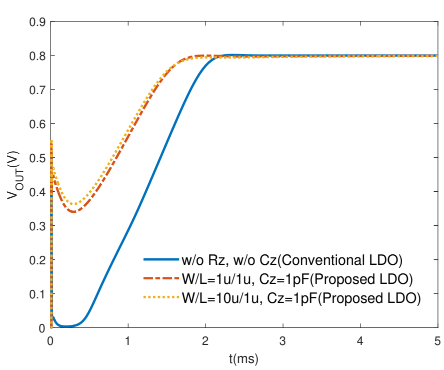


Fig. 5. Output voltages of the conventional and proposed LDO with different R_Z and C_Z at start-up.

to underdamping. Moreover, the pole w_{p5} decreases, resulting in reduced open-loop bandwidth, as shown in Fig. 6(b). When C_2 equals 1 pF, the open-loop gain between 1 Hz and 100 Hz is 8 dB lower than that of the conventional LDO; when C_2 equals 500 fF, it is approximately 5 dB lower than that of the conventional LDO.

Fig. 7 shows that the line regulation of the LDO for the 200 mV the input voltage step is 0.012 mV/V. The overshoot and undershoot in the output voltage have close values in different settings. However, settling times are lowered to 52.37 % and 62.77 % of those of the conventional LDO when

TABLE I
PERFORMANCE COMPARISON

	[12]	[13]	[8]	[14]	[7]	[6]	[15]	This Work
Year	2018	2019	2020	2020	2021	2021	2022	2022
CMOS Technology(nm)	65	65	65	180	180	180	500	180
LDO Type	Analog	Digital	Analog	Analog	Analog	Analog	Hybrid	Analog
V_{IN}(V)	1	0.5-1	1.5	1.8	1.8	1.4	3-6	1
V_{OUT}(V)	0.8	0.4-0.95	0.5	1.1	1.2	1.2	2.3-3.3	0.8
Dropout Voltage(mV)	200	50	300	50^*	40^*	200	300	200
$\triangle V_{out}@\triangle I_{load}$(mV)	487.5	76.5	151	812.5^*	785	313	75	201
I_L(mA)	10	0.27	0.5	3.86	11	0.01	50	0.001
I_Q(nA)	30	0.745	0.97	1.88	3.08	6.5	10	15
Load Capacitor(pF)	10	1×10^5	NA	NA	10	1	220	1
Line Regulation(mV/V)	NA	NA	20^*	1.7	0.71	0.003	NA	0.012
Load Regulation(mV/mA)	1.22	NA	1.1^*	40.2	8.62	8	1.2	60
Settling Time(μs)	0.25	48	1.36×10^4	9.8×10^2	147	189.86	0.06	442
PSRR(dB)	-24@1MHz	NA	NA	-7@10KHz	-5.2@10KHz	-22@1MHz	NA	-7.7@1MHz

NA: Not Applicable; *: Not given directly but accessed or calculated from contents or figures.

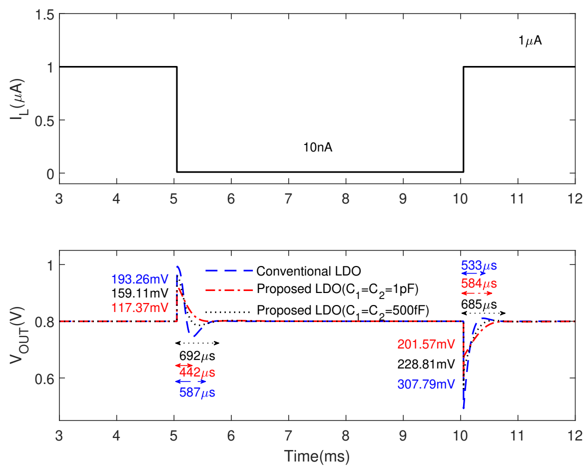


Fig. 8. Load transient response of conventional and proposed LDO.

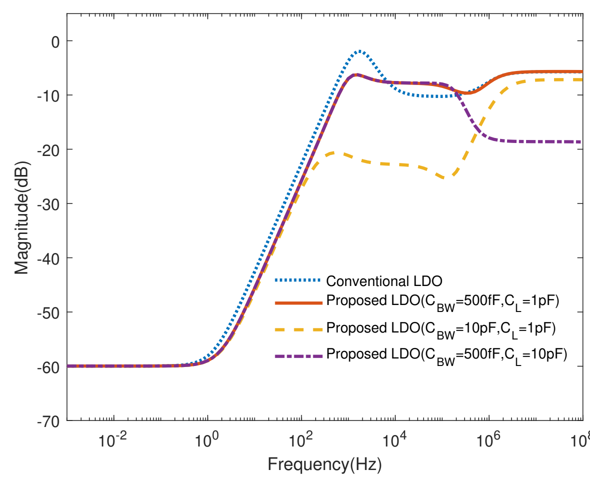


Fig. 9. PSRR comparisons of conventional and proposed LDO for different C_{BW} and C_L.

V_{DDL} changes from 0.9 V to 1.1 V and then to 0.9 V with $C_1 = C_2 = 500$ fF; settling times are 64.34 % and 75.54 % when V_{DDL} keeps the same change but $C_1 = C_2 = 1$ pF. Fig. 8 shows the output voltage when the I_L, with 50 ns rise and fall times, is changed between 10 nA and 1 μA. The load regulation is 60 mV/mA. Under the condition of $C_1 = C_2 = 1$ pF, phase margin is relatively smaller but does not result in underdamping oscillation; and the lower bandwidth relieves the effect from the post-transition overshoot and undershoot. Settling times of 0.375 % precision are 63.88 % (442 μs) and 85.26 % (584 μs) of those of the conventional LDO when I_L changes from 1 μA to 10 nA and then to 1 μA, respectively; overshoot and undershoot are reduced to 60.73 % (117.37 mV) and 65.49 % (201.57 mV).

Fig. 9 demonstrates that the proposed LDO improves the PSRR from -3.7 dB to -7 dB at 1 kHz since the ripple from V_{DDH} is directly applied on gate of the pass NMOS through the SARC rather than amplified by the cascade PMOS transistors in EA. From the PSRR transfer function in [6], the C_{BW} and C_L have a major influence on the PSRR above LDO bandwidth frequency. A larger C_{BW} flattens PSRR earlier at low frequencies rather than continuing to rise. Once C_{BW} was increased to 10 pF, the PSRR at 1 kHz becomes -21.2 dB. In addition, a larger C_L moves the second zero higher and the second pole lower in related functions, which leads to a magnitude drop of the PSRR at high frequencies. Correspondingly, the PSRR is pulled down to -17.9 dB from -7.7 dB at 1 MHz when replacing 1 pF C_L by a 10 pF one.

The comparison with the state-of-the-art designs is shown in Table I. The LDO in this work has an equivalent 1 pF load capacitor. With the 1 μA maximum load current and 15 nA low quiescent current, the proposed LDO is a good candidate for integration in the power management block of the RF energy harvesting sensor.

IV. CONCLUSION

A fully integrated 15 nA ultra-low I_Q NMOS LDO with transient enhanced inverter and start-up assistant RC for RF energy harvesting devices is analyzed and designed. The design will be integrated in the RF backscattering tag in order to provide the voltage supply for powering of the ultra-low power low-resolution successive-approximation analog-to-digital converter.

References

[1] M. Stanaćević, A. Athalye, Z. J. Haas, S. R. Das, P. M. Djurić, "Backscatter Communications with Passive Receivers: From Fundamental to Applications," *ITU Journal on Future and Evolving Technologies*, vol. 1, no. 1, 2020. [Online]. Available: http://handle.itu.int/11.1002/pub/8173ddf7-en

[2] P. Hazucha, T. Karnik, B. Bloechel, C. Parsons, D. Finan, and S. Borkar, "Area-efficient linear regulator with ultra-fast load regulation," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 4, pp. 933–940, 2005.

[3] J. Jiang, W. Shu, and J. Chang, "A 65-nm cmos low dropout regulator featuring >60-db psrr over 10-mhz frequency range and 100-ma load current range," *IEEE Journal of Solid-State Circuits*, vol. PP, pp. 1–12, 05 2018.

[4] K. Li, C. Yang, T. Guo, and Y. Zheng, "A multi-loop slew-rate-enhanced nmos ldo handling 1-a-load-current step with fast transient for 5g applications," *IEEE Journal of Solid-State Circuits*, vol. 55, no. 11, pp. 3076–3086, 2020.

[5] S.-Y. Peng, L.-H. Liu, P.-K. Chang, T.-Y. Wang, and H.-Y. Li, "A power-efficient reconfigurable output-capacitor-less low-drop-out regulator for low-power analog sensing front-end," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, no. 6, pp. 1318–1327, 2017.

[6] P. Zheng, X. Sha, and M. Stanaćević, "Analysis of the sub-μa fully integrated nmos ldo for backscattering system," in *2021 IEEE 34th International System-on-Chip Conference (SOCC)*, 2021, pp. 52–56.

[7] Pereira-Rial, P. López, J. M. Carrillo, V. M. Brea, and D. Cabello, "An 11 ma capacitor-less ldo with 3.08 na quiescent current and ssf-based adaptive biasing," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 69, no. 3, pp. 844–848, 2022.

[8] S. Li and B. H. Calhoun, "Sub-microamp energy harvesting and power management units for self-powered iot socs: Analog vs. digital implementations," in *2020 IEEE Custom Integrated Circuits Conference (CICC)*, 2020, pp. 1–8.

[9] Y. Li, "A nmos linear voltage regulator for automotive applications," Ph.D. dissertation, Delft University of Technology, 2012.

[10] E. Vittoz and J. Fellrath, "Cmos analog integrated circuits based on weak inversion operations," *IEEE Journal of Solid-State Circuits*, vol. 12, no. 3, pp. 224–231, 1977.

[11] M. Huang, Y. Lu, and R. P. Martins, "Review of analog-assisted-digital and digital-assisted-analog low dropout regulators," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 68, no. 1, pp. 24–29, 2021.

[12] Y. Huang, Y. Lu, F. Maloberti, and R. P. Martins, "Nano-ampere low-dropout regulator designs for iot devices," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 11, pp. 4017–4026, 2018.

[13] S. Li and B. H. Calhoun, "14.6 a 745pa hybrid asynchronous binary-searching and synchronous linear-searching digital ldo with 3.8×105 dynamic load range, 99.99% current efficiency, and 2mv output voltage ripple," in *2019 IEEE International Solid- State Circuits Conference - (ISSCC)*, 2019, pp. 232–234.

[14] Pereira-Rial, P. López, J. M. Carrillo, V. M. Brea, and D. Cabello, "1.88 na quiescent current capacitor-less ldo with adaptive biasing based on a ssf absolute voltage difference meter," in *2020 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2020, pp. 1–5.

[15] J.-R. Huang, Y.-H. Wen, T.-H. Yang, J.-J. Lee, G.-T. Liu, K.-H. Chen, Y.-H. Lin, S.-R. Lin, and T.-Y. Tsai, "A 10 na ultra-low quiescent current and 60 ns fast transient response low-dropout regulator for internet-of-things," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 69, no. 1, pp. 139–147, 2022.