

# A 4-Phase DAB Current-Mode Hysteretic Controlled Buck Converter With Relaxed Inductor Requirements and Enhanced DC and Dynamic Performance

Lei Zhao<sup>ID</sup>, *Student Member, IEEE*, Junyao Tang<sup>ID</sup>, *Student Member, IEEE*,  
Kang Wei<sup>ID</sup>, *Member, IEEE*, and Cheng Huang<sup>ID</sup>, *Member, IEEE*

**Abstract**—This article presents a four-phase current-mode hysteretic-controlled DC–DC buck converter with fixed-frequency double-adaptive-bound (DAB) control. In prior current-mode converter designs, there exists undesired output DC error caused by control loop delays and mismatches between the  $RC$  current sensing network and the DC resistance (DCR) of the power inductor. Circuit delay is also an obstacle in achieving higher switching frequency and multi-phase operation. To address these issues, ratioed sensing  $RC$  network and digital output DC calibration are proposed. To reduce the efficiency degradation caused by imbalanced phase current, digital current balancing (CB) calibration is also developed. To maintain a high efficiency with a wide output load range, digital active-phase-count (APC) function was also introduced, with burst mode (BM) to improve transient responses at fast load current steps. The proposed converter has been fabricated in 180-nm CMOS process and measured at 10 and 25 MHz with 18-to-100-nH miniature 0402 inductors, converting 1.8-V supply ( $V_{IN}$ ) to 0.6–1.5-V output with 93.9% peak efficiency.

**Index Terms**—Buck, DC–DC converter, digital calibration, double adaptive bound (DAB), efficiency, hysteretic control, load regulation, multi-phase, transient response.

## I. INTRODUCTION

MODERN microprocessors can achieve peak performance boosting supported by bursts in current consumption. The currents can be dynamically scaled with larger than 1-A/ns slew rate when the microprocessor switches between different operation conditions [1]. Inductor-based buck converters can offer high power efficiency and have been a popular candidate to provide tightly regulated point-of-load (PoL) voltage for microprocessors. Voltage droops need be minimized to keep the microprocessor alive above its minimum operation supply voltage with large and fast transient load steps. From large-signal perspective, smaller

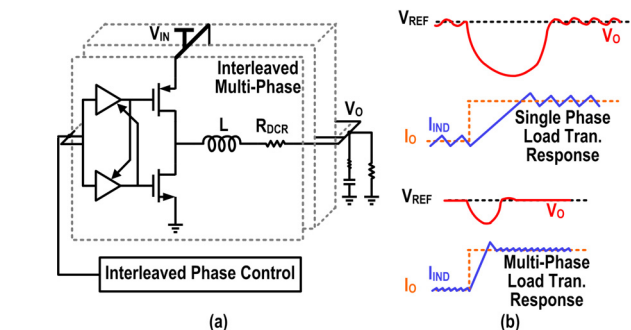


Fig. 1. (a) Illustration of a multi-phase buck converter and (b) comparison with a single-phase converter: faster transient response and smaller voltage and current ripples.

inductors are preferred since they can be charged/discharged with larger  $di/dt$  slew rate to reduced voltage droop. Smaller inductance also helps achieve a higher level of integration. With such smaller inductors below 100 nH range [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], the switching frequency needs to be boosted (to above 10 MHz even higher) to achieve acceptable inductor current and output voltage ripples. As shown in Fig. 1, compared with single-phase operation, multi-phase operation can extend the power delivery capability and further speed up the transient response [1], [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [15], [16], [17], [18]. With interleaved  $N$ -phase operation, the equivalent inductor current ripple can be reduced significantly due to the ripple cancellation effect, high heavy-load efficiency can be achieved with spread current stress and reduced resistance, and the inductor charging/discharging slew rate can be enhanced by  $N$  times. In addition, for multi-phase converters, digital-intensive controller has been demonstrated for its benefits of scalability with technology node migration and to extend the number of phases for higher current capacity [6].

Traditional linear pulswidth modulation (PWM) control features a fixed switching frequency operation [2], [5], [21], [22], [23] and has been widely adopted for multi-phase design [2], [5], [21]. However, in terms of closed-loop response, linear control always has small-signal bandwidth limitation. This limitation can be further compromised to ensure stability at different loading conditions with PVT and  $LC$  components

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Lei Zhao, Junyao Tang, and Cheng Huang are with the Department of Electrical and Computer Engineering, Iowa State University, Ames, IA 50011 USA (e-mail: leizhao@iastate.edu; chengh@iastate.edu).

Kang Wei is with Texas Instruments, Dallas, TX 75243 USA.

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variations. To eliminate small-signal limitations and potentially achieve a faster dynamic response, non-linear control, such as hysteretic control, has been implemented in the main control loop of switching-mode converters [3], [15], [17], [19] or been introduced in the extra hybrid path [20]. For the hybrid scheme in [20], the digital controlled switches can be fully turned ON/OFF to significantly speed up the transient response by comparing the error amplifier output with a window. Compared with monitoring the output directly, this helps improve the noise immunity. However, the bandwidth of the error amplifier still limits its response. In addition, to achieve stable operation with different PVT/component/load variations, the bandwidth of the analog loop and the strength of the digital path need to be carefully designed and optimized. For hysteretic control in the main loop, there are two typical hysteretic control strategies, i.e., voltage mode and current mode are widely used. Voltage-mode control is based on monitoring only the output voltage ( $V_O$ ) ripples, which is difficult to be adopted in multi-phase converters because of the single  $V_O$  ripple information. It usually has variable switching frequency with unpredictable noise spectrum, which is undesired for noise-sensitive systems. Traditional current-mode hysteretic control topology using current sensor or  $RC$  network also suffers from variable switching frequency [17]. To achieve a fixed switching frequency operation, different clock synchronization techniques have been introduced [3], [15], [17], [19]. In [17], a delay-lock-loop was designed and, however, also introduced small-signal limitations and stability concerns with extra delay elements that is counterproductive for fast dynamic response. An external clock was used to reset the comparison boundary periodically [3], [15]. However, to ensure proper operation at higher switching frequency, careful matching between the inductor current-sensing  $RC$  network and the inductance and parasitic DCR of power inductors or the matching between the  $RC$  pairs [15] or a more complex  $RC$  sensing network [3] is required.

Double-adaptive-bound (DAB) hysteretic control in [19] has been demonstrated for fixed frequency operation and fast transient response. However, it only works in single phase, and the operation is sensitive to the delay of comparator, the gate driver and other circuits in control path, and the matching of the  $RC$  filters, especially at higher switching frequencies.

Due to the lack of a high-gain amplifier, output voltage DC accuracy is also compromised in hysteretic-controlled switching converters [15]. In addition, for multi-phase converter, imbalanced current could be introduced due to mismatches in power transistors, control timing, and power inductors between phases, which could increase the equivalent inductor current ripple and compromise power efficiency significantly [18], [24]. Another consideration for multi-phase converter is to only keep an optimized number of phases in active according to the loading condition. At relatively lighter loading conditions, if all the phases are alive, the switching loss can degrade the power efficiency significantly. Thus, active-phase-count (APC) control has been introduced [2], [6], [15], [16], [18].

To address the abovementioned limitations and issues, this article proposes a four-phase DAB current-mode hysteretic-controlled buck converter with fixed-frequency operation and

digital calibration techniques for DC output voltage calibration, current balancing, and APC management. These digital calibration functions are all based on similar bidirectional-shift registers-controlled logics, which makes the converter easily extendable to adapt more phases with minimum design complexity overhead.

The rest of this article is organized as follows. The analysis of the limitations of inductor current  $RC$  sensing network in previous current-mode hysteretic controlled converter designs is presented in Section II. The operation principle and circuit implementation of the proposed four-phase DAB hysteretic-controlled buck converter, including the design circuitry details and considerations for the developed digital calibration functions, are described in Section III. Measurement results are discussed in Section IV to verify the effectiveness of the designed functions. Finally, Section V gives the conclusion of the proposed converter design.

## II. ANALYSIS OF $RC$ SENSING NETWORK RELATED ISSUES: OUTPUT DC ERROR AND SWITCHING FREQUENCY CORRUPTION

DAB control was introduced in [19], achieving fixed frequency non-linear control with simplified circuit complexity. Fig. 2(a) illustrates the system diagram of the DAB hysteretic control in [19], which employs a pair of  $RC$  filters to establish the adaptive hysteretic boundary for output voltage regulation. By leveraging the inherent delay from the comparator output to the switching node, two ramps are created and intersect with each other to generate the duty-cycle control signal for inductor charge/discharge. However, there are mainly two closely related issues associated with the  $RC$  current sensing network and circuit delays: output DC error and switching frequency corruption.

### A. Output DC Error

The DAB control in [19] does not include DC information in the reference path, as shown in Fig. 2(a) and (b). Without DC information, although AC information can be used to accelerate the response when load transient happens,  $V_O$  in fact is not being regulated.  $V_O$  is not correlated to  $V_R$ , thus will result in a random DC voltage. To regulate  $V_O$  to  $V_R$  and also cancel the DC error caused by DCR, a short reset period is introduced in [19] to periodically synchronize the  $V_{FB}/V_{DAB}$  boundaries with  $V_O/V_R$ . With the reset for  $V_{DAB}$ , the reference DC information is included for  $V_O$  regulation. Thus,  $V_O$  is fed to the duty predictor to generate  $D_{PRE}$ . However, this short reset period is time and noise sensitive and could cause mistriggering of the comparator, especially with higher switching frequency. Once the comparator is mistriggered, it would introduce another misreset to further disturb the original stable fixed frequency operation. As a result, chaos in operation will occur and corrupt the fixed-switching frequency behavior, which is one of the most important advantages of DAB control and is essential to extend to multiphase operation. Thus, reset mechanism is not adopted here.

To maintain  $V_O$  regulation without resetting the boundaries, in this work, the reference DC voltage information is included

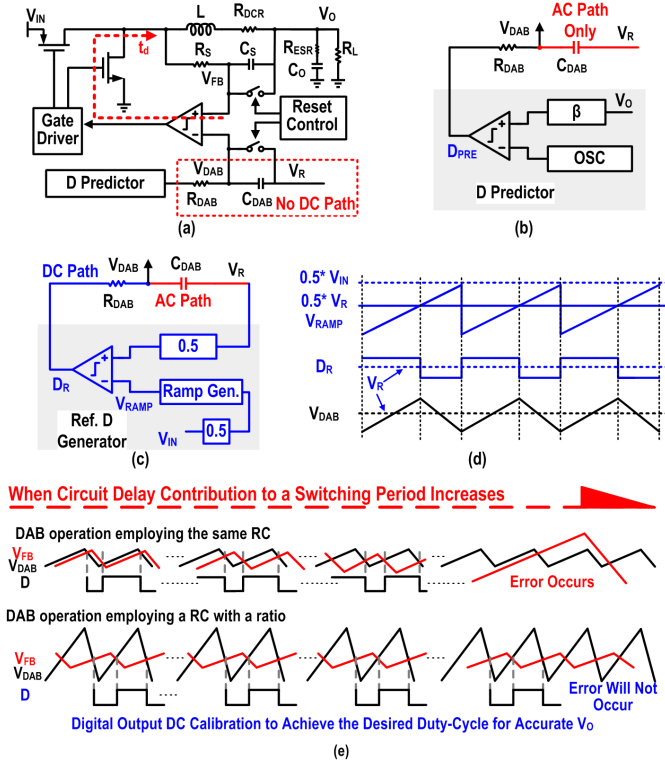


Fig. 2. (a) System diagram of a DAB-controlled buck converter and (b) duty-cycle predictor in [19]. (c) Reference duty-cycle generator in this design. (d) Illustrations of  $V_{DAB}$  DC information with timing diagram in this work. (e) Illustration of delay related error in DAB control with traditional and proposed ratioed RC network.

in the generated reference duty cycle ( $D_R$ ). As shown in Fig. 2(c) and (d),  $V_{DAB}$  is obtained with  $D_R$  low passed by the RC, thus sharing the same average value with  $D_R$ , which is equal to the reference voltage. With the DC reference information included,  $V_{DAB}$  is fed to the comparator for voltage regulation.

However, this does not completely solve the DC error issue. Even with the DC information of the reference included, circuit delays can still degrade the DC accuracy and even corrupt the desired fixed switching frequency operation (Section II-B). Fig. 2(e) illustrates the ramp waveforms with increased circuit delay, which directly impacts the output DC accuracy. As the delay increases, the DC value of output deviates from the desired point, causing a corresponding upward or downward shift in the  $V_{FB}$  waveform. Consequently, the output voltage will be larger (or smaller) than the reference.

To estimate the output voltage error resulting from the control timing delay, a MATLAB model for the basic DAB structure with two identical RC pairs is constructed. A simplified flowchart is displayed in Fig. 3 to help better understand the model. With predefined parameters for  $V_{IN}$  (supply voltage),  $V_R$  (DC reference voltage),  $T$  (period of switching frequency), resistance  $R$ , and capacitance  $C$  for RC sensing network, the reference turn-on time,  $T_{on\_r}$ , can be expressed as follows:

$$T_{on\_r} = T * \frac{V_R}{V_G}. \quad (1)$$

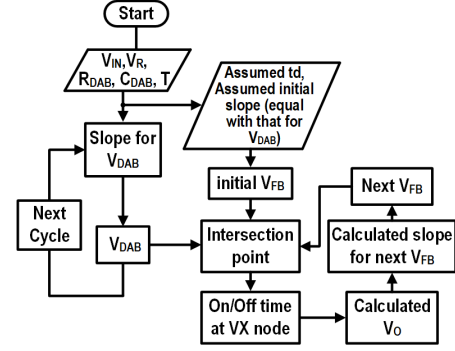


Fig. 3. Flowchart for the MATLAB model.

The rising slope ( $k_{ref\_r}$ ) and falling slope ( $k_{ref\_f}$ ) of the  $V_{DAB}$  can be expressed as follows:

$$k_{ref\_r} = \frac{V_G - V_R}{R * C} \quad (2)$$

$$k_{ref\_f} = \frac{-V_R}{R * C}. \quad (3)$$

With (1)–(3), the waveforms of the reference boundary can be plotted.

To build the feedback  $V_{FB}$  boundary, an initial delay  $t_d$  is added at one point on  $V_{DAB}$ . The rising and falling slopes of the feedback boundary are  $k_{fb\_r}$  and  $k_{fb\_f}$ . Here, we assume that this delay happens at the valley point of  $V_{DAB}$ . Thus, the coordinates of initial point of  $V_{FB}$  are assumed to be  $(t_d, -k_{ref\_f} * t_d)$ . Before intersecting with  $V_{DAB}$ ,  $V_{FB}$  is considered as having equal slope as  $V_{DAB}$  and  $V_{FB}$  is kept rising/falling to reach its peak/valley point after  $t_d$  of the intersection point. To simplify the model, the average output voltage  $V_{Oavg}$  of the  $i$ th switching cycle is assumed to be filtered from the turn-on time of the  $(i - 1)$ th switching node, which can be expressed as follows:

$$V_{Oavg(i)} = \frac{T_{on\_fb(i-1)}}{T_{fb(i-1)}} * V_G. \quad (4)$$

With the average output voltage calculated with (4), the rising and falling slope of  $V_{FB}$  can be calculated with (5) and (6). Thus, the waveforms for  $V_{FB}$  can be plotted cycle by cycle with the known slope and further obtain the intersection point between the two ramps can also be used to get the period and turn-on time of the switching node cycle by cycle

$$k_{fb\_r(i)} = \frac{V_G - V_{Oavg(i-1)}}{R * C} \quad (5)$$

$$k_{fb\_f(i)} = \frac{V_G - V_{Oavg(i-1)}}{R * C}. \quad (6)$$

With the iterative process described above, the simplified model can be developed to estimate the behavior of the RC networks. Fig. 4(a) presents the simulated two comparison ramps using the developed model for 25-MHz switching frequency operation, with  $V_{IN}$  at 1.8 V,  $V_R$  at 1.2 V,  $R = 1\text{ k}\Omega$ , and  $C = 100\text{ pF}$ . As illustrated in the 3-D plot in Fig. 4(b)–(d), the output error settles down after several switching cycles and the normalized DC error increases with larger delays. With higher switching frequency, circuit delays become more

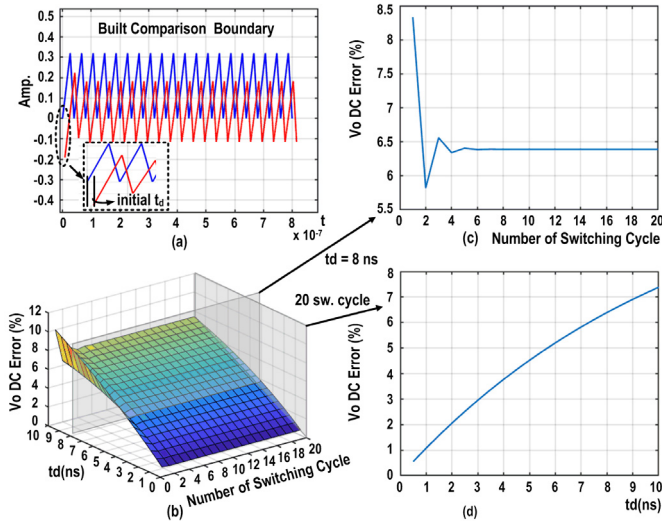


Fig. 4. Simulation results of the MATLAB model. (a) Built comparison boundary. (b) 3-D plot of normalized DC error versus delay and the settling behavior. (c) Normalized DC error with 8-ns delay time. (d) Normalized DC error versus delay at steady state.

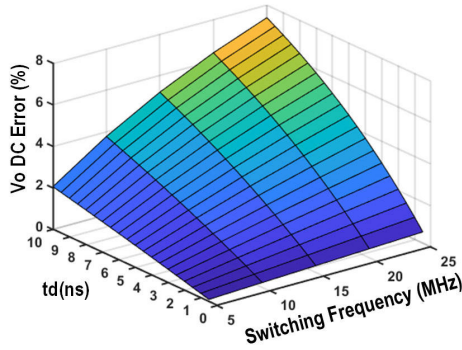


Fig. 5. MATLAB model simulation results of DC error versus delay and switching frequency.

significant with larger DC error, as verified in this model and shown in Fig. 5.

This model is simplified to focus on the analysis of the impact of  $t_d$  on the DC output accuracy to illustrate the tendency of DC error versus delay and demonstrate the necessity of delay-related DC error correction. The same tendency, DC error increases almost linearly with circuit delay, is also verified in Cadence simulation with a real power stage switched by a DAB controller. However, other factors that can also affect the slope of the ramp or the coordinates for intersection points, such as the linearity of the ramp or the matching of the RC, can also degrade the DC accuracy.

### B. Switching Frequency Corruption

With the increase of the DC offset of  $V_{FB}$  due to larger circuit delays,  $V_{FB}$  and  $V_{DAB}$  may no longer intersect each other within one reference duty-cycle period, causing sub-harmonic oscillations with a much larger ripple, as illustrated in Fig. 2(e). Because of the frequency corruption, it becomes difficult to extend DAB control to multi-phase operation to generate equally interleaved sub-phases. This delay-related

issue becomes even more pronounced with higher switching frequency, as analyzed above. To achieve a fixed switching frequency,  $V_{FB}$  must intersect with  $V_{DAB}$  both on its rising and falling durations. If the delay is larger than either of the two durations, no intersection happens in one switching period of  $V_{DAB}$ . With higher switching frequency or shorter duration for rising/falling (e.g., for a large or small duty-cycle ratio operation), it has a more stringent requirement on circuit delays for a fixed frequency operation.

## III. PROPOSED DAB HYSTERETIC CONTROLLED BUCK CONVERTER

To address the frequency corruption issue, ratioed RC networks are used in this work to allow more margin for error, as illustrated in Fig. 2(e). To address the DC output voltage accuracy limitation, especially at higher switching frequency, digital calibration technique is introduced. With less sensitivity to control loop delays and passive components variations, the DAB structure is extended to four-phase operation. Current balancing and active phase count (APC) control techniques are introduced to distribute the load current evenly among the phases and dynamically adjust the active phase number to ensure high efficiency over a wide loading range.

### A. Overall Structure of the Proposed DAB Hysteretic Control

The DAB hysteretic control was initially introduced in [19] with 10-MHz single-phase operation. To obtain fixed switching frequency operation and maintain a small voltage window between the two comparison boundaries, the propagation delay from the gate driver to the feedback controller needs to be minimized. A duty-cycle generator synchronized at a fixed external clock (CLK) was used to generate a predicted duty cycle  $D_{PRE}$ . Two identical RC filters were used to establish the hysteretic boundary. However, the adaptive hysteretic window was decided by the intrinsic delay. With a larger circuit delay, it would be more difficult for the sensed voltage  $V_{FB}$  to exceed the valley or peak value of  $V_{DAB}$ ; thus, the inductor may not be energized or deenergized fully to 100% or 0% duty cycle, losing the advantage of fast transient response of a non-linear control. These issues become more significant at higher switching frequency, which is preferred for smaller form-factor and low-cost converter designs.

In this work, to enable DAB hysteretic control at higher switching frequencies,  $R_S C_S$  is chosen to be four times of  $R_{DAB} C_{DAB}$  instead of using the identical RC values. The corresponding amplitude of the resulted boundary  $V_{DAB}$  is much larger than  $V_{FB}$ . Even though  $V_{FB}$  shifts up or down due to circuit delays,  $V_{FB}$  can still intersect with  $V_{DAB}$ , and the switching frequency remains fixed at CLK.

With the proposed ratioed RC filters, the DAB hysteretic operation features a higher tolerance of circuit delays to ensure a fixed switching frequency, which is critical for multiple-interleaving operation. In this design, a four-phase operation is chosen for demonstration. Fig. 6 illustrates the overall system diagram of the proposed buck converter. A reference duty-cycle generator, as described in Fig. 7, produces four reference duty cycles, each interleaved with 90° phase

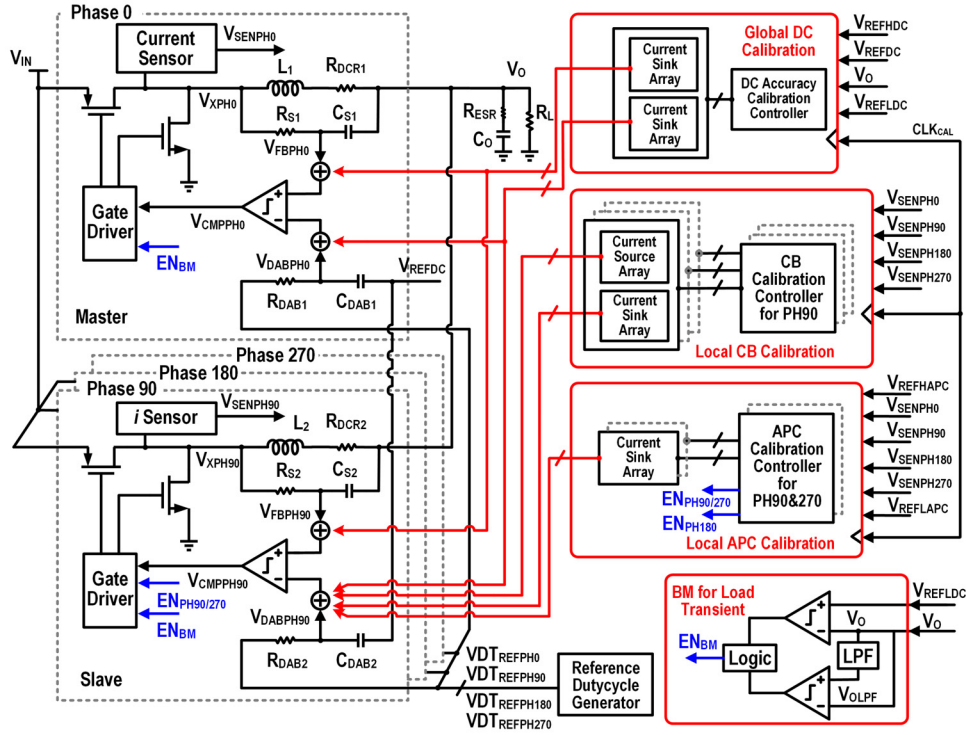


Fig. 6. System block diagram of the proposed four-phase DAB hysteretic controlled buck converter with digital calibrations.

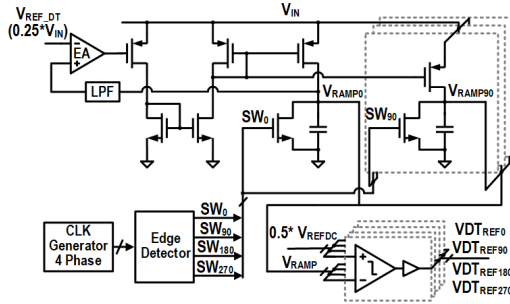


Fig. 7. Block diagram of the four-phase reference duty-cycle generator.

difference. The clock generated by the on-chip oscillator is divided by 4 to synchronize the corresponding ramp generator. To generate precise reference duty-cycle signals, the average of  $V_{RAMP0(90/180/270)}$  is regulated to be  $0.25 \times V_{IN}$ , thus with a regulated peak value of  $0.5 \times V_{IN}$  by controlling the charging current of a capacitor. With  $0.5 \times V_{REFDC}$  voltage intersecting the ramp, accurate reference duty cycles can be obtained and are fed into the corresponding  $R_{DAB}C_{DAB}$  network in each phase, and the corresponding DAB hysteretic controller regulates the corresponding phase. Digital DC offset calibration is introduced to act on the four phase globally. Set the phase  $0^\circ$  as the reference phase, local CB and APC calibration are also developed for the other three phases. With the proposed calibration loops, the matching requirement of the passive components and control timing for individual phase or among different phases can be significantly relaxed. For each phase, the controller, including the DAB main controller and respective digital calibration controllers for each phase,

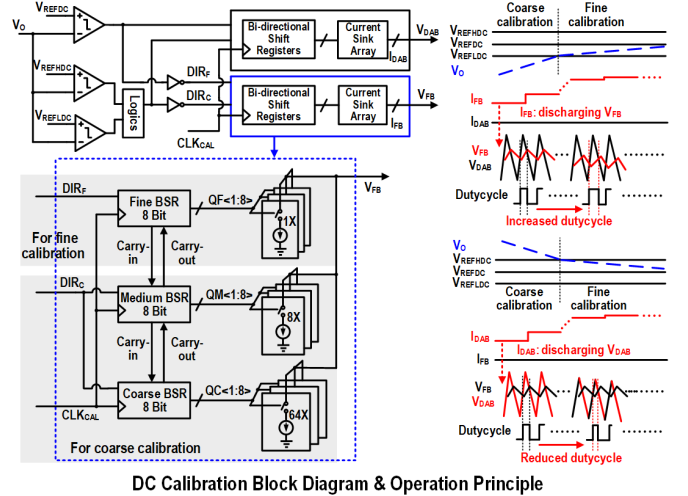


Fig. 8. Block diagram and operation principle of the proposed digital  $V_O$  DC calibration.

is the same, thus making the converter easily extendable to adapt more phases for modularized design with minimum complexity overhead.

### B. Global DC Calibration

The block diagram and operation principle of the digital DC output voltage ( $V_O$ ) is shown in Fig. 8. A dead-zone window is set between  $V_{REFHDC}$  and  $V_{REFLDC}$  for DC calibration. When the output voltage is beyond this predefined dead zone, the “coarse calibration” is activated to rapidly reduce the DC offset. When the output enters the dead zone, the “fine

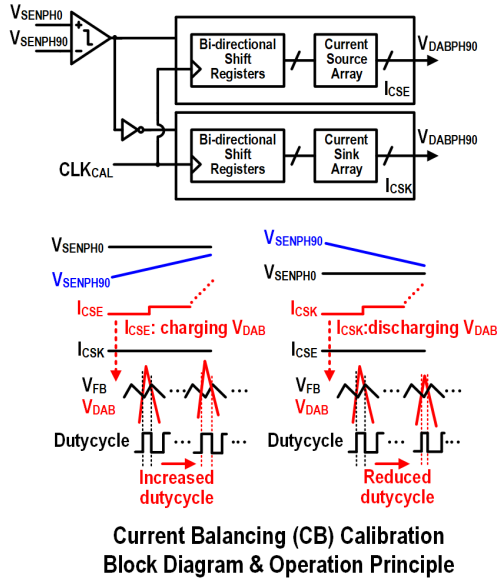


Fig. 9. Simplified diagram and operation principle of the proposed digital current balancing (CB) calibration.

calibration” takes over to tune the DC offset with higher precision. The actual  $D$  of switching node is determined by the intersection of  $V_{DAB}$  and  $V_{FB}$ . By adjusting the charging/discharging of  $V_{DAB}$  or  $V_{FB}$ , the intersection points can be changed, thereby adjusting  $D$  to compensate the DC error. The current for charging/discharging  $V_{DAB}/V_{FB}$  is digitally adjusted with discrete current sink array. As shown in Fig. 8, bidirectional shift registers (BSRs) are designed to control the current sink array. Three comparators are used to detect the DC level of the output voltage and determine the shift direction of the output codes of the BSRs. The BSRs are designed to include 3-bit fine, 3-bit medium, and 3-bit coarse segment with carrying in/out operations [26]. With the designed three segments, the DC calibration can cover a wide range (by the medium and coarse BSRs) as well as maintain fine resolution (by the BSRs). The DC calibration range is estimated by covering the DC error caused by delay obtained with the model described in Section II, with extra margin to further cover other factors that can also affect DC accuracy, such as DCR of inductors. When DC calibration operates,  $D$  is increased by discharging  $V_{FB}$  and decreased by discharging  $V_{DAB}$  separately. With the BSR control, limit-cycle-oscillation (LCO) appears when the controller operates with fine calibration. To fix this issue, freeze mode is introduced to stop calibration when the output enters the dead zone after 64 cycles of the external calibration clock, which is much slower than the switching frequency to avoid conflict with the main control loop.

### C. Local Current Balancing (CB) Calibration

To address imbalanced current issue in multi-phase converters, current balancing calibration is introduced in this design. Fig. 9 describes the system diagram and operation principle of the proposed CB calibration. The  $R_S C_S$  in each phase only contains AC information of the inductor current. To obtain average/DC information, for each phase, a current

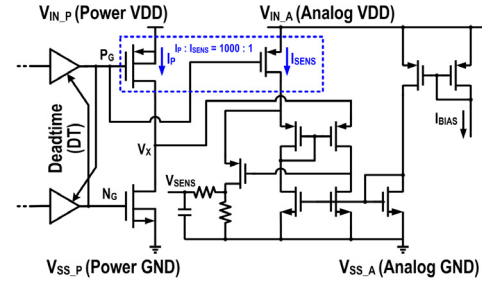


Fig. 10. PMOS average current sensor for CB and APC control.

sensor is designed to sense the high-side power PMOS current, as shown in Fig. 10. The sensed voltage of phase  $0^\circ$ , referred to as  $V_{SENPH0}$ , serves as the reference voltage for CB calibration. By comparing the sensed voltage of the other three phases ( $V_{SENPH90}$ ,  $V_{SENPH180}$ , and  $V_{SENPH270}$ ), the corresponding local CB calibration controller operates to maintain the current in this phase relatively equal to the current in phase  $0^\circ$ . The CB calibration process is also based on BSRs control to charge/discharge the corresponding hysteretic boundary. Take the CB calibration for phase  $90^\circ$  as an example, if the sensed voltage  $V_{SENPH90}$  is larger than the sensed voltage  $V_{SENPH0}$ , it indicates that the current in this phase is higher than the current in the reference phase (phase  $0^\circ$ ).  $V_{DAB}$  in this phase is discharged by  $I_{CSK}$  to decrease  $D$  or average current reduction in this phase. If  $V_{SENPH90}$  is smaller than  $V_{SENPH0}$ ,  $V_{DAB}$  is charged by  $I_{CSE}$  to increase the  $D$ . For the current sink and current source, they are designed not to conduct at the same time. For the current sensor, it is specifically designed with sufficiently bandwidth to track the current flowing through the high-side PMOS, even under the condition when the converter operates with high switching frequency and short high-side turn-on time, e.g., for 0.6-V output voltage with 25-MHz switching frequency. With CB calibration, the current in sub-phases is regulated to that of the reference phase. Thus, the absolute accuracy of the current sensor becomes less critical, while the relative matching between the sub-phases is more significant.

### D. APC Calibration

APC control is developed to maintain the activation of  $1\times$ ,  $2\times$ , or  $4\times$  phases according to the loading condition. Fig. 11 shows the operation principle of the APC controller with different load-current change scenarios. Two reference voltages,  $V_{REFHAPC}$  and  $V_{REFLAPC}$ , are predefined to decide the phase count adjustment process. The phase  $0^\circ$  is always kept active.  $V_{SENPH0}$  is compared with  $V_{REFHAPC}$  to decide the increasement of the active phase number. Under light-load conditions when  $V_{SENPH0}$  is smaller than  $V_{REFHAPC}$ , only phase  $0^\circ$  is activated. If the load current increases such that  $V_{SENPH0}$  rises above  $V_{REFHAPC}$ , then phase  $180^\circ$  will be turned on. With one more phase activated, current in phase  $0^\circ$  may decrease if the loading does not reach a heavy load rapidly. If  $V_{SENPH0}$  drops below  $V_{REFHAPC}$  again, which indicates that the load current is still in the two-active-phase range, phase  $90^\circ/270^\circ$  will not be activated at this time. With further increasement

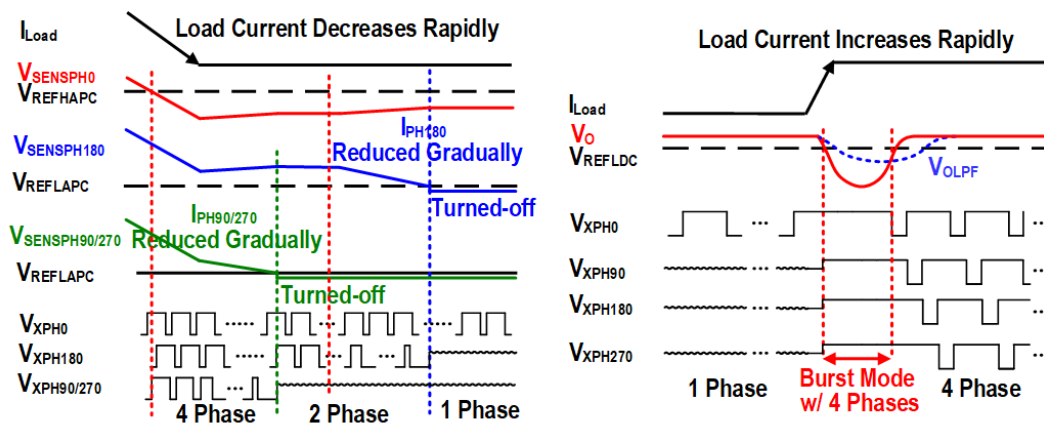


Fig. 11. Operation principle of the proposed APC control.

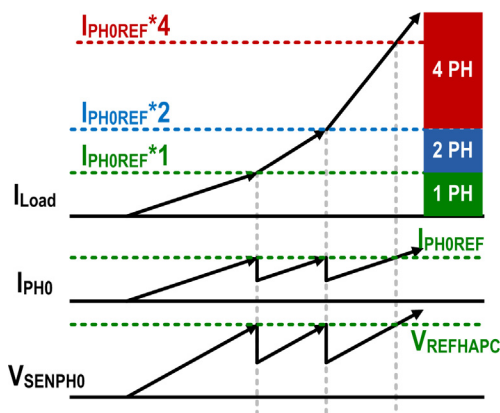


Fig. 12. Illustration of the number of active phases enabled by current sensors with increased loading.

of the load current, when  $V_{SENPH0}$  touches  $V_{REFHAPC}$  again, phase  $90^\circ/270^\circ$  will be activated for the full-four phase operation. On the contrary, when the load current decreases slowly, if  $V_{SENPH0}$  is still larger than  $V_{REFHAPC}$ , the converter maintains its current number of active phases. If  $V_{SENPH0}$  is smaller than  $V_{REFHAPC}$ , the system will first turn off phase  $90^\circ/270^\circ$ . If  $V_{SENPH0}$  is still lower than  $V_{REFHAPC}$  due to rapid current change directly to light load, after a preset settling period threshold of 64 cycles of the calibration clock, phase  $180^\circ$  will also be turned off. If the load current decreases slowly and is still located in the two-active-phase region, the phase  $180^\circ$  will be active until  $V_{SENPH0}$  drops below  $V_{REFHAPC}$  again. To avoid significant voltage fluctuation when turning off phases, the APC operation will proceed smoothly by the local APC controller. For the phase to be turned off, its  $D$  is reduced gradually, so that current in this phase is handed over to the other remained active phases. When  $D$  of the corresponding phase is reduced, the voltage sensed by the current sensor also decreases. Once this sensed voltage drops below a preset threshold voltage  $V_{REFLAPC}$ , the current remaining in this phase is small enough and this phase will be fully turned off without causing a large voltage droop. When turning off the phases during the APC control, the current in one phase is decreased gradually while increased in the other phases. This creates an

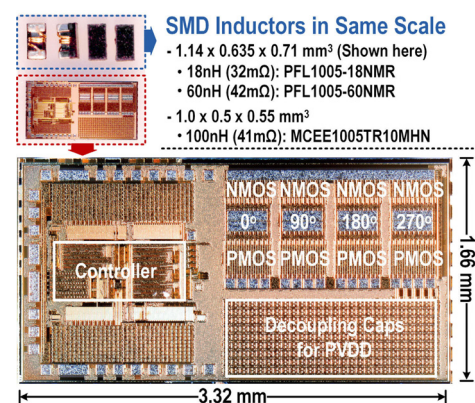


Fig. 13. Chip photograph with 0402 miniature SMD power inductors in the same scale.

imbalanced current, and to avoid conflicts with CB calibration, the CB calibration is designed to proceed only after the APC operation is finished.

Because the amplitude of  $V_{DAB}$  is set larger than  $V_{FB}$  with the  $4 \times RC$  ratio to address the frequency corruption issue, the AC coupling impact will be weakened compared to the original DAB control in [19]. So, the DAB control alone in this work will be slower than the original DAB control as a tradeoff for ensured fixed-frequency operation at higher switching frequency. Also, the low-passed average current sensor would be relatively slow to respond to a large current step to fully utilize the four-phase slew rate. Considering a fast up transient, as shown in Fig. 12, if the activation of the sub-phases is determined by the current sensor, its limited bandwidth will be too slow to react to a sudden voltage droop on the output. To improve uptransient response, as shown in Fig. 11, a burst-mode (BM) operation is introduced to achieve fast asynchronous response with 100% duty cycle and four-phase activation to maximize the slew-rate once BM is triggered when the output drops below the BM threshold. The BM will be disabled once the output starts to recover, indicating that the current in the inductors is larger than the load current at the new steady state. This is achieved by comparing the

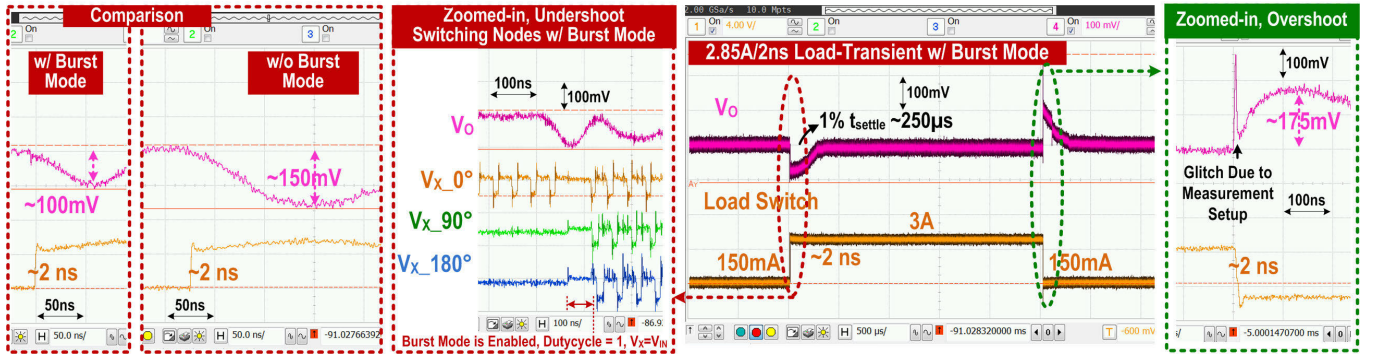


Fig. 14. Measured transient performance and comparison between with and without burst mode.

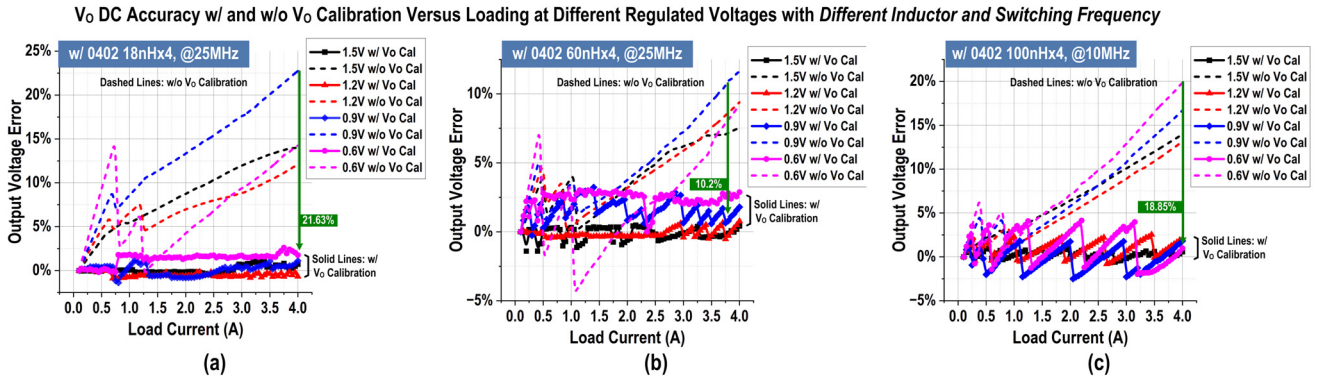


Fig. 15. Measured output DC accuracy with and without the proposed DC calibration, with (a) 18-nH inductor and 25-MHz switching frequency, (b) 60-nH inductor and 25-MHz switching frequency, and (c) 100-nH inductor and 10-MHz switching frequency.

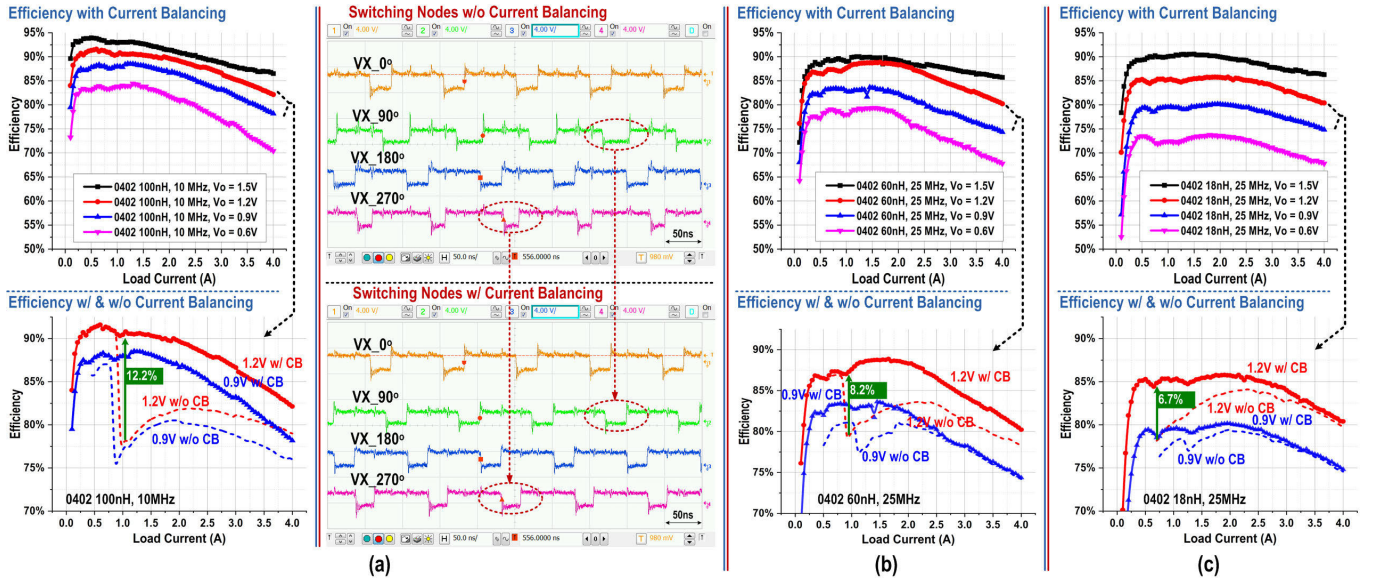


Fig. 16. (a) Measured efficiency versus load current at different output voltages and VX waveforms, with comparison between with and without CB, using 100-nH inductors switching at 10MHz. Measured efficiency versus load current using (b) 60-nH and (c) 18-nH inductors switching at 25 MHz.

output voltage with a delayed (low-pass filtered) version of itself, representing a “previous output voltage signal.”

#### IV. MEASUREMENT RESULTS

The proposed converter has been fabricated in 180-nm CMOS process and measured at 10- and 25-MHz switching frequency with 18-, 60-, and 100-nH 0402 inductors

for potential in-package integration. Fig. 13 shows the chip photograph with 0402 miniature SMD inductors in the same scale, showcasing that the size of the four inductors combined is still smaller than the chip itself. The measured transient response results are shown in Fig. 14. For a load uptransient with 2.85 A/2 ns step, without BM operation, the measured voltage droop is 150 mV. With BM, the measured droop is

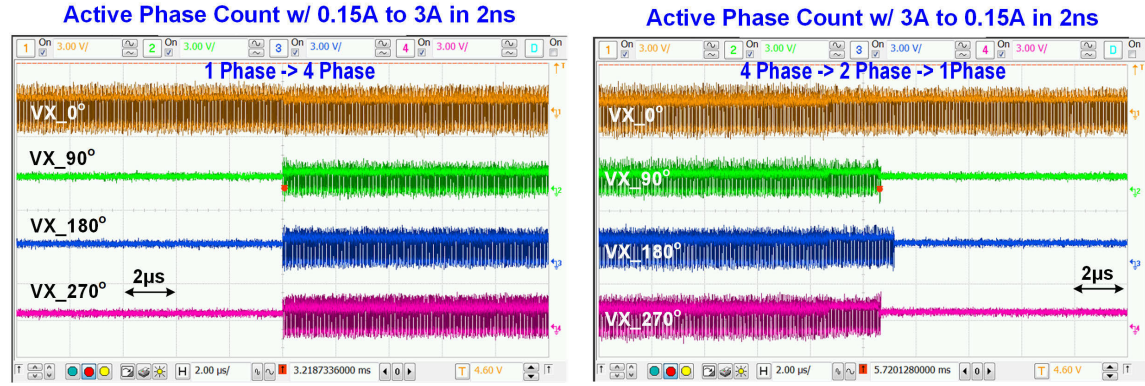


Fig. 17. Measured switching node waveforms for APC control verification.

TABLE I  
COMPARISON WITH THE STATE-OF-THE-ART DESIGNS

|                                   | ISSCC'14<br>[3]        | ISSCC'14<br>[16]         | JSSC'15<br>[5]           | ISSCC'17<br>[15]       | ISSCC'17<br>[20]          | ISSCC'19<br>[4]       | JSSC'21<br>[19]       | This work                  |       |       |
|-----------------------------------|------------------------|--------------------------|--------------------------|------------------------|---------------------------|-----------------------|-----------------------|----------------------------|-------|-------|
| Technology                        | 180nm                  | 250nm                    | 65m                      | 350nm                  | 130nm                     | 28nm                  | 180nm                 | 180nm                      |       |       |
| Control                           | CM<br>Hysteretic       | CM<br>Hysteretic         | PWM                      | CM<br>Hysteretic       | VM<br>Hybrid              | Digital<br>AOT        | CM<br>Hysteretic      | CM<br>Hysteretic           |       |       |
| # of Phase                        | 4                      | 3                        | 4                        | 4                      | 1                         | 4                     | 1                     | 4                          |       |       |
| $V_{IN}$                          | 3.3V                   | 2.8-5.5V                 | 1.8V                     | 3.3V                   | 3.3                       | 1.2V                  | 3-5V                  | 1.8V                       |       |       |
| $V_O$                             | 0.7-2.5V               | 0.2-3.3V                 | 0.6-1.5V                 | 0.3-2.6V               | 1.8                       | 0.6-1V                | 0.5-2.5V              | 0.6-1.5V                   |       |       |
| Ind.                              | 78nH                   | 2.2μH                    | 90nH                     | 200nH                  | 90nH                      | 15nH                  | 200nH                 | 18nH                       | 60nH  | 100nH |
| Ind. Size                         | N.A.                   | N.A.                     | N.A.                     | N.A.                   | N.A.                      | N.A.                  | N.A.                  | 0.51 mm <sup>3</sup> x 4   |       |       |
| Output Cap.                       | 0.94μF                 | 66μF                     | 470nF                    | 2.5μF                  | 0.94μF                    | 0.2μF                 | 2μF                   | 1.2μF                      | 1.2μF | 2.0μF |
| Switching Frequency               | 40MHz                  | 500kHz                   | 30-70MHz                 | 25MHz                  | 30MHz                     | 75MHz                 | 10MHz                 | 25MHz                      | 25MHz | 10MHz |
| Peak Eff.                         | 86.1%                  | 90.2%                    | 87%                      | 88.1%                  | 90.7%                     | 89%                   | 91%                   | 90.6%                      | 90.0% | 93.9% |
| RC & L/DCR Matching Requirement** | High                   | High                     | Low                      | High                   | No                        | No                    | High                  | Low                        |       |       |
| Active Phase Count                | No                     | Yes                      | Yes                      | Yes                    | N.S.***                   | Yes                   | N.S.***               | Yes                        |       |       |
| Current Balance                   | No                     | No                       | No                       | No                     | N.S.***                   | No                    | N.S.***               | Yes                        |       |       |
| $V_O$ Droop (%)                   | 117.6mV<br>(9.8%@1.2V) | 40.5mV<br>(2.7%@1.5V)    | 90mV<br>(9%@1V)          | 102.4mV<br>(6.4%@0.9V) | 36mV<br>(2%@1.8V)         | 80mV<br>(8.9%@0.9V)   | 31mV<br>(2%@1.6V)     | 100mV*<br>(8.3%@1.2V)      |       |       |
| @Current Step (Current Slope)     | @5A/5ns<br>(1A/ns)     | @8A/20μs<br>(0.0004A/ns) | @0.4A/10ns<br>(0.04A/ns) | @4A/5ns<br>(0.8A/ns)   | @1.25A/2ns<br>(0.625A/ns) | @1A/10ns<br>(0.1A/ns) | @1A/3ns<br>(0.33A/ns) | @2.85A/2ns*<br>(1.425A/ns) |       |       |
| Max. Load Current                 | 6A                     | 9A                       | 0.8A                     | 6A                     | 1.25A                     | 1.2A                  | 1A                    | 4A                         |       |       |

\* With 18-nH SMD Inductors. \*\*Including the Matching of RC Pairs and RC &amp; L/DCR. \*\*\*Means not Suitable for the Single-Phase

reduced to 100 mV, which is reduced by 33.3%. The long 1% settling time of 250  $\mu$ s is mainly caused by the DC calibration. The 2.85-A load current difference between the two transient steps creates a significant IR drop difference across the DCR of the miniature power inductors and the bonding/routing resistance, which creates a relatively large DC error difference that needs more calibration cycles to correct, and in this work, a slower calibration clock was implemented. On the other hand, in this work, we mainly focused on the response time (by the DAB and BM control) to suppress voltage droops rather than on the settling time, because in most applications, it is the droops that matter the most. If a load circuit could survive the minimum voltage of the droop, when the voltage starts to recover, it could survive the recovery during the settling period. If settling time needs to be reduced in an application, a faster calibration clock could be used to speed up the DC calibration process. Fig. 15 demonstrates the

measured steady-state DC accuracy of the output when the DC calibration is enabled and disabled. With the DC calibration, improved DC accuracy is achieved. An enhancement of 21.63%, 10.2%, and 18.85% is observed for the heavy loading condition with different inductors. Furthermore, the DC error with 1.8–1.2-V conversion for all inductors remains within 2.5% across the full-loading range with different voltages, indicating a load regulation comparable to designs employing linear control with a high-gain error amplifier. Fig. 16 depicts the measured power efficiency performance. With different load currents and output voltages when the converter operates at 10/25 MHz with different inductors, the measured peak efficiency is 90.6%, 90%, and 93.9% with 18-, 60-, and 100-nH inductors, respectively. A comparison of efficiency with and without CB calibration reveals up to 12.2% improvement, which also highlights the significances of current balancing. The waveforms of the switching node VX are also measured

to validate the functionality of the proposed CB calibration. As shown in Fig. 16(a), better VX duty-cycle matching is observed with the CB calibration. Also, the VX waveforms for APC operation are presented in Fig. 17. During an uptransient, all four phases are activated by the BM. When the load current steps down to the light load, the converter operates from four phases to two phases and to one phase.

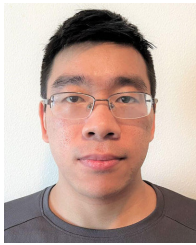
Table I summarizes the performance of the proposed converter. Compared with the state-of-the-art designs, this converter relaxes the matching and accuracy requirements of the RCs, inductance, and DCR of inductors, thus has more flexible requirement and choices for the power inductors and the switching frequency. The designed converter also achieves higher efficiency and can handle faster load current steps, using 0402 inductors for potential in-package integration.

## V. CONCLUSION

This article introduces a four-phase fixed-frequency current-mode hysteretic DC–DC converter that offers flexibility in selecting power inductors and switching frequency. Fixed frequency operation is ensured at a higher switching frequency by the ratioed RC networks without using the reset mechanism for DC error correction. To regulate the output voltage, an intrinsic DC path in DAB controller is introduced, and DC error is further corrected by the digital DC calibration to address the circuit delay-related issues and relax the requirement for precise matching of the RC, inductance, and DCR of the power inductors. Additionally, digital current balancing calibration and APC control are also designed to maintain high efficiency over a wide range of loading, with BM to reduce the voltage droop at fast and large current steps. The converter is verified with small form-factor 0402 power inductors for in-package integration or to achieve a higher current/power density.

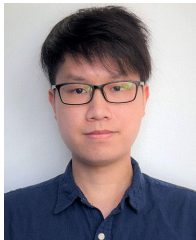
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**Lei Zhao** (Student Member, IEEE) received the B.E. degree in the electronic science and technology from the Harbin Institute of Technology, Harbin, China, in 2016, and the M.Sc. degree in electrical and computer engineering from the University of Macau, Macau, China, in 2019. He is currently pursuing the Ph.D. degree with the Electrical and Computer Engineering Department, Iowa State University, Ames, IA, USA.

He worked as a summer intern with MediaTek, Woburn, MA, USA, in 2023. His research interests include different types of power management and analog IC designs.



**Junyao Tang** (Student Member, IEEE) received the B.Eng. degree in electronic and electrical engineering from the Southern University of Science and Technology, Shenzhen, China, in 2018, and the Ph.D. degree in electrical and computer engineering from the Iowa State University, Ames, IA, USA, in 2023.

He worked as a summer intern with Skyworks, Austin, TX, USA, in 2022. He will be joining Halo Electronics, Dallas, TX, USA, in 2023. His current research interests include analog, mixed signal, and

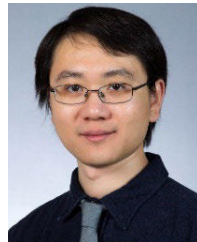
power management IC designs.

Dr. Tang received the College Research Excellent Award in 2023.



**Kang Wei** (Member, IEEE) received the B.E. degree in microelectronics from Northwestern Polytechnical University, Xi'an, China, in 2011, and the Ph.D. degree in electrical engineering from the University of Texas at Dallas, Richardson, TX, USA, in 2021.

From 2011 to 2013, he worked as a Research Assistant with Sun Yat-sen University, Guangzhou, China, focusing on the design of analog circuits and system for lock-in amplifier. He joined Texas Instruments, Dallas, TX, USA, in 2016 and 2017, respectively, as an Analog Design Intern, working on highly efficient point-to-load power IC design. Since 2021, he has been an Analog Design Engineer with Kilby Labs, Texas Instruments, where he is currently developing high-voltage gate drivers, galvanic isolation solutions, and ultralow-cost linear regulators for automotive, industrial, and consumer power systems.



**Cheng Huang** (Member, IEEE) received the B.Eng. degree from Zhejiang University, Hangzhou, China, in 2008, and the Ph.D. degree from the Hong Kong University of Science and Technology, Hong Kong, China, in 2014.

From 2014 to 2015, he was with the Department of Electronics and Electrical Engineering, Keio University, Yokohama, Japan. From 2016 to 2017, he was with Broadcom Ltd., San Jose, CA, USA, as an Analog and Power IC Design Engineer. In 2018, he joined the Department of Electrical and Computing Engineering, Iowa State University, Ames, IA, USA, where he is currently a Harpole-Pentair Assistant Professor. His work focuses on different types of power management integrated circuits, including high-frequency and fully integrated switching converters, single-inductor multiple-output switching converters, wireless power transfer systems, isolated DC–DC converters, GaN drivers, and GaN-based power electronics.

Dr. Huang has been serving as an Associate Editor for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS PART II: EXPRESS BRIEFS since 2020, as a Guest Editor of IEEE SOLID-STATE CIRCUITS LETTERS in 2023, as a TPC member in CICC, and as a TPC member in the ASP sub-committee for the IEEE CAS society. He also served as a Track Chair of ISCAS 2022 and MWSCAS 2021.