A 96.1% Efficiency Single-Inductor Multiple-Output (SIMO) Buck Converter With 2.1-A/ns Transient Speed and 2.2-A Maximum Current Capacity

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***Abstract*— To overcome the limitations of transient handling capability, current capacity, power efficiency, and current density in existing single-inductor multiple-output (SIMO) converters, this article presents: 1) loop response enhancement by the fully comparator-based "Buffet-Like" dual-sampling non-linear control; 2) voltage droop suppression by the hybrid digital LDO (HLDO) attached to each output; 3) efficiency enhancement by frequency hopping and bootstrapped N-type MOSFET (NMOS) output switches; and 4) the power density enhancement with a smaller than the chip power inductor. The prototype with two outputs achieves a transient handling capability of 2.1 A/ns, which is a significant advancement over the state of the art. A maximum current capacity of 2.2 A, and a peak efficiency of 96.1% are also measured using a 0806 miniature power inductor.**

***Index Terms*— Bootstrap driver, digital LDO, efficiency, hybrid, inductor current control, load transient steps, non-linear control, power density, single-inductor multiple-output (SIMO), undershoot.**

I. Introduction

MULTIPLE voltage rails are generally required in processors, SoCs, and SiPs for different blocks, e.g., cores, cashes, and I/Os [1]. Each rail requires an individual switcher with a bulky and expensive power inductor, resulting in increment of materials and dominating system footprint and cost. Single-inductor multiple-output (SIMO) converter, introduced in the early 2000s [2], is a promising solution to deliver multiple rails using one inductor for smaller form-factor system designs. However, it is still striving to come to fruition with a primary obstacle of its limited current capacity and transient handling capability. As illustrated in Fig. 1(a), the SIMO converter regulates different output channels by alternatively selecting the switches M_1 and M_2. To respond to load variation in any of the outputs, the total energy stored in the inductor as well as the energy distributed among the outputs are adjusted. Thus, with current discretely delivered to the outputs, voltage fluctuations known as self- and cross-regulations, will be introduced by the load transient events at the same output or at the other outputs, respectively [2], [3], [4], [5], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20].

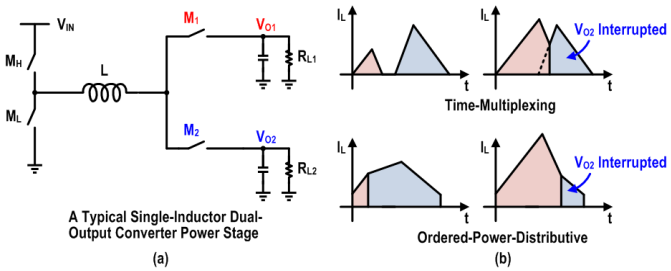

Fig. 1. Illustration of (a) conceptional structure of an SIMO converter and (b) voltage interruption happening on one output.

Typically, there are two popular control schemes for SIMO converters, i.e., time-multiplexing control (TMC) [2], [3], [4], [5], [7], [8] and ordered power distributive control (OPDC) [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], with a simplified output power distribution process, as shown in Fig. 1(b). In the TMC scheme, the duty cycle of each output is modulated in a time-multiplexed manner, with the inductor current at discontinuous conduction mode (DCM). Each output operates for a certain period before switching to the next output. The duty cycle of each output is adjusted to achieve the desired voltage regulation for the selected output. It can provide isolation between the inductor current for different outputs; however, only at light loading conditions. When the load condition becomes heavier, such that the inductor current collides, crosstalk will occur, thus the current and power capacity are limited. Pseudo continuous-conduction mode [2] increases the current capacity by raising the baseline average current level to ensure each output can be provided with sufficient energy at the selection period. However, the power efficiency will be degraded with a large amount of current

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free wheeling in the inductor for a long period in every cycle. On the other hand, the OPDC scheme can regulate all the outputs as a group within one inductor charge/discharge cycle. It operates in continuous conduction mode (CCM) and supports a larger power capacity and reduces output voltage ripples compared with TMC; thus, it is much popularly used in the existing SIMO converter designs. However, it requires precise control over the timing and sequencing of the output switches, and crosstalk always exists because the inductor current is continuous and shared. Especially, if the outputs are selected in a fixed order, when significant load change occurs in the higher priority output, the inductor current distributed to the other output will be immediately interrupted and result in significant cross-regulation, especially at heavier loading conditions.

If the voltage regulation loops are fast enough to correct voltage errors, voltage fluctuations caused by both self- and cross-regulation can be minimized. In previous SIMO converters, either with TMC or OPDC, almost all of them adopt linear control [2], [3], [4], [5], [7], [9], [10], [11], [12], [13], [14], [15], [16]. However, linear control has small-signal bandwidth limitation and is especially challenging to optimize in SIMO converters due to multiple dependent loops, which is further compromised by ensuring stability with process, voltage, and temperature (PVT) and component variations at different loading conditions. Because of these limitations, state-of-the-art SIMO converters [2], [3], [4], [5], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20] can only handle small current changes (typically 10–300 mA) in a slow step (typically in microseconds).

Hybrid topology with parallel fast linear regulators was used in [6] and [13]; however, the maximum current steps were still limited to 90 mA due to the limited bandwidth.

Compared with linear control, fully comparator-based nonlinear control (such as hysteretic control or constant on/off time control) eliminates the small-signal bandwidth and stability concerns, and thus can significantly enhance the dynamic response. However, compared with traditional buck converters that only have inductor charge/discharge control (two switches) and a duty-cycle to adjust, SIMO converters have both the inductor charge/discharge control and the output rotation control, with at least four switches (for two outputs) with dependency that make it less intuitive and more challenging to operate with non-linear control. Thus, to the best of the authors' knowledge, fully comparator-based nonlinear control is only achieved in [17], but with a freewheel period introduced to store the energy when both outputs are not selected to realize voltage-mode hysteretic control. With the freewheel period, the inductor current in [17] was much larger than needed, significantly compromising its efficiency to be peaked at only 73%, while the maximum current step was still limited to 100 mA. Reference [18] is comparator-based but still relied on an analog loop with phase-locked loop (PLL) to correct errors, and the maximum current steps were limited to 250 mA.

In addition to the current transient handling capability, the power efficiency of an SIMO converter is also limited. As the exact opposite of a multiphase single-output buck converter, currents of all outputs share one inductor in an SIMO converter. The conduction loss caused by inductor DCR becomes much more significant. With more switches for output rotation, SIMO converters also have higher switching and conduction loss, which further limits the efficiency and current capability. A bulkier inductor with lower DCR was typically used to maintain a decent efficiency. This makes SIMO converters less attractive even from the "single-inductor" aspect (one much larger inductor versus multiple smaller ones).

To overcome the above-mentioned limitations, this article proposes a fully comparator-based controlled SIMO converter, with a new "Buffet-Like" non-linear control as the core scheme and a hybrid digital LDO (HLDO) assistance outside the loop to significantly improve the load transient handling capability and current capacity, while maintaining high-power efficiency performance with additional efficiency optimization techniques even using a miniature power inductor.

II. Proposed Architecture and Key Techniques

To help better understand the proposed control scheme, Fig. 2 illustrates different control methods used in SIMO converters with a daily scenario as an analogy. In this analogy, the food is the current/charge, the customers are the loads on the outputs consuming the food, the chef is the inductor charge controller and the power stage distributing the food.

1) *TMC (Fig. 2, Top):* At steady state, the chef will pick just enough food first for customer 1; then pick just enough food for customer 2. Because each needs to complete an entire inductor charge/discharge cycle, the blank-service period (when serving customer 1, customer 2 needs to wait) is relatively long. When a load transient happens to, say customer 2, while customer 1 is being served, customer 2 will need to wait the entire blank-service period for the chef to serve it. And even when it is customer 2's turn, in order not to disturb customer 1, it cannot fully utilize the switching period to maximize the slew rate. And, it will take multiple cycles for the correction due to system bandwidth limitations. This may not cause cross-regulation, but self-regulation (voltage droops at the output having transients) will be larger, especially with larger current steps.
2) *OPDC (Fig. 2, Middle):* At steady state, the chef will pick just enough food for both customers combined, then deliver the food in order. When load transient happens, causing not enough food, cross-regulation occurs. The chef will pick more food in the next cycle; however, due to insufficient food in the previous cycle, outputs dropped and stored energy in the capacitors are consumed, and more charges than needed at the new steady state will be required to compensate the lost charges on the output capacitors. This will need multiple cycles to eventually correct the errors, depending on the system bandwidth which is compromised by stability concerns caused by the dependent multiple loops and PVT/component/loading variations, hence a much longer error correction period. During this process, both cross- and self-regulation will be introduced to all outputs,

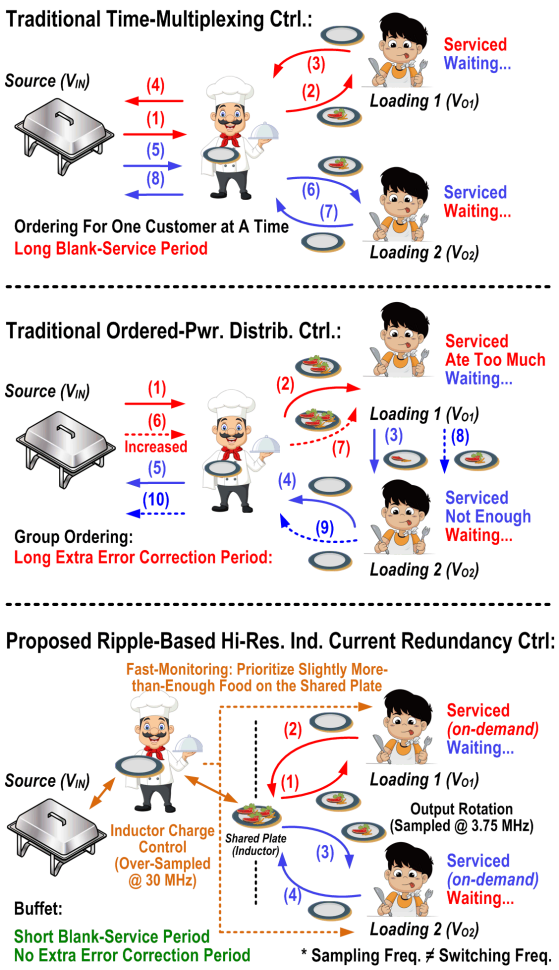

Fig. 2. Conceptual illustration of the traditional TMC and OPDC and the proposed "Buffet-Like" non-linear control for SIMO converters.

which cause unwanted voltage fluctuations and becomes much worse at larger and faster current steps or with heavier loading.

3) *Proposed "Buffet-Like" Control Scheme (Fig. 2, Bottom):* Different from traditional TMC or OPDC, the proposed control decouples the inductor charge/discharge control and the output rotation control, with two different sampling frequencies (not switching frequencies). By monitoring both customers at an over-sampled frequency (30 MHz), the chef ensures that there is always slightly more than enough food on the plate (inductor), but not too much to cause significant efficiency degradation or requiring a free-wheeling period. Then based on the needs from the outputs, the two customers will negotiate at a lower sampling frequency (3.75 MHz) to take turns to pick up their food. When a load transient happens to either output, the chef will notice immediately due to the faster sampling frequency, and immediately charge the inductor at its maximum slew rate, which means sufficient (even excessive) food can be obtained quickly. In the meantime, the output who drops below its reference will be given full priority to be charged until above its reference, then switch

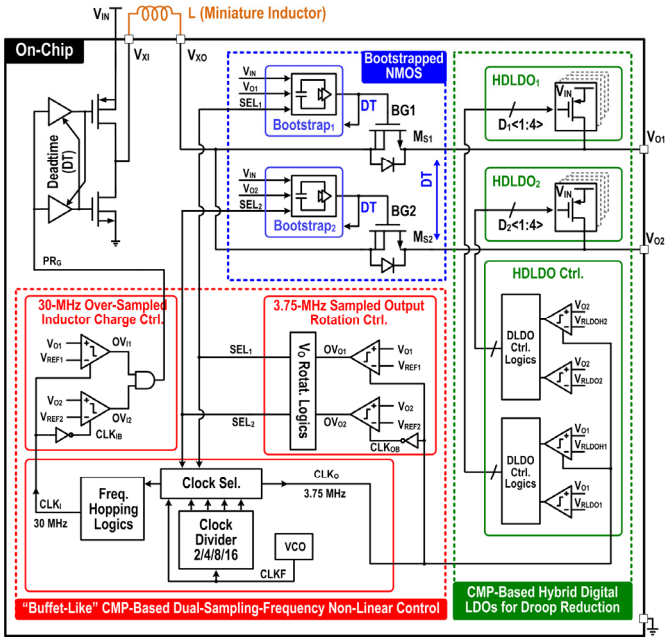

Fig. 3. System block diagram of the proposed SIMO converter.

to the other output. Although cross-regulation may be introduced to the output that does not have a transient, the actual droops will become smaller because: 1) the inductor is being charged with 100% duty cycle and 2) the outputs shared the impacts and balanced the droops, and in the end, it is how much voltage droop really matters, either caused by cross- or self-regulation. These decision-making processes are solely comparator-based, which means that there are neither small-signal limitations nor stability concerns.

4) *Proposed HDLDOs:* Although the inductor can be charged at full slew rate, it is still limited by its inductance as a large-signal limitation. To address this limitation, an HDLDO for each output is used to provide an extra current path to clamp the outputs around its references and prevent excessive droops, with smoothing control strategies to exit the hybrid mode without introducing oscillations or multiple triggering.

5) *Additional Proposed Techniques:* To improve power efficiency, frequency hopping is also introduced to reduce the over-sampling frequency when high-resolution is not needed, and N-type MOSFETs (NMOS) are used as the output switches with bootstrap drivers to minimize ON-resistance and extend the output voltage range, with proper deadtime control and body connectivity to ensure reliability.

With the "Buffet-Like" core control loop and the HDLDOs to provide extra clamping, this converter can handle the much larger and faster current steps, measured at 2.1 A/ns. Higher efficiency is also achieved with a smaller volume inductor. The system block diagram is shown in Fig. 3, and the detailed descriptions of the proposed techniques will be provided below.

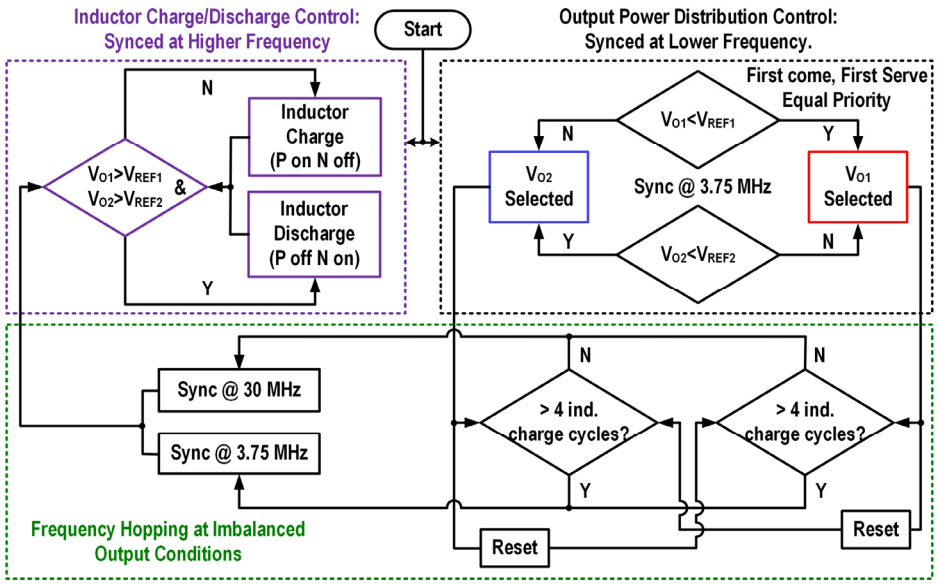

Fig. 4. Operation flowchart of the proposed "Buffet-Like" dual sampling frequency nonlinear control.

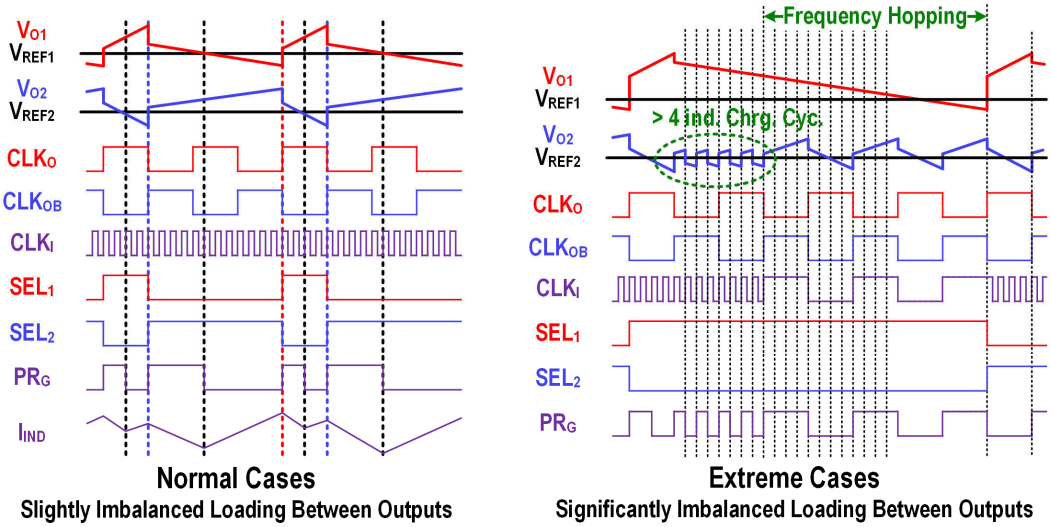

Fig. 5. Operation timing diagram of the proposed "Buffet-Like" control at different loading conditions.

A. Proposed "Buffet-Like" Dual Sampling Frequency Non-Linear Control for Breaking the Small-Signal Limit

Fig. 4 shows the operation flowchart of the proposed comparator-based "Buffet-Like" control. For the over-sampled inductor charge control, the two outputs are monitored at complementary 30-MHz CLK_I and CLK_{IB}, respectively. The inductor will remain in charge mode until V_{O1} and V_{O2} are both detected to be higher than their corresponding reference voltages, indicating that the current in the inductor is more than enough. This 30-MHz over-sampling frequency ensures a higher resolution to maintain a more precise energy in the inductor based on the need to avoid excessive surge (overshoot) or shortage (droop) and minimize the current redundancy for better efficiency; hence, no freewheeling is required. For output rotation control, it is monitored at a lower sampling frequency of 3.75 MHz to achieve a better trade-off between voltage ripples and efficiency based on the targeted maximum loadings. The two outputs are rotated with equal priority to achieve a self-adaptive duration of selection depending on loading conditions. The operation timing diagram with different loading conditions is shown in Fig. 5. In normal cases with no significant load imbalance, the two outputs are served with similar durations. If significant loading imbalance exists, this SIMO converter then behaves like a traditional single-output buck converter.

In extreme cases with significantly imbalanced loadings between output, e.g., when V_{O1} has a much lighter load current than V_{O2}, it maintains higher than V_{REF1} for a longer period where only V_{O2} is selected. The inductor is charged/discharged based on V_{O2} ripples, which introduces unnecessary switching loss due to the 30-MHz sampling. To solve this problem, frequency hopping is introduced based on monitoring the duration of selection of each output. For example, if V_{O1} is not selected more than four cycles of inductor charge control, the

over-sampling for V_{O2} will be reduced to 1/8 (3.75 MHz). It will be reset once V_{O1} is selected again and repeats if necessary.

B. Sampling Frequencies and Switching Frequencies

In this work, the sampling frequencies are not equal to the switching frequencies but have complicated relationships depending on different conditions. The main control loops are output-ripple based. When the multiple outputs touch the predefined boundaries, the power transistors and switching nodes switch to different states, respectively. The switching frequency is directly related to the ripple information of all outputs, the clocked detection whether they are above/below the corresponding boundary, and how the control strategy selects the inductor charging and discharging states and the conduction of V_{O1} and V_{O2}. As a result, the load current of each output, the output capacitors (capacitance and ESR), and the sampling clock frequency can all affect the actual switching frequency. Because of the complex nature of the non-linear control, it is not intuitive to quantitatively derive the relationship between these components. Instead, some qualitative descriptions are provided as follows.

1) Relationship between the over-sampling frequency for inductor charging/discharging and the input stage switching frequency. Intuitively, this sampling frequency limits the resolution of the inductor charging and discharging control, thus the switching frequency of the input stage. If this sampling frequency is too low, the update rate of the output information, which is used for the controller to determine inductor charging and discharging phases, will be limited. This will also place a limit on the switching frequency because the switching of power transistors is synchronized to the sampling frequency. On the other hand, if the sampling frequency is high enough, to an extent that it does not become a bottleneck anymore, then the steady-state input stage switching frequency will have a weaker relationship to the sampling frequency as shown in Fig. 6, but will be dependent on other factors, such as the loading conditions and the ESR of the output capacitor (because the ESR can affect or even dominate the voltage ripple, especially for SIMO converters that the output current is discontinuous). In this work, with the *LC* selections and the output voltage and current ranges, the input-stage switching frequency is maintained within 1–8 MHz or lower.

   On the other hand, having a faster sampling frequency above 20 MHz for the inductor charging/discharging will not increase the switching loss in this case (except for a higher controller loss, but is still minor), but will benefit the transient response by providing a faster monitoring rate so that when a load transient happens, the inductor can be charged with less delay. In the proposed design, a 30 MHz was finally chosen as the sampling frequency for the inductor charging/discharging control.
2) The output rotation sampling frequency, on the other hand, does not directly relate to the input-stage switching frequency, but relates to the output-stage switching frequency, and can be separately optimized. It affects the steady-state output voltage ripples and dynamic transient response. Therefore, this is mainly optimized with the goal of balancing the output-stage switching loss (and the impact on overall system efficiency), transient response, and steady-state voltage ripple. In this work, 3.75 MHz (30 MHz/8) was finally selected.

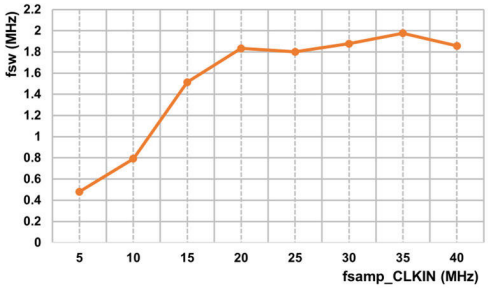

Fig. 6. Simulated input-stage switching frequency versus sampling frequency of the inductor charging/discharging control with all other parameters fixed.

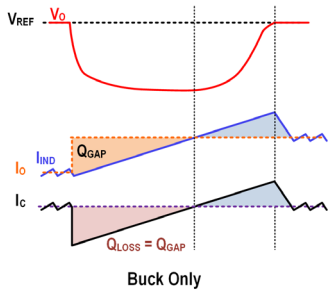

Fig. 7. Illustration for an up-transient response for buck-only.

C. Proposed HDLDO for Breaking the Large-Signal Limit

Although small-signal limitations are relieved by the "Buffet-Like" control scheme of the main voltage regulation loop, large-signal limitations still exist with the limited inductor charging slope when handling transient events. Fig. 7 depicts a simplified response process of a single-output buck converter for load up transients. Even assuming that the inductor can be charged immediately with full thrust after the load transient happens, there is still a large gap (Q_{GAP}) between charges of what the load demanded and what the inductor provided before the output voltage begins to recover. Throughout this time, the output capacitor is being discharged to compensate for this charge gap with a charge loss (Q_{LOSS}) and shows an undershoot voltage at the output.

To limit this voltage droop, in this work, an extra current path per output by an HDLDO is introduced to directly charge the output capacitor, bypassing the inductor. For each HLDO, it is composed of a continuous-time comparator, a discrete-time comparator, a digital controller, and an array of p-type MOSFETs (PMOS) with 4×, 2×, 1×, and 1× sizing. The operation diagram of the proposed HDLDO is illustrated in Fig. 8. A predefined boundary V_{RLDO} is set to be lower than V_{REF}. With a load up-transient happening, if V_O drops below V_{RLDO} and is detected by the continuous-time comparator, the

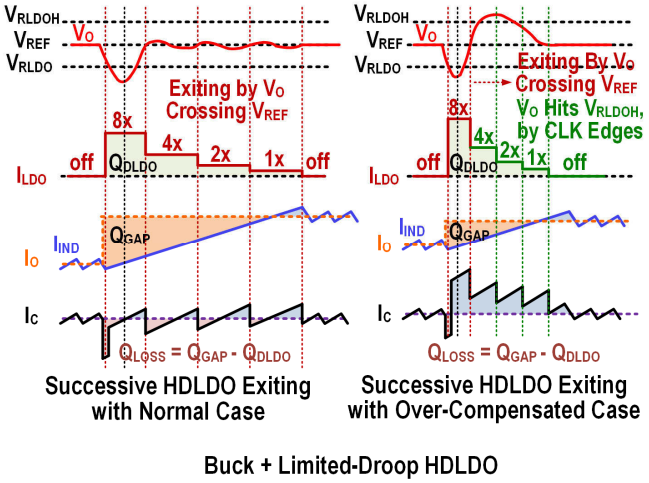

Fig. 8. Illustration of the limited voltage droop with HLDO and the operation timing diagram of the HLDO (shown with a single-output buck for simplicity).

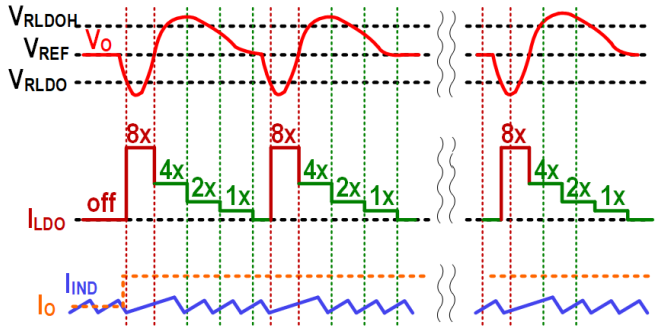

Fig. 9. Possible scenario when the operation is dominated by HDLDO, causing multiple triggering or oscillations.

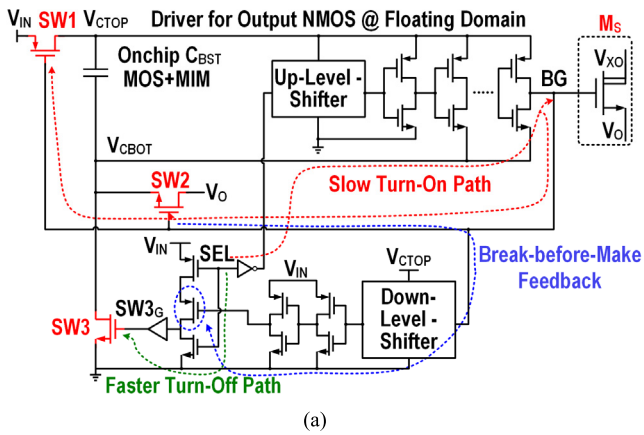

Fig. 10. Detailed circuitry of the bootstrapped output NMOS switch and the deadtime implementation. (a) Circuit diagram for bootstrapped output NMOS. (b) Deadtime for bootstrap capacitor charge and discharge control.

HLDO power switches will be turned on with full strength (with 8× sizing) and be applied to provide instantaneous charge (Q_{LDO}) to the output to suppress the droop and shorten the recovery time. When V_{O} recovers back to V_{REF}, the HLDO will begin to exit. For smooth exiting, the switches will be successively turned off with an order of 8×–4×–2×–1× off strength, with two scenarios described below.

For a fixed maximum size HLDO power switch array, the absolute current strength is related to the difference between the supply and output voltage. With a larger voltage difference, the current strength will be stronger. First, for a normal case, if the strength of the HLDO is not excessively stronger compared with the load steps, the output voltages will recover back as depicted in left of Fig. 8. The exiting process of the HLDO is triggered by V_{O} up-crossing V_{REF} (detected by the corresponding clocked comparator used in the output rotation control). Second, for a significantly over-compensated case, the strength of the HLDO is too strong and provides too much current with 8×, an overshoot may appear. If V_{O} hits V_{RLDOH}, a higher boundary, the HLDO power switches will be turned off by counting $\mathrm{CLK_{O(B)}}$, with each cycle turning off one switch. In addition, the strength of the 4×–2×–1×–1× dose in this work can also be programed with a 2-bit control to cover a wider voltage and loading range for more flexibility, but this function does not need to be adjusted during our measurements with our current specifications.

Because the HLDO loop responds faster than the main control loop, the current provided to output may be dominated by the HLDO. As shown in Fig. 9, the current in the inductor is suppressed by the HLDO and is stuck at a lower level. When turning off the HLDO, the current provided by the inductor to the outputs is not sufficient, thus large droop appears at V_{O} again and even causes multiple triggering of the HLDO or oscillation. To avoid this issue: the inductor remains in charge mode; whenever, the HLDO is triggered until it is fully turned off and 2) once triggered and when the LSB is turned off, a short blank period with 32× $\mathrm{CLK_O}$ period is introduced to the HLDO operation.

D. Proposed Bootstrapped NMOS Output Switches for Efficiency Enhancement

To further reduce the conduction loss on the output current path, the turn-on resistance of the output rotation switch is minimized with bootstrapped NMOS, which provides output-independent V_{GS} to fully turn on the output switches. Fig. 10(a) and (b) shows the detailed circuitry design and operation principle of the proposed bootstrap drivers and control circuits for the 1.8-V DNW NMOS output switches. An on-chip

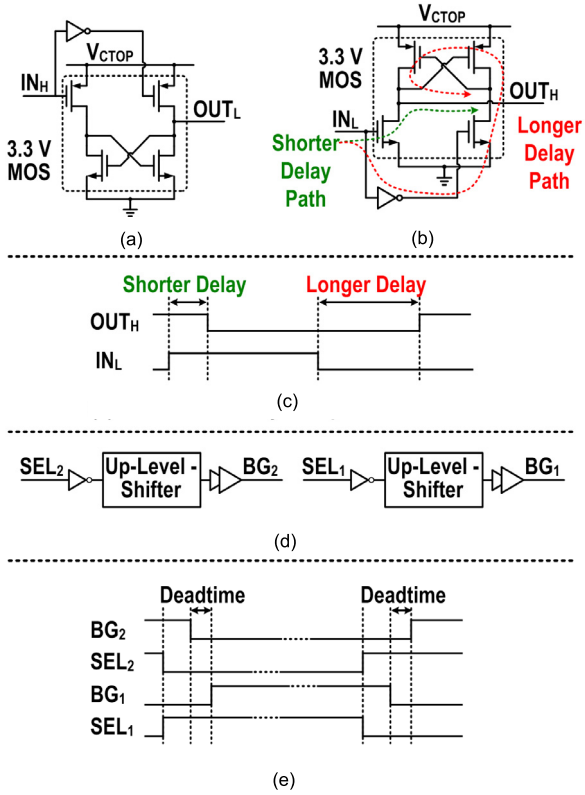

Fig. 11. Deadtime implementation for the output switches. (a) Down-level shifter. (b) Up-level shifter. (c) Imbalanced delay for up-level shifter. (d) Signal path for V_O selection. (e) Deadtime utilizing the imbalanced delay of the up-level shifter.

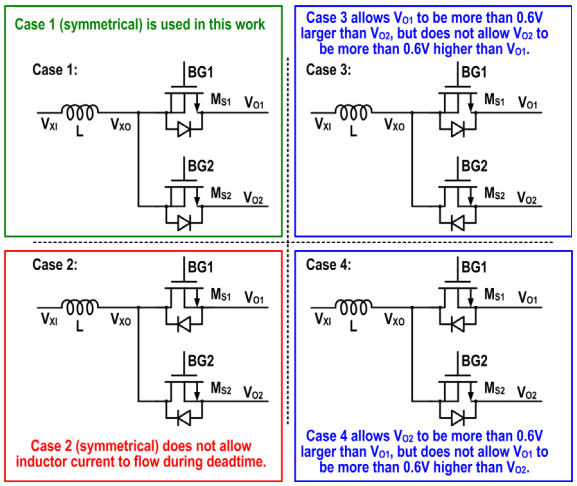

Fig. 12. Possible configurations of the body-diode connectivity for the bootstrapped output rotation switches.

2.16-nF bootstrap capacitor with MOS varactors (1.74 nF) and MIM capacitors (0.42 nF) stacked is integrated for each output as C_{BST1} and C_{BST2}. The SEL signal is provided by the output rotation control to indicate the output selection. When an output is not selected (SEL low and BG low), C_{BST} is charged to the supply (1.8 V) by turning on SW1 and SW3. And when the output is indicated to be selected, SEL becomes high and passes through the up-level shifter to set BG to be high. Thus, SW1 and SW3 will be turned off, and SW2 will be turned on to stack C_{BST} on the top of the output as V_O+ 1.8 V. Ideally, this should provide a 1.8-V V_{GS} to fully turn on the corresponding NMOS. Due to the charge-sharing loss, the actual V_{GS} will be slightly lower. During the design stage, we have ensured an at least 1.7-V V_{GS} can be achieved across different PVT corners with a large enough C_{BST}.

For this bootstrapped operation of the two output switches, there are two deadtime controls that are critical to ensure reliability, one for C_{BST} charge/discharge, and one for the two outputs rotation. First, as shown in Fig. 10, for C_{BST} charge/discharge, SW2 and SW3 are designed to avoid shoot-through when switching their states. When SEL becomes high, SW3 can be turned off with a short delay path and SW2 will be turned on after SEL passes through the up-level shifter and the followed driver chains with a longer delay. Thus, SW2 is ensured to be turned on after SW3 is turned off. When SEL becomes low, a break-before-make feedback path is designed to guarantee SW2 to be turned off before SW3 is turned on. Second, for the deadtime of output rotation, it is achieved by the intrinsic imbalanced delay of level shifters, as shown in Fig. 11. SEL1 and SEL2 (the select signal for the corresponding output from the controller) are exactly complementary. Before controlling the output switches gate, they pass through an up-level shifter with different delay paths of rise and fall times. This intrinsic delay difference (600 ps–1.2 ns at PVT variations) is utilized as the deadtime for the output rotation.

Fig. 12 shows the possible body-diode connections of the output DNW NMOS. Case 2 will not work, as during the deadtime, the inductor current should have a path to continuously flow, while the other three cases do provide possible paths through the body diodes. In this design, Case 1 is selected. Although there is a maximum ~0.6-V difference limitations between the outputs, the circuit/layout complexity is lower, and it is more than enough for the targeted applications. If an application requires the voltage difference between the two outputs to be larger than 0.6 V, the asymmetrical Case 3 or 4 could be used.

Fig. 13 shows the simulated power loss breakdowns for two different loading conditions. For the loading conditions near the peak efficiency point [Fig. 13(a)], the converter is operating at light-to-medium load conditions. In this case, the losses are relatively well balanced, with the conduction losses slightly larger than the switching losses. The frequency hopping in this case can help reducing the switching frequency, thus the switching losses. The controller is relatively power hungry at ~2 mW due to the high-frequency VCO and related circuits, but 16.35% of total loss or 0.82% efficiency loss if projected to the total efficiency calculation is still acceptable.

At heavy load with 1.5-A total current, the conduction losses dominate the power losses. On the other hand, thanks to the bootstrapped output NMOS transistors that are fully turned on, their conduction loss is not very significant. The ON-resistance of the input-stage power PMOS, NMOS, and the output-stage bootstrapped NMOS is simulated to be 26.5, 9.56, and 9.82 mΩ, respectively. The switching-node losses also increase with the increase of the inductor current, mainly due to the higher power losses during the on-off transitions.

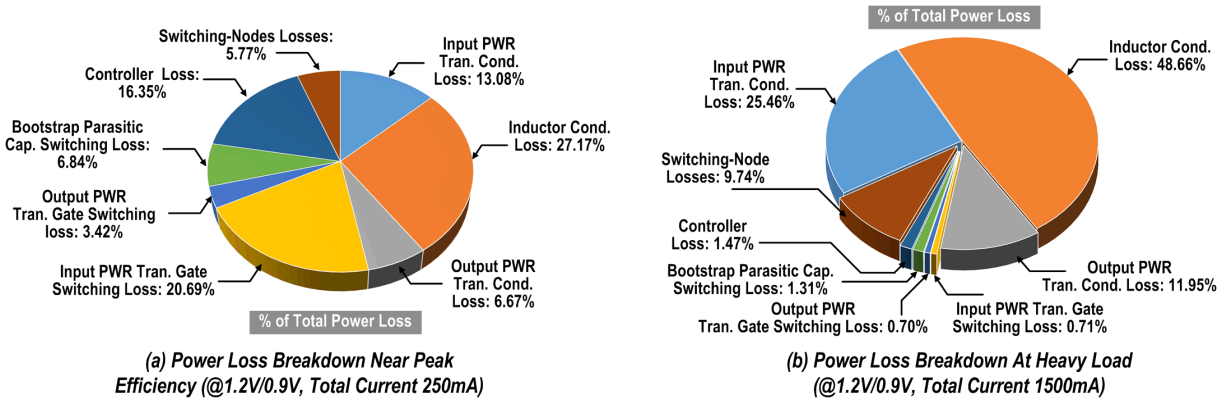

Fig. 13. Simulated power loss breakdown at two different conditions. (a) Power loss breakdown near peak efficiency (@1.2/0.9 V, total current of 250 mA). (b) Power loss breakdown at heavy load (@1.2/0.9 V, total current of 1500 mA).

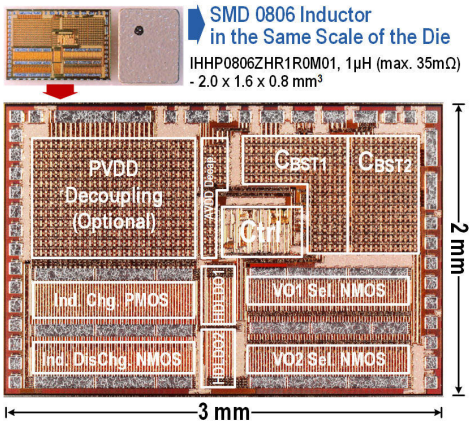

Fig. 14. Die photograph with power inductor in the same scale.

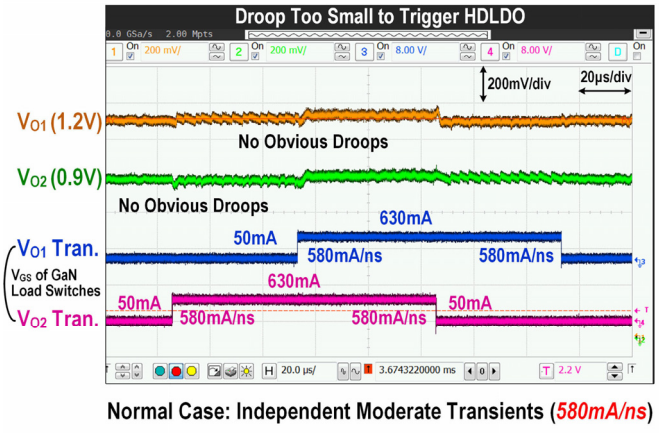

Fig. 15. Measured transient response with independent moderate transients.

III. Measurement Results

The proposed SIMO converter has been fabricated in a standard 180-nm CMOS process and measured with 1-μH 0806 miniature inductors (2 × 1.6 × 0.8 mm). Fig. 14 shows the chip photograph with the SMD inductor on the same scale. The measured transient response results are shown in Figs. 15–17 with different current steps. For a moderate independent load transient with a step of 580 mA in 1-ns time-step happened to the outputs regulated at 1.2 and 0.9 V (Fig. 15), the core control loop is fast enough to prevent excessive undershoots, and the observed voltage droops on both outputs are not obvious. In this case, the HLDOs were not triggered. In Fig. 16, for an extremely independent load transient event with ≥1-A current step in 1-ns time step, the non-linear core loop is limited by the inductor large-signal slew rate. Without the assistance of the external HLDO, the measured voltage droop is ∼100 mV when both outputs are at >1-A heavy loading conditions. With the HLDOs enabled (the voltage threshold for HLDO triggering is around 50 mV below V_{REF}), no obvious voltage droops (<50 mV) are observed at both outputs. Fig. 17 further shows the significant improvement HLDO brings at more extreme cases, in which a >1-A current-step of 1-ns time-steps simultaneously happens to both outputs (causing a combined 2.1 A in 1-ns load transient). Without the HLDOs, the voltage droops are serious with 225 and 350 mV, respectively. With the HLDO, the droops are again suppressed to an acceptable value of ∼80 mV on both outputs. Steady-state waveforms of the outputs V_{O1} and V_{O2}, the two switching nodes V_{XI} and V_{XO}, and the inductor current I_{ind} are shown in Fig. 18, with each output having 300-mA loading.

The overall efficiency shown in Fig. 19(a) is measured with different load currents for 1.5-/1.2-, 1.2-/0.9-, and 0.9-/0.6-V output voltages from a 1.8-V input. The measured efficiency peaks at 96.1%, 93.7%, and 90.4%, respectively. The light-load efficiency with V_{O1} fixed at 1.2 V and V_{O2} varies within the design range is shown in Fig. 19(b). In Fig. 19(c), a comparison of efficiency with and without bootstrap NMOS gate driver for 1.2-/0.9-V outputs reveals up to 8.92% efficiency improvement and load current range extended for above 80% efficiency. In Fig. 19(d), the efficiency comparison when the frequency hopping function is enabled/disabled is measured for different output voltages with one output fixed at 50-mA load current, showing that the frequency hopping technique benefits efficiency. In Fig. 20, the waveforms of V_{XI} and I_{ind} are also measured to verify the functionality of the proposed frequency hopping. With imbalanced 50- and 300-mA load currents at V_{O1} and V_{O2}, respectively, without frequency hopping, V_{O1} is supported with enough energy within one shot, and most of the selection period is

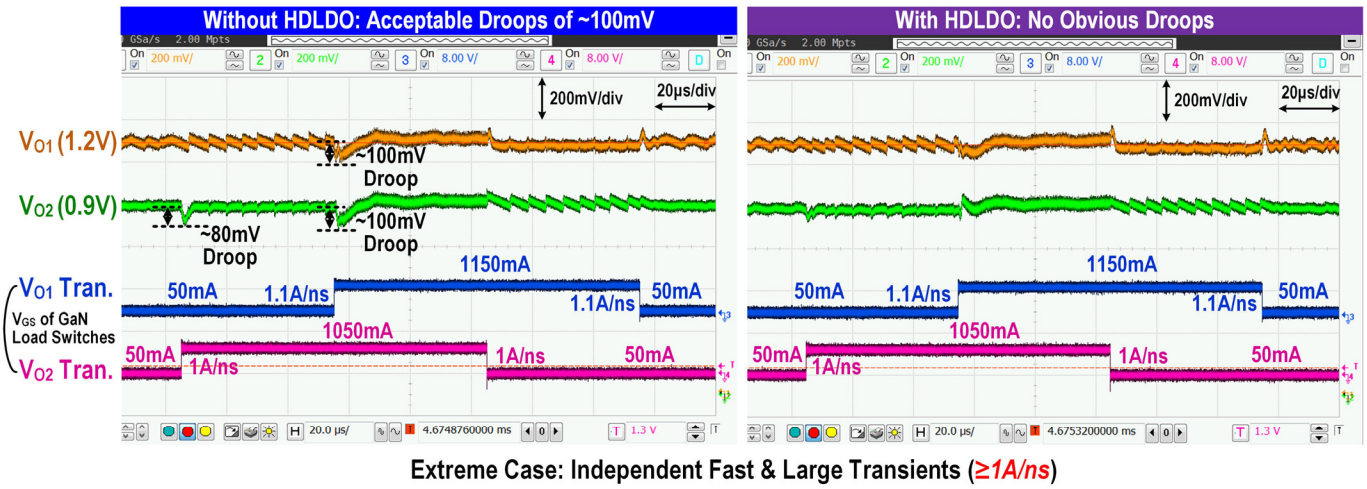

Fig. 16. Measured load transient responses without and with HDLDO at extreme cases with independent ≥1-A/ns load steps at both outputs.

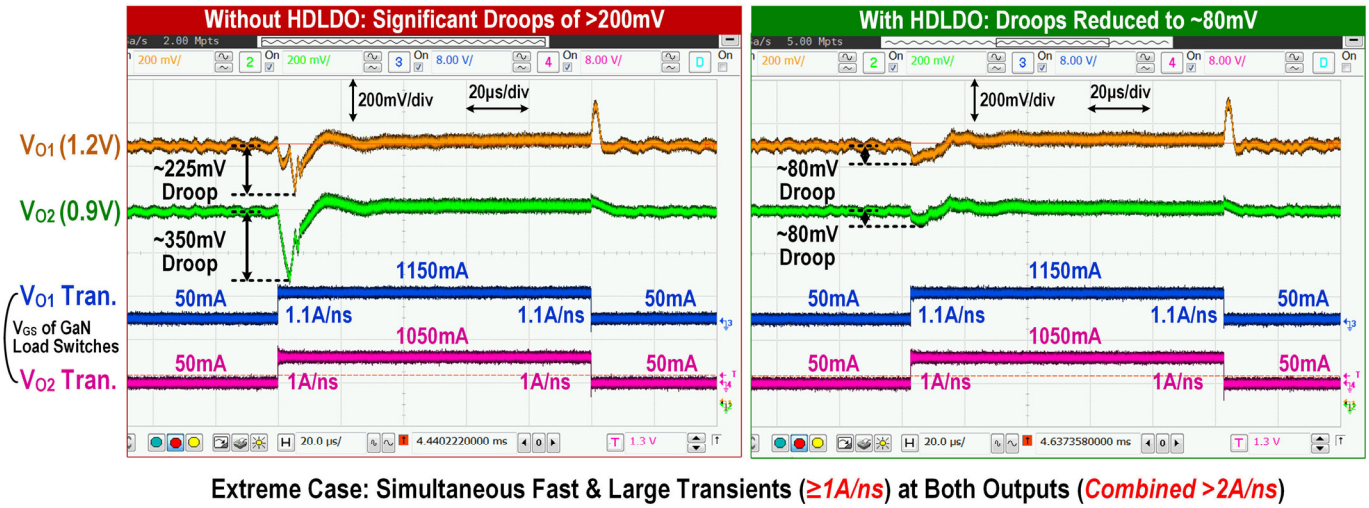

Fig. 17. Measured load transient responses without and with HDLDO at extreme cases with simultaneous ≥1-A/ns load steps at both outputs.

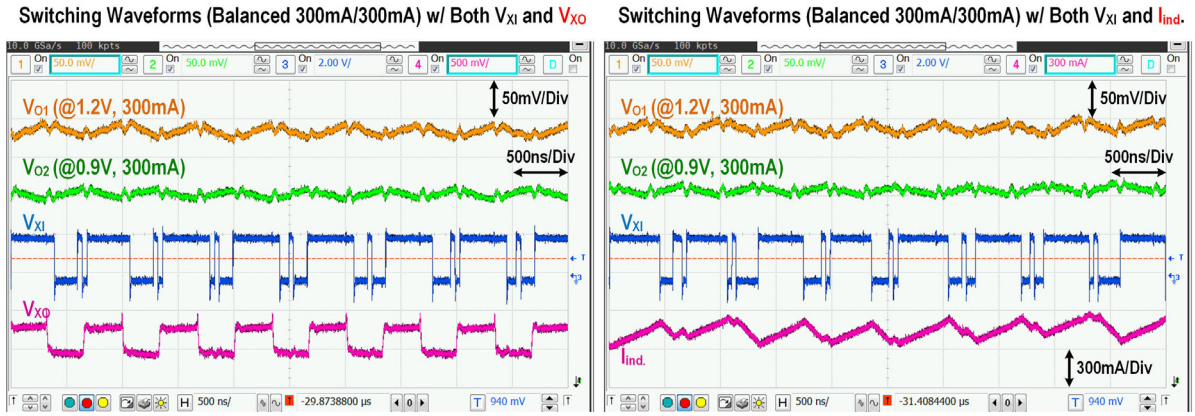

Fig. 18. Measured waveforms of both outputs, V_{XI} and V_{XO} switching nodes and inductor current with balanced load current.

provided to V_{O2}; then, V_{XI} is switched at high frequency. With frequency hopping, the switching activities of V_{XI} are reduced, which reduces the unnecessary switching loss to improve efficiency.

Table I lists the comparison of the performance of the proposed SIMO converter with state-of-the-art designs. This converter exhibits a significant improvement on load transient handling capability, from ≤300 mA of the state of the art to

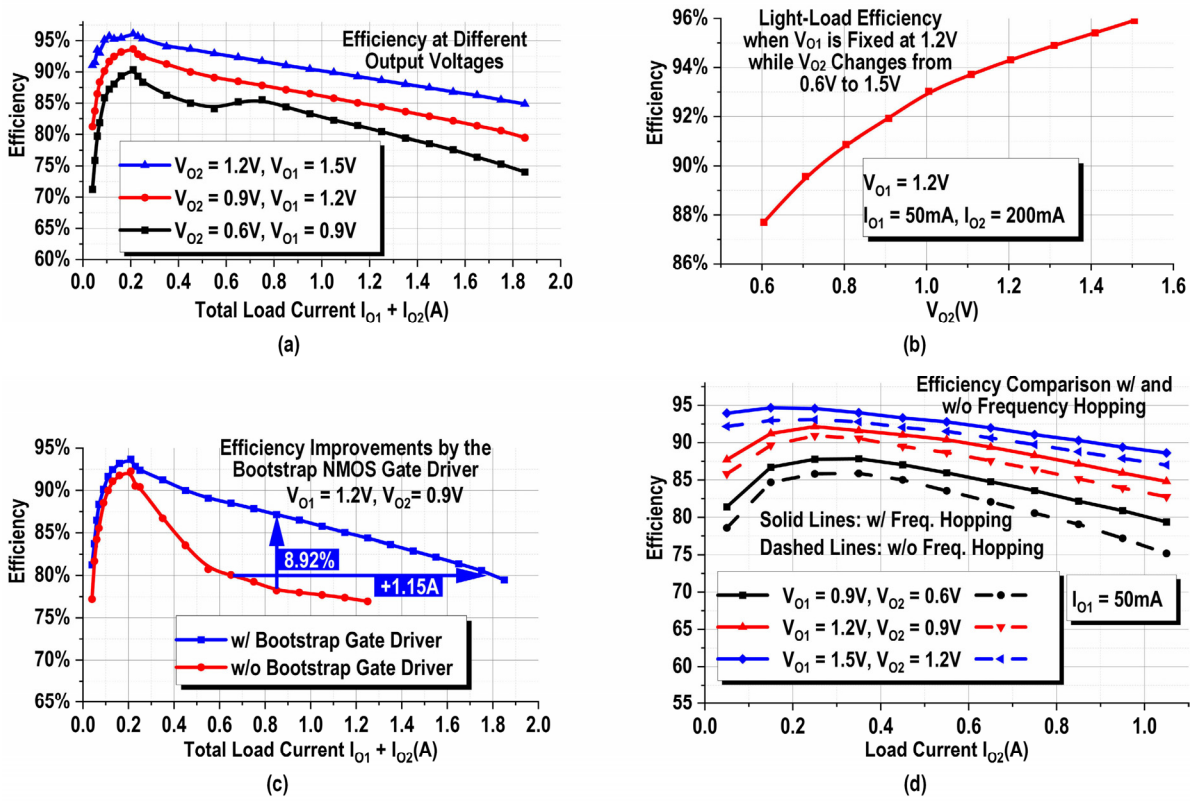

Fig. 19. Measured efficiency at different conditions (a) overall efficiency at different voltages, (b) system light-load efficiency with V_{O1} fixed at 1.2 V while V_{O2} varies within the design range, (c) efficiency improvements with and without the designed bootstrapped NMOS switches, and (d) efficiency comparison with and without frequency hopping.

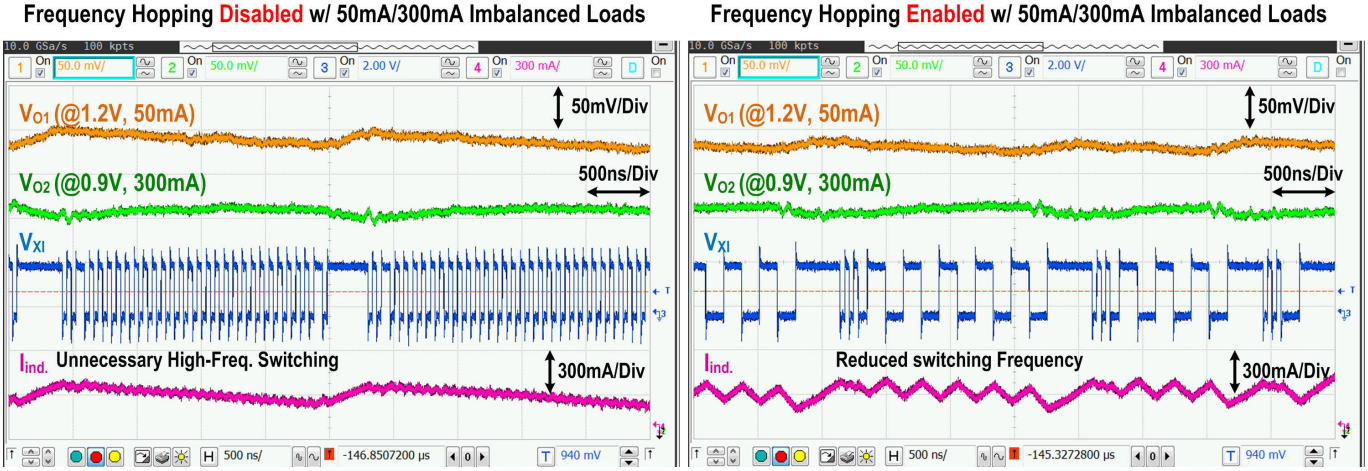

Fig. 20. Measured waveforms of both outputs V_{XI} switching node and inductor current with and without frequency hopping when the load currents of the two outputs are imbalanced.

2.1 A/ns, and a higher efficiency of 96.1%. The reasons can be summarized as follows.

Faster transient response is achieved by: 1) the proposed non-linear control with small-signal limitation in traditional linear control eliminated and 2) the HDLDO providing extra current paths with large-signal *LC* limitations eliminated.

Better power efficiency even with a miniature inductor is achieved by: 1) over-sampling frequency for inductor charging and discharging control with a higher resolution to eliminate the need of the freewheel transistor and the freewheeling cushion period that was needed to decouple the input and output stages in previous works [17]; 2) frequency hopping technique to lower the switching frequency when not necessary; 3) higher mobility NMOS (compared with PMOS) transistors are used at the output stage; and 4) bootstrap drivers for the output NMOS switches to ensure a V_O-independent fully turn-on operation, which also allows a wider output voltage and current range.

TABLE I
COMPARISON WITH STATE-OF-THE-ART DESIGNS

	ISSCC '17 [4]	ISSCC '15 [5]	JSSC '14 [6]	ISSCC '21 [9]	ISSCC '21 [7]	TPE '18 [10]	CICC '20 [20]	ISSCC '14 [18]	JSSC '15 [11]	TPE '18 [17]	**This work '23**
Tech. Node.	28nm	0.25µm	0.35µm	130nm	65nm	180nm	180nm	0.35µm	45nm	180nm	180nm
Input Voltage (V)	3-4.5	3.6-5	2.7-3.3	1-5	1.8	3.3-4	1.8	2.7-5	1.6-2	2.7-3.7	1.8
Output Voltage (V)	0.8-1.45	1.2-3.3	1.2-1.8	1.2-3.6	0.7-0.95	0.9-1.8	0.4-1.6	0.6-1.8	0.6-1.2	1-1.8	0.6-1.5
#. of Outputs	3	4	2	4	4	5	3	4	5	4	2
Inductor (µH)	3	4.7	1	2.2	10	4.7	4.7	4.7	10-15	4.7	**1**
Inductor Size	-	-	-	-	-	-	-	-	-	-	**2.0x1.6x0.8 mm^3**
Capacitor (µF)	2.2	4.7	22	10	1	10	1.5/3	10	0.013	10	10
Control Type	Linear	Linear	Linear/ Hybrid	Linear	Linear	Linear	Linear	Linear (PLL)	Linear	Non-Linear	**Non-Linear**
Max. I_O (A)	1	0.7	0.2	-	-	2.3	0.45	-	0.11	-	**2.2**
Max. P_O (W)	-	-	0.3	3	0.2	2.28	0.72	2.16	0.14	0.33	**2.7**
Max. Voltage Droops* (mV/mA)	0.068	0.064	0.15	0.133	0.42	0.5	1.14	0.16	-	1	**0.038**
Measured @ Total I_O Step (in time step)	220mA (-)	250mA (-)	90mA (40ns)	300mA (-)	78mA (0.4ns)	250mA (100µs)	140mA (-)	250mA (-)	7.5mA (-)	100mA (-)	**2.1A (1ns)**
Simultaneous Load Tran.	N	N	N	N	16mA per V_O	N	N	N	N	N	**≥1A per V_O (1.1A+1A)**
Max. Efficiency	89.6%	90%	82.8%	94.3%	84.1%	86%	87.5%	87%	73%	73%	**96.1%**

* From loading perspective, the impact caused by either self- or cross-regulation is similar: voltage droops, thus combined. This number normally gets worse with faster and larger current steps, and with heavier loadings due to the smaller error tolerance.

IV. CONCLUSION

This article proposes an SIMO buck converter advances significantly the state of the art on transient handling capability. The performance is demonstrated with a small-form-factor 0806 ($2 \times 1.6 \times 0.8$ mm) miniature inductor. With the proposed "Buffet-Like" dual sampling frequency fully comparator-based non-linear control and the loop-external assistance from the HLDOs, the SIMO converter can handle an extreme loading condition with up to 2.1-A/ns steps. Also, a 96.1% peak efficiency is achieved thanks to the precise charge redundancy control, frequency hopping, and bootstrap technique, with a wide output voltage range.

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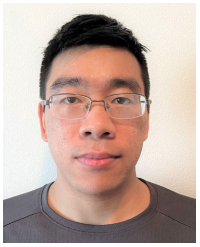

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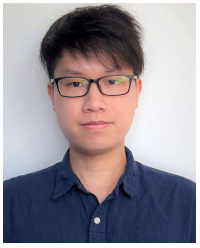

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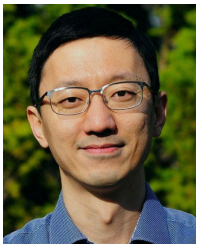

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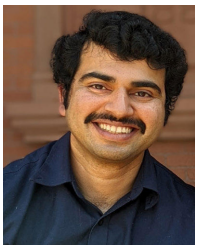

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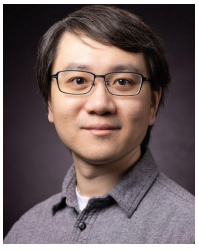

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