

A Monolithic 3-Level Single-Inductor Multiple-Output Buck Converter with State-Based Non-Linear Control Capable of Handling 1A/1.5ns Transient with On-Die LC

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3-Level Single-Inductor Multiple-Output (SIMO) buck converter is introduced in [1] to provide multiple outputs sharing one inductor to save cost while taking advantage of 3-Level topologies. Linear voltage-mode PWM control was used in [1], which is also what most single-output 3-Level converters used. It is intuitive to generate matching duty-cycles (D1 and D2) for the 2 pairs of switches by having the error amplifier (EA) outputs cutting interleaved ramps. However, linear control has small-signal bandwidth limitation, which is even more challenging to optimize with multiple dependent loops in SIMO and 3-Level converters. This is further compromised to ensure stability with PVT/component/loading variations. In the literature of SIMO converters [1-7], load-transient response was typically limited to handle steps ≤ 250 mA to avoid excessive droops due to self-/cross-regulation. Faster control loops can help correct voltage errors in time to reduce droops and support a faster and larger load transient for advanced digital loads. Non-linear control such as hysteretic control was widely used in buck converters for a faster response. However, it is not intuitive to generate switching signals to non-linearly control a 3-Level SIMO converter.

This paper introduces a fully state-based control for 3-Level SIMO converters to achieve non-linear inductor charge control with current redundancy regulation, intrinsic C_{FLY} balancing, and prioritized output rotation, demonstrating small output fluctuations at 1A/1.5ns steps and at steady-states, enhanced efficiency, and well-regulated C_{FLY} voltage even at large and fast transients. Moreover, C_{FLY} and the power inductor L are directly soldered on-die to reduce ESR and parasitic inductance for better reliability and efficiency (die photo).

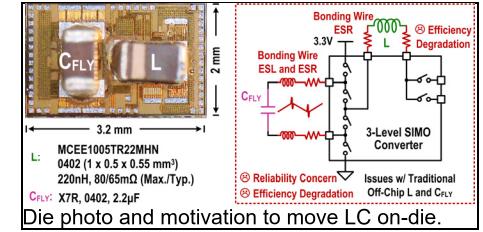
Fig. 1 shows the block diagram realizing the proposed control, with the operation principle detailed in Fig. 2. All power transistors are 1.8-V devices configured for a 3.3-V to 0.6-1.4V conversion. LDOs are designed to generate the internal rails needed to drive the power switches. Output current information is sensed and injected to the voltage-mode control to provide a more precise inductor current control for a higher efficiency and a faster dynamic response, without relying on the ESR of output capacitors. Other enhancement techniques, including auto Discontinuous-Conduction-Mode (DCM), auto output switching frequency hopping, and adaptive sizing are introduced to further optimize the light-load efficiency.

Fig. 2 shows the simplified operation principle of the proposed state-based non-linear control. 5 operation states are identified based on the charging, discharging, and holding of L and C_{FLY} . Then based on the output voltage information sensed by clocked comparators, the system rotates among different states. The following lists 3 important design considerations of the proposed non-linear control.

1) For faster transient response, a) a higher priority for L charging (compared to L discharging) is achieved by: having 3 out of 4 cases for L charging, always ensuring a *slight* current redundancy in the inductor, while L only discharges when both outputs are higher than their references; b) having a 64-MHz clock to monitor the outputs so that the system can response rapidly when droop happens. Please note that the “64 MHz” is the sampling frequency and is not the switching frequency of the 3-level power stage that is related to the redundant current regulation to be discussed later, nor the output rotation switching frequency that is load dependent and related to the system loop delay. The switching frequencies of the 3-level and output stages are independent, and output rotation is normally faster.

More details are given as follows. Only when both outputs are higher than their references, indicating a solid over-powered status, State 4 (L Hold) will be selected for freewheeling to cut off L current to the outputs, until either of them returns below its reference. Then the system enters State 3 (L Discharging) to reduce L current level. The duration of State 3 is determined by the redundancy regulation discussed next. During State 3, output rotation continuous with output Case 2-4 (Fig. 2) sensed at 64 MHz, selecting the output based on

the demands. In the meantime, at very light-load conditions, whenever the L current reaches zero, State 5 (DCM, L Hold) will be triggered to stop reverse inductor current. Also, auto frequency hopping and adaptive sizing are utilized to enhance light-load efficiency.



Die photo and motivation to move LC on-die.

2) For higher efficiency, the inductor current redundancy will be regulated to $\sim 20\%$ more than needed to maintain a good balance between transient performance and efficiency. This is done by digitally adjusting the inductor discharging period based on the length of the freewheeling period. Every time the freewheeling State 4 (L Hold) is selected, its duration will be integrated as FW_{INT} to indicate how significant the over-power status is. This will then be used to regulate the inductor current redundancy within a hysteretic window. If FW_{INT} is higher/lower than its higher/lower reference V_{FW_H}/V_{FW_L} , indicating too-much/not-enough inductor current redundancy, a 5-bit counter will increase/reduce the next State 3 (L Discharging) by 1 LSB, respectively. The freewheel period integration time-window is set to 16 μ s, which is much longer than a switching period of the converter. To avoid affecting dynamic performance due to a too-long State 3, a reset logic is designed such that when the inductor is continuously being charged for 600 ns, the control code will reset to its maximum to prepare for a heavy-load condition with the shortest inductor discharging period.

3) For ensured reliability, smaller ripple, and higher efficiency, C_{FLY} is regulated within a 300-mV hysteretic window automatically. A floating C_{FLY} sensor (Fig. 3) is designed to sense the C_{FLY} differential voltage V_{CF} , based on which V_{CF} is regulated within a hysteretic window based on State 1 (C_{FLY} Discharging) and State 2 (C_{FLY} Charging) rotation. When V_{CF} is larger/smaller than V_{CF_H}/V_{CF_L} derived from $1/2 VDD \pm 150$ mV, indicating that C_{FLY} is over-/under-charged, the power stage will start to drain/charge C_{FLY} by selecting State 1/State 2, respectively, while continuous to support the inductor current. Because V_{CF} is regulated in real-time without small-signal bandwidth limitation as long as the inductor is being charged, even during a rapid load up-transient when the inductor is charged at full slew-rate to support a heavier loading, V_{CF} can still remain in the desired range to ensure reliability.

The prototype chip is fabricated in 0.18 μ m standard CMOS. Fig. 4 shows the measured load transient waveforms. With the fast non-linear control, even with relatively extreme cases where both outputs are having a simultaneous 10-mA to 510-mA transient in a 1.5-ns time step, which combined to be 1A/1.5ns, the droops are suppressed within 50mV. Fig. 3 measures the benefits of having the C_{FLY} on-die. Due to the large Ldi/dt from switched discontinuous inductor current charging and discharging C_{FLY} through bonding wires, large spikes were observed if C_{FLY} is off chip, while no obvious spikes are observed with on-die C_{FLY} . Fig. 5 shows the measured efficiency with different output voltages, observing a peak of 91.3%. Due to the elimination of both the forward and backward bonding resistance for both the on-die C_{FLY} and L (illustrated next to the die photo above), a 3% peak and 5% heavy-load efficiency enhancement over the off-chip LC version are observed. Fig. 5 also verifies in measurements that including output current information for more accurate inductor current control can improve efficiency by up to 14%. Fig. 6 compares the proposed design with state of the arts. This work achieves smaller droops with ≥ 4 load-transient handling capability, along with higher efficiency using a small 0402 inductor that is on-die, without using advanced technology.

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References:

- [1] L.-C. Chu *et al.*, ISSCC, 2017, DOI:10.1109/ISSCC.2017.7870323
- [2] S. Kim *et al.*, ISSCC 2023, DOI:10.1109/ISSCC42615.2023.10067637
- [3] C.-H. Huang *et al.*, ISSCC 2021, DOI:10.1109/ISSCC42613.2021.9365760
- [4] Z. Zhou *et al.*, CICC 2020, DOI:10.1109/CICC48029.2020.9075892
- [5] Y. Zhang *et al.*, JSSC 2014, DOI:10.1109/JSSC.2014.2304497
- [6] D. Lu *et al.*, ISSCC 2014, DOI:10.1109/ISSCC.2014.6757347
- [7] T. Y. Goh *et al.*, TPE 2018, DOI:10.1109/TPEL.2017.2700483

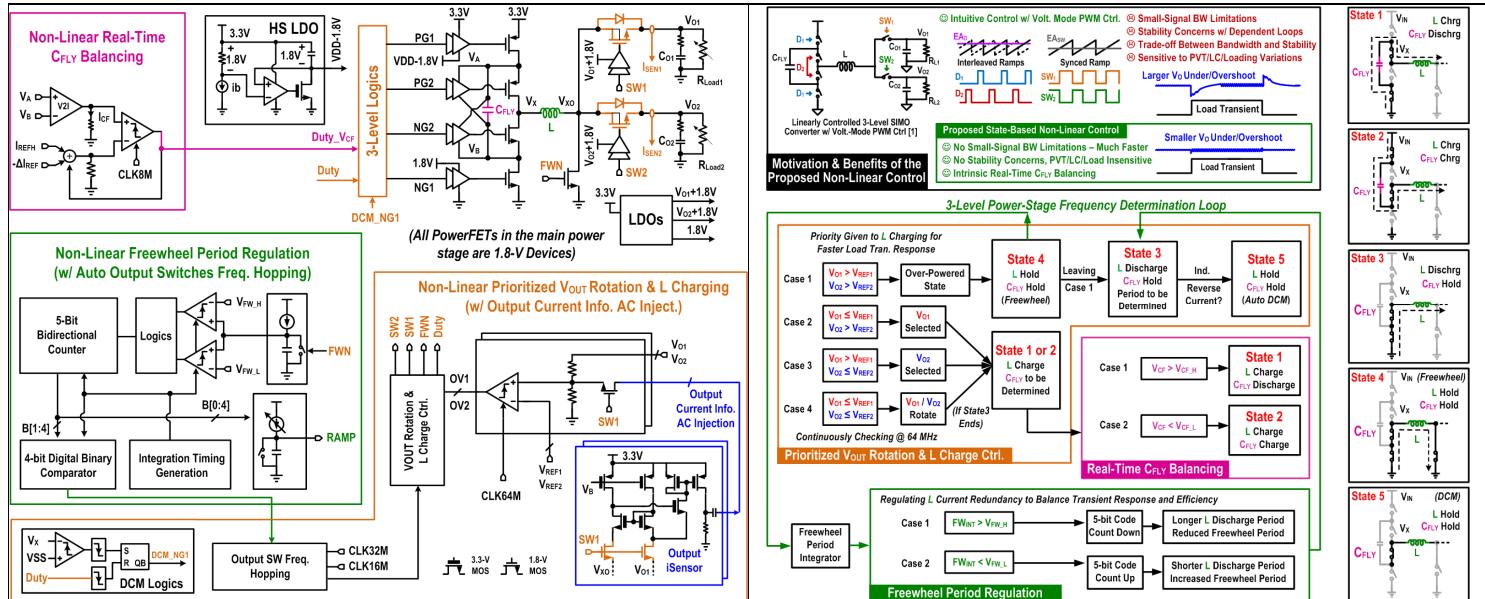


Fig. 1. State-based non-linearly controlled 3-level SIMO converter.

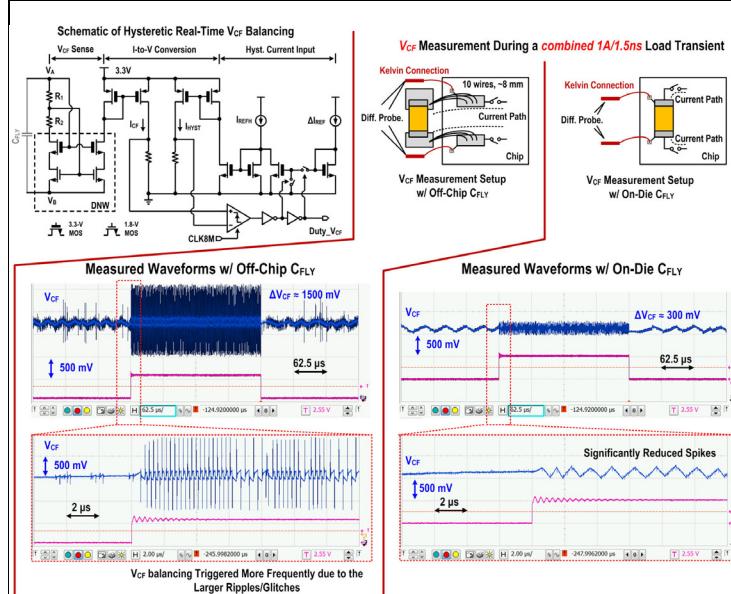


Fig. 3. CFLY balancing, and measured benefits of moving CFLY on-die.

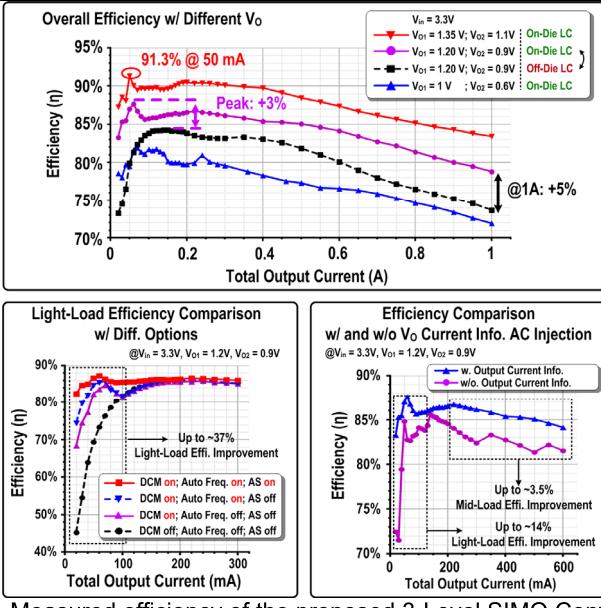


Fig. 5. Measured efficiency of the proposed 3-Level SIMO Converter.

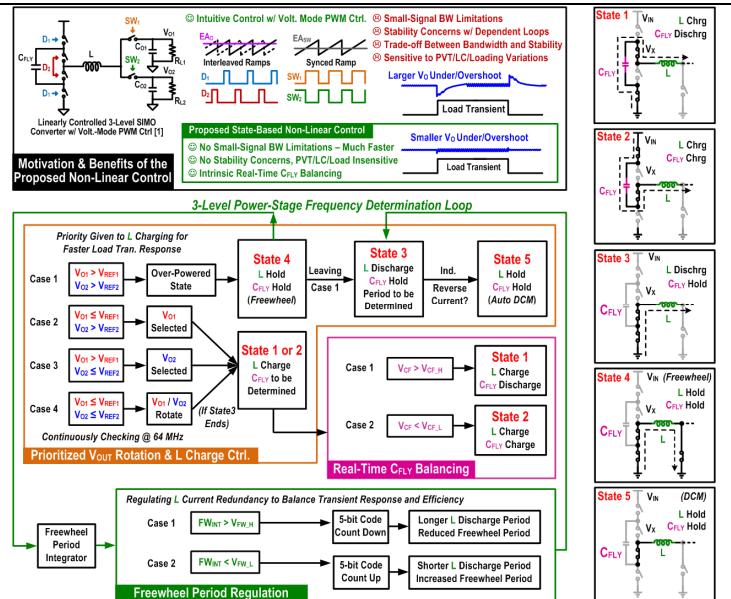


Fig. 2. Simplified operation principle of the proposed non-linear control.

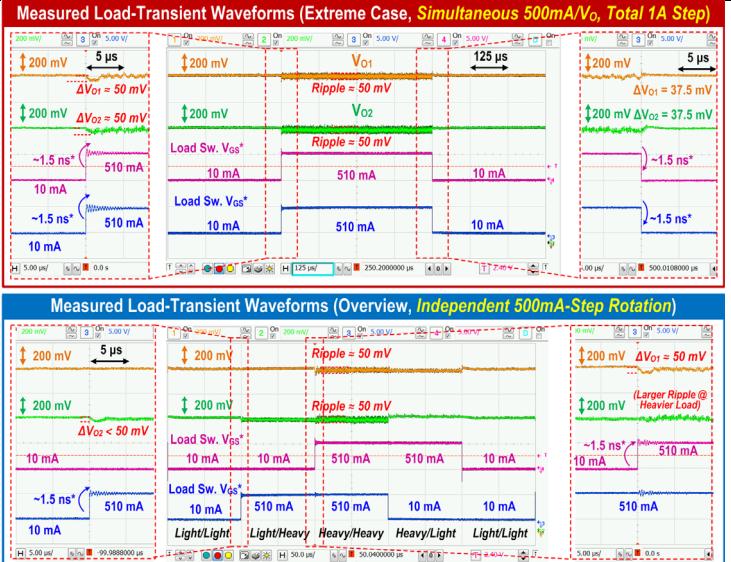


Fig. 4. Measured waveforms at with different load transient steps.

	CICC'20 [4]	ISSCC'21 [3]	JSSC'14 [5]	ISSCC'14 [6]	TPE'18 [7]	ISSCC'23 [2]	ISSCC'17 [1]	This work
Tech. Node	180nm	65nm	0.35μm	0.35μm	180nm	16nm	28nm	180nm
3-Level	N	N	N	N	N	N (Stacked)	Y	Y
# of Outputs	3	4	2	4	4.7	4	3	2
L (μH)	4.7	10	1	4.7	4.7	0.005/0.01	2.2	0.22
L Integration	N	N	N	N	N	N	N	On-Die
L Size	N.A.	N.A.	N.A.	N.A.	N.A.	N.A.	N.A.	0402 (0.275mm ²)
CFLY Integration	N	N	N	N	N	N	N	On-Chip (+1nF On-Chip)
C_O (μF)	1.5/3	1	22	10	10	20	2	10
Control Methodology	Linear	Linear	Linear/Hybrid	Adaptive Off-time	Single-Discharge	Adaptive On-time	Linear	State-Based Non-Linear
V_{in} (V)	1.8	1.8	2.7-3.3	2.7-5	3	1.8	3-4.5	3.3
V_O (V)	0.4-1.6	0.4-1	1.2, 1.8	0.6-1.8	1.1, 1.2, 1.5, 1.8	0.8-1.4	0.8, 1.2, 1.45	0.6-1.35
Max. I_O (A)	0.45	0.22	0.2	1.2	0.2	1.5	1	1
Max. Droop* (mV/mA)	1.14	0.42	0.083	0.16	0.8	1.67	0.068	0.05
Transient total I_O step (in time Step)	140mA (N/A)	78mA (0.4ns)	180mA (40ns)	250mA (N/A)	100mA (N/A)	180mA (N/A)	250mA (N/A)	1A (1.5ns)
Max. Efficiency	87.5%	84.1%	82.8%	87%	73%	87.3%	89.6%	91.3%

* Including the worst output voltage droops/fluctuations caused by both self-/cross-regulation, divided by the corresponding total load-current step. The numbers are extracted from measured waveforms in the papers.

Fig. 6. Comparison with prior SIMO converters.