

# BitGNN: Unleashing the Performance Potential of Binary Graph Neural Networks on GPUs

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## ABSTRACT

Recent studies have shown that Binary Graph Neural Networks (GNNs) are promising for saving computations of GNNs through binarized tensors. Prior work, however, mainly focused on algorithm designs or training techniques, leaving it open to how to materialize the performance potential on accelerator hardware fully. This work redesigns the binary GNN inference backend from the efficiency perspective. It fills the gap by proposing a series of abstractions and techniques to map binary GNNs and their computations best to fit the nature of bit manipulations on GPUs. Results on real-world graphs with GCNs, GraphSAGE, and GraphSAINT show that the proposed techniques outperform state-of-the-art binary GNN implementations by 8-22X with the same accuracy maintained. BitGNN code is publicly available.<sup>1</sup>.

## CCS CONCEPTS

- Computing methodologies → Neural networks; Massively parallel algorithms;
- Computer systems organization → Single instruction, multiple data.

## KEYWORDS

graph neural networks, binarized GNN, bit manipulation, GPU, sparse matrix

### ACM Reference Format:

Jou-An Chen, Hsin-Hsuan Sung, Xipeng Shen, Sutanay Choudhury, and Ang Li. 2023. BitGNN: Unleashing the Performance Potential of Binary Graph Neural Networks on GPUs. In *International Conference on Supercomputing (ICS '23), June 21–23, 2023, Orlando, FL, USA*. ACM, New York, NY, USA, 13 pages. <https://doi.org/10.1145/3577193.3593725>

<sup>1</sup><https://github.com/PICTureRG/BitGNN>

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ICS '23, June 21–23, 2023, Orlando, FL, USA

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ACM ISBN 979-8-4007-0056-9/23/06...\$15.00  
<https://doi.org/10.1145/3577193.3593725>

## 1 INTRODUCTION

Recent years have witnessed a rapidly increasing adoption of Graph Neural Networks (GNNs) in various domains, from social networks [1] to bioinformatics [2], computational chemistry [3, 4], 3D computer vision [5, 6], and so on. GNN allows the linear and non-linear transformations of Neural Networks to work directly on graphs. By seamlessly integrating both the graph structure and node/edge features into the modeling, GNN is a natural fit for graph-based problems. Numerous studies [7–12] on graph-based classification and prediction have reported significantly better results achieved through GNNs than traditional methods.

Because real-world graphs are often large, GNN inference is often time-consuming and space-hungry, frequently exceeding the capacity of the storage or memory and the desirable latency. Inspired by the binarization (i.e., quantization to the 1-bit extreme) for ordinary deep neural networks [13–17], an emerging effort is to investigate the potential of GNN binarization. By converting each value in the activation maps, weights, and/or adjacency matrices into a single bit (sometimes through matrix factorizations), GNN binarization can significantly reduce the space demands and computation amounts.

The continuous research in the recent several years on GNN binarization has achieved some remarkable progress [18–21]. For instance, the accuracy loss caused by binarization has reduced from 16% to less than 5% [18]. These studies show solutions that can control the loss of accuracy within a small percentage on various graphs and architectures while giving significant theoretical reductions in the number of computations and memory usage. Nevertheless, how to turn the potential into full speedups and memory savings on real machines remains an open question. For example, based on a theoretical analysis, the authors of a recent study [18] on binary GNNs report ~47X potential savings of computations and ~30X possible memory footprint reduction. Still, their experiments show no speedups or memory savings over the original non-binarized GNN.

Existing work on binary GNNs mainly focuses on *algorithm-level* improvement on network architectures [18–20] or training techniques [18, 20, 21]. The immense potential of binary GNN inference on hardware has not yet been harvested.

Quantizing tensors into bits and representing and manipulating them efficiently on word-based architecture involves lots of intricacies. It is even more so for GNNs, for several reasons. First, a GNN layer typically consists of interleaving dense and sparse operators. It is not straightforward to reconcile the inconsistency between dense and sparse bit-level layouts while minimizing the inference latency and achieving desirable accuracy-speed tradeoffs. Second, in binary GNNs, the meaning of bits in activations/weights (1/0 means +/-) and graphs (1/0 means connectivity) differ. For these special properties, integer intrinsics should be carefully orchestrated to maximize bit-level and thread-level parallelism. Third, to fully harness the significant memory reduction brought by bit representation, it is important to synergize the careful use of registers and memory hierarchy with the massive parallelism on accelerators.

This work provides the first known systematic exploration to unlock the performance potential of binary GNNs. The target hardware it focuses on is Graphics Processing Units (GPUs), the most commonly used device for GNNs and binary GNNs. This work makes four-fold contributions:

**(1) Materializing binary GNNs with a series of bit-level optimized abstraction.** To effectively materialize a binary GNN model, there are various possible compositions of bit-level BLAS kernels with various choices in precisions, eliminations of rebinarization, and fusions. We propose the first known two-level Binary GNN abstraction, which hides the complexities from users, offers flexible support of various scenarios and enables easy drop-in replacements for converting a GNN into a binary GNN.

**(2) Representation of bit tensors.** Binary GNN includes binarized activations, weights, and adjacency matrices. Unlike activations and weights, adjacency matrices are typically sparse, the representation of which is subject to a granularity dilemma. We propose a *fine-representing dynamic-coarsening* (FRDC) scheme to simultaneously minimize graph storage cost and maximize kernel efficiency on a GPU. Additionally, we propose several solutions to reconcile the 1/0 and +/- inconsistency between binary graphs and activations.

**(3) Materialization of the BitGNN abstractions.** We develop the BitGNN abstractions into an efficient library through careful bit manipulations via binary intrinsics and memory and parallelism optimizations. We devise and materialize the abstractions for different precision needs with bit-manipulation intrinsics. We propose a series of techniques with dedicated treatment on workload decomposition, bit-tensor load/store with registers and on-chip memory usage, intra-warp and inter-warp synchronizations, and efficient binary sparse matrix multiplication (BSpMM) kernels.

**(4) Evaluation of BitGNN.** We integrate all the techniques into a full solution, namely BitGNN, in the form of a collection of a library and tuning utilities. Compared to the state-of-the-art binary GNN [18] and full-precision GNN [22] implementations, BitGNN gives up to 26X, 22X, and 19X latency reduction on GCN, GraphSAGE and GraphSAINT models. Meanwhile, BitGNN makes GNNs possible to efficiently process several graphs that are too large to process by prior solutions.

## 2 BACKGROUND

### 2.1 Graph Neural Networks

There are typically two types of operations in a GNN: *aggregate* and *apply*. The *aggregate* phase collects the information from the input graph's geometric structure. The *apply* phase performs linear or non-linear operations as in typical Neural Networks. A GNN can be formulated as follows:

$$\mathbf{X}_i^{(l+1)} = \gamma_\theta \left( \mathbf{X}_i^{(l)}, \Psi_{j \in N(i)} \phi_\theta \left( \mathbf{X}_i^{(l)}, \mathbf{X}_j^{(l)}, \mathbf{E}_{i,j} \right) \right)$$

For node classification tasks, the node representation is the activation in each GNN layer. The representation of node  $i$  at layer  $l$  is denoted as  $\mathbf{X}_i^{(l)}$ .  $N(i)$  represents the set of neighbors of node  $i$ . In an *aggregate* phase,  $\Psi$  denotes a permutation-invariant function that performs message aggregation. The commonly used functions include sum, mean, and max. Before the aggregation,  $\phi_\theta$  denotes any user-defined operators applied to the following:  $\mathbf{X}_i$  (the representation of node  $i$ ),  $\mathbf{X}_j$  (the representation of node  $j$ , the neighbors of node  $i$ ), or  $\mathbf{E}_{i,j}$  (the representation of edge  $(i, j)$ ). After the aggregation,  $\gamma_\theta$  denotes the operations of the *apply* phase. Most GNNs have neural operations (e.g., MLP and ReLU) in this phase. We briefly explain several popular GNNs.

**GCNConv** Graph Convolutional Network (GCN) [7] introduces a semi-supervised learning algorithm that can learn the graph structure directly. A forward layer of GCNConv can be defined as follows:

$$\mathbf{X}^{(l+1)} = \sigma(\tilde{A}\mathbf{X}^{(l)}\mathbf{W}^{(l)}),$$

where, the normalized adjacency matrix  $\tilde{A}$  equals  $\hat{D}^{-\frac{1}{2}}\hat{A}\hat{D}^{-\frac{1}{2}}$ . The  $\hat{A} = A + I$  is the adjacency matrix plus self-adjacency, and  $\hat{D}_{ii} = \sum_{j=0} \hat{A}_{ij}$  is its diagonal out-degree matrix.  $\mathbf{X}^{(l)} \in \mathbb{R}^{N \times d}$  denotes the node feature embedding in the  $l$ -th layer, and  $\mathbf{W}^{(l)}$  is the learnable parameters or weights, and  $\sigma$  represents a non-linear activation function (e.g., ReLU). Bi-GCN [18] is composed of two such GCNConv layers.

**SAGEConv** SAGEConv [23] enhances the graph convolution layer with a mean aggregator as it is a linear approximation of a localized spectral convolution [7]. It also extends the layer with a skip connection to emulate the concatenation of the prior layer's node representation in the convolutional aggregator. A SAGEConv layer is defined as follows:

$$\mathbf{X}_i^{(l+1)} = \mathbf{X}_i^{(l)}\mathbf{W}_1^{(l)} + \text{mean}_{j \in N(i)} \mathbf{X}_j^{(l)} \cdot \mathbf{W}_2^{(l)}$$

**GraphConv** GraphConv [24] is similar to SAGEConv except that it uses a normal sum aggregator:

$$\mathbf{X}_i^{(l+1)} = \mathbf{X}_i^{(l)}\mathbf{W}_1^{(l)} + \sum_{j \in N(i)} \mathbf{X}_j^{(l)}\mathbf{W}_2^{(l)}$$

To allow learning on large graphs, GraphSAGE [23] proposes a neighbor sampling approach to deal with the neighbor explosion problem on large graph training. Bi-GraphSAGE [18] is composed of two such SAGEConv layers. GraphSAINT [25, 26] introduces a graph sampling-based inductive learning approach. The Bi-GraphSAINT [18] model referred to in this paper comprises two GraphConv layers and a fully-connected layer.

## 2.2 Binary Neural Networks

A bit-dot-product between two 0/1 bit-vectors can be computed as follows:

$$c = \text{popc}(a_{(b)} \& b_{(b)}),$$

where  $\&$  denotes logic AND operation and  $\text{popc}()$  is the population count function that counts the number of 1 bits.

In binary neural networks (BNNs) [13–16], the binarization function is often defined as follows:

$$x_{(b)} = \text{sign}(x) \begin{cases} 1, & \text{if } x \geq 0 \\ -1, & \text{otherwise} \end{cases}$$

The bit-dot-product operation of +1/-1 bit-vectors can be computed through:

$$c = n - 2 \times \text{popc}(a_{(b)} \oplus b_{(b)}) = 2 \times \text{popc}(a_{(b)} \odot b_{(b)}) - n$$

where  $\oplus$  is exclusive-OR (XOR),  $\odot$  is exclusive-NOR (XNOR), and  $n$  is the *bit-width* of  $a_{(b)}$  and  $b_{(b)}$ .

## 2.3 Bit-ops Intrinsics

Other than commonly-seen logical AND ( $\&$ ), OR( $\mid$ ), XOR ( $\wedge$ ), negation ( $\neg$ ), bit left-shifting ( $\ll$ ) and right-shifting ( $\gg$ ), GPUs are equipped with several integer intrinsics that can be used for efficient bit operations.  $\text{__popc}()$  and  $\text{__popcl}()$  allow fast bit-accumulation of a single 32-bit or 64-bit unsigned integer.  $\text{__shfl\_sync}()$  is for register data exchange between threads in a warp [27]. By indicating the thread lane to exchange, the intrinsic will receive register data from the designated thread lane.  $\text{__ballot\_sync}()$  is a warp-voting intrinsic used for register data exchange between threads in a warp. Assuming all threads in a warp are active, it will return a bit-masked 32-bit unsigned integer showing the boolean evaluation result of the predicate-argument in each thread. It is the same as a clockwise transpose of a bit-column into a bit-row and can be useful for fast binarizing the full-precision values with a warp of threads.  $\text{__brev}()$  and  $\text{__brevll}()$  reverse the bit-order of a 32-bit and a 64-bit unsigned integer, respectively. When paired with  $\text{__ballot\_sync}()$ , they can be helpful in rotating a bit-column 90° anti-clockwise into a bit-row [28]. Our implementation of efficient binary GNN is based on those intrinsics. As similar intrinsics can be found in other vendors' GPUs [29], our BitGNN is portable to other GPU platforms.

## 3 BITGNN

Our design of BitGNN aims to achieve (i) efficiency: a GNN using BitGNN should enjoy a significantly higher speed; (ii) accuracy: a binary GNN that uses BitGNN should be able to get the same accuracy as the binary GNNs by prior approaches do; (iii) ease to use: with BitGNN, users should be able to convert a GNN into a binary GNN easily; (iv) flexible to tune: Different GNNs may require a different accuracy-speed objective; with BitGNN, users should be able to tune the tradeoff easily.

This section presents our design. The design of BitGNN consists of a set of novel abstractions, representations, algorithms, and optimizations. The final materialization is a library and utilities that users can use to build and tune their efficient binary GNNs easily.

Two key components of a GNN are operations and tensors. Correspondingly, our creation of BitGNN centers around three key

research questions: (R1) What should be the abstractions of common binary GNN operations? (R2) How should binary tensors be represented? (R3) How to assemble them into efficient ready-to-use libraries?

### 3.1 R1: What should be the abstractions of common binary GNN operations?

GNNs have many kinds, and their binarized forms may consist of even more complexities and variations, depending on which part of the GNN is binarized for good accuracy-speed tradeoffs. For BitGNN to be easily applicable to various GNNs, it is hence important to abstract the common binary GNN operations into some building blocks. The result of such an abstraction must cover the most important operations of various binary GNNs, and at the same time, support their different needs in binarization. To the best of our knowledge, no prior work has studied systematic abstractions of binary GNN operations.

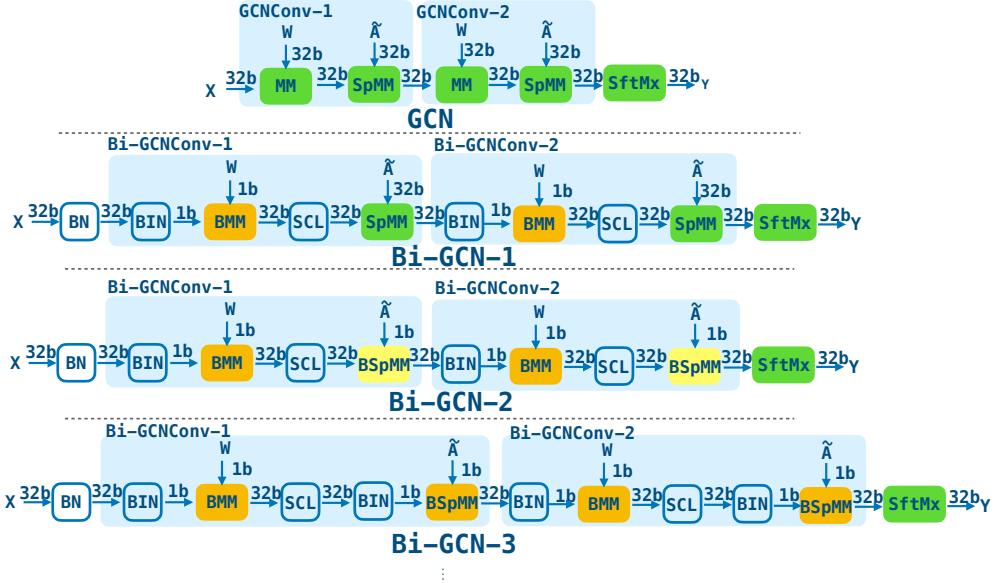
**3.1.1 Complexities.** To provide a deeper understanding of the complexities involved in designing binary Graph Neural Network (GNN) operations, this section takes a closer look at the binarization process using the Graph Convolutional Network (GCN) as an example.

The top graph in Figure 1 illustrates the original GCN [7]. A forward pass of GCN involves two GCNConv layers followed by a softmax. Each GCNConv layer starts with a matrix-matrix multiplication (MM), where the input activation is multiplied by the weight matrix. The result at each graph node is then aggregated with its neighbor nodes' results, which is carried out by multiplication with the adjacency matrix of the graph. Because the adjacency matrix is typically sparse, the second matrix multiplication can use sparse matrix multiplication (SpMM).

Below the original GCN in Figure 1, three variations of the binarized form of GCN are shown. The first one, Bi-GCN-1, is based on a previous work [18]. It replaces the first MM with binary matrix multiplication (BMM) by binarizing the weight matrix offline. It also includes three extra operations - batch normalization (BN), a tensor binarization (BIN) before BMM, and a scaling operation (SCL) after the BMM to recover the scale of the results. The second MM is also replaced with BMM, and a BIN and an SCL operation are inserted before and after BMM, respectively.

The binarized form of Bi-GCN-1 focuses solely on the binarization of the two MM operations in the original GCN. However, other operations in the GCN could also be binarized, perhaps to varying degrees. For example, Bi-GCN-2 in Figure 1 demonstrates a variant in which the two SpMM operations are "half" binarized - that is, the adjacency matrices are binarized, but the activation maps are not. In contrast, Bi-GCN-3 in Figure 1 showcases a scenario where the two SpMM operations are fully binarized, with more auxiliary operations included. All three variations have their advantages and disadvantages: as the binarization increases, there is a potential for greater speedups, but also an increased risk of accuracy loss. It is evident that, besides these three variants, there can be numerous other variants, each corresponding to the combination of operations binarized to a certain degree.

Designing binary GNN operations becomes even more complex when the GNN contains additional operations, as illustrated by the original architectures of SAGE and SAINT depicted at the top



**Figure 1: Illustration of the original full-precision GCN [7], and several variants of binary GCN.**

of Figure 2. Our analysis of numerous common GNNs and their binarized forms lead us to several observations:

- (i) There can be multiple possible binarized forms for a given GNN, each involving numerous additional operations.
- (ii) A simple one-on-one mapping is insufficient. After various binarizations, a single operation in the original GNN may be replaced with different sequences of operations. Therefore, creating only one abstraction for the binarized form of a specific original operation is inadequate.
- (iii) There is a set of operations that constitute the core operations of binary GNNs. The variations depicted in Figure 1, for instance, are all composed of BN, BIN, BMM, SCL, SpMM, and softmax, despite their differences in specific connections and architectures. This pattern also emerges in other GNNs since most GNNs have MM and SpMM as their core operations.

### 3.1.2 Two-level BitGNN Abstraction.

Based on our observations, we develop a two-level BitGNN abstraction and design them according to the following principles:

- (1) Coverage: The abstraction must cover the most time-consuming core parts of common GNNs.
- (2) Flexibility: The abstraction should support the need for different accuracy-speed tradeoffs.
- (3) Efficiency: The abstraction should be mindful of the implications to computing efficiency.
- (4) Ease of application: The abstraction should allow for easy adoption in GNN development so that a GNN can be easily revised into a binary GNN. Furthermore, it should support easy tuning of the binarization process to achieve different accuracy-speed objectives.

The bottom of Figure 2 displays the core components of the abstraction. The low-level functions provide the primary building blocks, while the high-level functions offer options for drop-in replacement of the components in GNNs for binarization. The former offers flexibility, while the latter offers ease of use.

**Low-level functions.** The low-level functions are grouped into three categories. The first group focuses on the binarization of matrix multiplication (MM). In prior binary GNN materializations, one of the performance bottlenecks is the re-binarization of activation tensors in each layer. Our design of the functions takes this into consideration. We include seven BMM variants, each corresponding to a different combination of input activation, weight matrix, and output precisions, as shown at the bottom of Figure 2. These precisions determine the auxiliary operands required (e.g., full-precision inputs require BIN before participation in the multiplication). In our design, these operands are included within the BMM functions to avoid invocation overhead and the need for complex kernel fusions.

One of our insights is that when BIN immediately follows SCL, the SCL becomes redundant and can be removed. The reason for this is that the scaling factor is always positive<sup>2</sup>, so the element-wise multiplication of the scaling factor will not affect the binarization result.

The second group of low-level functions is related to SpMM operations that are commonly used for multiplications involving adjacency matrices in GNNs [30]. Our design of binarized forms includes eight variants, as illustrated at the bottom of Figure 2. The reasons for these variants include the accuracy-speed tradeoff, similar to the BMM case, and the special property of adjacency matrices. In GNN workloads, the connections between two nodes may or may not carry weights. In the former case, only 0/1 values are in the adjacency matrix, representing node connectivity. In the latter case, BSpMM can still be applied using a standard approach to binarize an adjacency matrix through factorization. Following the matrix multiplication, there will be a multiplication with a full-precision factorization vector.

The third group consists of auxiliary operations, such as the add operations for self-connectivity and concatenation operations. As

<sup>2</sup>In Bi-GCN [18], for instance, the scaling factors are the row-wise and column-wise L1 normalization values.

binary operations may output results of different precisions, this group includes several variants. However, unlike other operations, mixed precisions of operands for these two operations are not meaningful in practice, and our design excludes those variants.

**Notation:** for convenience, the following discussion uses a **three-letter suffix** to distinguish the variants of an operator: For instance, BSpMM.FBB represents BSpMM that takes in a full-precision (F) matrix (1st operand) and a binary (B) matrix (2nd operand) as inputs and produces a binary (B) matrix.

*High-level functions.* The low-level functions cover the most essential operations in binary GNNs and provide flexibility in meeting various needs. To facilitate adoption, we also design a set of high-level functions that enable simple drop-in replacement of key time-consuming operations in a GNN for binarization. Our research reveals that despite the wide range of GNNs available, their most time-consuming core operations are matrix multiplications (MM) and sparse matrix multiplications (SpMM). As a result, our high-level functions revolve around these operations and their combinations.

The high-level functions are organized into two groups, each combining multiple low-level functions to ease the adoption of binary GNNs. The first group is designed for a typical case where BSpMM immediately follows BMM, as seen in GCN illustrated in Figure 2. The variants are determined by the activation tensor between the BMM and SpMM operations. It can be either in binarized form (B) or full-precision form (F). Consequently, we have BMM.FBB+BSpMM.BBB or BMM.FBF+BSpMM.FBB for the first GCNConv layer, and BMM.BBF+BSpMM.FBF or BMM.BBB+BSpMM.BBF for the second GCNConv layer. The second group is designed for another common case where some auxiliary operations follow MM, as seen in the architecture of SAGE in Figure 2. The auxiliary operator comes from self-connectivity, for which we can use either ADD.BBF or ADD.FFF to merge the activation output at the end of the first SAGEConv layer.

The top of Figure 2 demonstrates how the three GNNs can be easily converted into binary GNNs by replacing the common operation sequences with the corresponding high-level functions. Low-level functions with small latency, such as ADD, are fused with BMMs or BSpMMs, while high-level functions are optimized through inter-layer fusions between BMMs and BSpMMs using cooperative kernel launch to improve thread block synchronization. Furthermore, the high-level functions enable easy tuning of binary GNNs for accuracy-speed tradeoffs. For instance, the user can replace the two MM-SpMMs in GCN.bin shown in Figure 2 with other options in the high-level function set. As long as the output precision of a predecessor block matches the input precision of its successor, the correctness of types is guaranteed, while the accuracy and speed may vary.

To summarize, BitGNN’s design of high-level and low-level abstractions provides comprehensive coverage of the decision space for binary GNN architecture exploitation. At the low-level, the design addresses the various precision requirements of the core operations while minimizing invocation overhead. At the high-level, the design avoids unnecessary rebinarization, offers flexibility for tuning accuracy-speed tradeoffs, and enables straightforward drop-in replacement for converting GNNs to binary GNNs.

### 3.2 R2: How to represent binarized tensors?

The representation of binarized tensors plays a crucial role in determining the efficiency of memory usage and data access speed of binarized GNNs. However, existing binary GNN implementations such as those in [13–16] do not truly store activation or weight tensors in bits, nor do they consider storing the graph in bits.

In conventional DNNs, some work has explored the representation of binary tensors and proposed various representations, as seen in [28, 31]. Nevertheless, two special complexities in GNNs call for innovative solutions. In the following, we will focus on discussing each of these complexities and the solutions we propose.

**3.2.1 Granularity Dilemma.** The first complexity is about the granularity of representations.

*Dilemma.* There are many representations proposed for sparse matrices, and one that shows a particularly good fit for adjacency matrices is block-based representation [30]. In this representation, the matrix is viewed as a composition of many k-by-k blocks, with each block’s content stored in a dense format. The block-level representation uses a sparse format (e.g., CSR) with all-zero blocks being ignored.

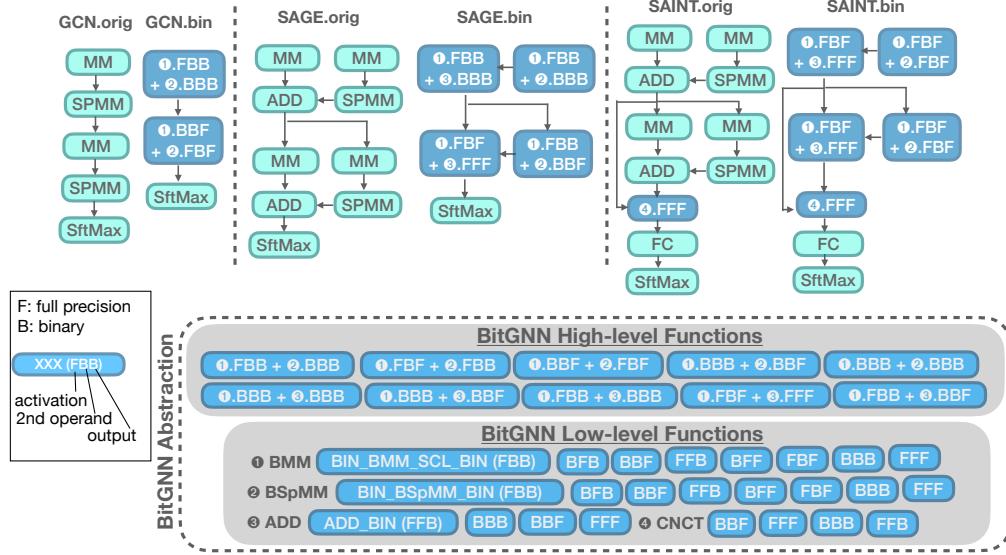
This representation, however, faces a dilemma with block size. The smaller the block size, the fewer zeros will be included in the representation, but it also leads to more reduction operations among blocks. A smaller block is also less friendly to the massive parallelism of the GPU.

*Solution.* To address the dilemma of block size, we propose *fine-representing dynamic-coarsening (FRDC)*. This approach utilizes a fine-grained representation to achieve high space efficiency and on-chip coarsening to attain high time efficiency. Specifically, FRDC uses a 4×4 block size for representation. The choice of 4×4 is motivated by the need to use a fine-grained representation to store matrices while using online stitched coarse-grained representation for computations. This approach saves storage and memory space while better exploiting bit-level parallelism.

Using larger block sizes such as 4×8 or 8×4 doubles memory usage, while smaller tiles lead to increased dynamic stitching overhead. Our empirical results demonstrate that 4×4 is a suitable block size. During computations, the 4×4 bit-blocks containing 16 bits are transferred from GPU DRAM to shared memory/registers. The BitGNN kernel then assembles the 4×4 bit-blocks into 32-bit aligned words on shared memory and efficiently processes them using word-level bit manipulation intrinsics (see Section 2.3). By using this approach, we can maintain the space benefits of the fine-grained representation while achieving maximal parallelism.

**3.2.2 Inconsistent Value Ranges.** The second special complexity arises from the different value ranges of tensors after binarization.

One common situation is the inconsistency between adjacency matrices and activation maps. While adjacency matrices use 1/0 to denote edge connectivity, the basic operation is a 0/1 dot-product. On the other hand, binary neural network activation uses the +1/-1 dot product. This inconsistency presents a challenge when conducting multiplications between them efficiently. However, previous studies have not addressed this issue.



**Figure 2: Core components of the two-level BitGNN abstraction (bottom) and its usage examples (top). At the low-level, BitGNN supports the core kernels in bit-ops, including ① BMM (Bit-MatMul) ② BSpMM (Bit-Sparse-Dense-MatMul) ③ ④ Auxiliary Ops. At the high-level, BitGNN provides fused operators for binary or full-precision operand input/output. In the usage examples, "orig" and "bin" suffixes represent the original and binary forms of the GNNs, respectively.**

In this work, we propose three methods to reconcile the incompatibility. Let  $a$  represent a 0/1-based bit-vector of the adjacency matrix, and  $b_{org}$  be a +1/-1-based bit-vector from the activation matrix. Both  $a$  and  $b_{org}$  are represented in 0/1 bits in memory, but for the sake of explanation, we introduce  $b$  to represent the in-memory 0/1 representation of  $b_{org}$ , where 1 corresponds to +1 and 0 corresponds to -1. We now describe the three methods to compute the dot product between  $a$  and  $b_{org}$ .

(1) If-else evaluation on  $a$ 's nonzeros: This method examines each bit of  $a$ . If the value is 1, we add the corresponding bit in  $b$  ( $1 \rightarrow 1, 0 \rightarrow -1$ ) to the temporary sum; otherwise, we skip the bit value in  $b$ .

(2)  $popc(a \& b) - popc(a \& \neg b)$ :  $popc(a \& b)$  accumulates the total number of 1s of  $a \times b$ .  $popc(a \& \neg b)$  ( $\neg b$  represents the complement of  $b$ ) gives the total number of -1s in  $b_{org}$ . Subtracting the two results provides the dot product of  $a$  and  $b_{org}$ .

(3)  $2 \times popc(a \& b) - popc(a)$ : The transformation from +1/-1 to 1/0 involves adding 1 and then dividing by 2 (i.e., right shift). Thus,  $b = (b_{org} + 1)/2$ . Consequently,  $b_{org} = 2 \times b - 1$ . Since  $popc(a \& b)$  is the bit-dot-product of  $a$  and  $b$ , we can compute the dot-product of  $a$  and  $b_{org}$  as  $2 \times popc(a \& b) - popc(a)$ .

If the activation values are in bits, Solution-2 and Solution-3 are more efficient than Solution-1. However, if the activation values are in other forms, Solution-1 may provide better performance. Section 3.4 provides additional discussions on selecting the appropriate method.

### 3.3 R3: How to realize the potential in coding?

The third research question pertains to the effective materialization of BitGNN abstractions to fully leverage the efficiency benefits of binary representations of tensors.

Previous works on binary graph neural networks, such as [18–20], have only simulated binarization using the `sign()` function and FP32 multiplication, without treating values as bits in the implemented operations.

To address this issue, our proposed solution meticulously explores the bit manipulation intrinsics offered by modern GPUs to fully unlock the performance potential of BitGNN. In BitGNN, the core operations are binary matrix multiplication (BMM) and binary sparse matrix multiplication (BSpMM), as illustrated in Figure 2. Both operations have several variants. While previous studies have examined BMM [28, 31], the ones in BitGNN build upon prior work while taking into account various precisions and the fusion of auxiliary operations. However, BSpMM has not been previously studied. Thus, the remainder of this discussion focuses on BSpMM.

**3.3.1 Design Principles.** The BSpMM kernels in BitGNN that use FRDC-based tensors are designed based on the following principles:

(1) *Warp-based workload partition*: We partition each workload unit of a node into one or more warps and utilize fast intra-warp communication [32] on GPUs to its fullest potential.

(2) *Maximizing bit-level parallelism*: This addresses the granularity dilemma mentioned earlier and maximizes the edge traversal throughput (measured in the number of traversed edges per second (TEPS)). We ensure that the small bit-blocks in sparse graphs are ultimately manipulated in a word-aligned fashion.

(3) *Maximizing bit-tensor load & store efficiency*: SpMM is often memory-bound [33, 34], so we must carefully use the memory hierarchy for bit-tensor manipulations to ensure maximum efficiency.

**3.3.2 Implementations.** Following the three principles mentioned earlier, we implement the BitGNN abstractions using the FRDC scheme and bit-manipulation intrinsics. We will explain the implementation of BSpMM.BBB in detail as an example.

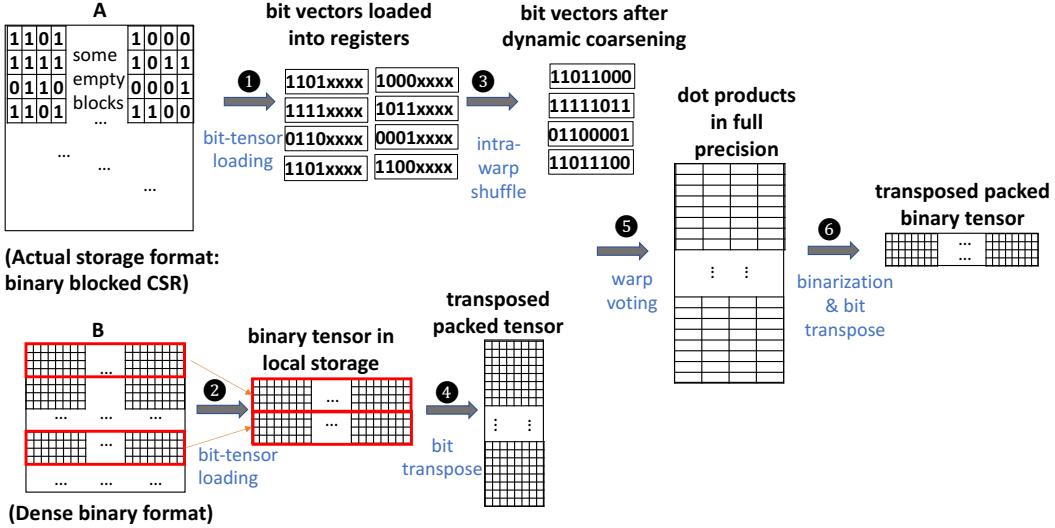


Figure 3: Illustration of the procedure of BSpMM.BBB using FDRC (Fine-Representing Dynamic-Coarsening).

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**Algorithm 1:** BSpMM.BBB

---

**Input:** AdjMat: RowPtr, ColInd, BitTiles, Tile-row ID  $r$ ;  
**Output:** OutActMat $_{(b)}$

- 1  $NT \leftarrow \text{RowPtr}[r+1]-\text{RowPtr}[r]; TS \leftarrow \frac{\text{SIMD\_unit}}{\text{tile\_dim}}$
- 2 **for** each tile set  $t_s$  where  $s = 1$  to  $\lceil \frac{NT}{TS} \rceil$  **do**
- 3   **register**  $A \leftarrow \text{BitTiles}[s]$  for  $s = 0$  to  $TS-1$
- 4   **register**  $B \leftarrow \text{InActMat}_{(b)}[k]$  for  $k = \text{ColInd}[s] \times \text{tileDim} + \{0, 1, 2, \dots, \text{tileDim}-1\}$  and  $s = 0$  to  $TS-1$
- 5   **register**  $a \leftarrow a \mid \text{shfl}(A, s \times \text{tile\_dim} + \text{laneid}) \ll (4 \times (TS-1-s))$  for  $s = 0$  to  $TS-1$  *// do bit-concatenate*
- 6   **shared memory**  $b[warpid \times \lceil \frac{32}{W} \rceil + k] \leftarrow \text{brev}(\text{ballot}(B \gg (31-k) \& 0x1))$  for  $k = 0$  to  $\text{SIMD\_unit}-1$  *// do bit-transpose*
- 7   **register**  $c[n] \leftarrow \text{popc}(\text{shfl}(a, n) \& b[warpid \times \lceil \frac{32}{W} \rceil + \text{laneid}] - \text{popc}(\text{shfl}(a, n) \& \neg b[warpid \times \lceil \frac{32}{W} \rceil + \text{laneid}])$  for  $n = 0$  to  $\text{tileDim}-1$  *// compute bit-dot-product*
- 8   **register**  $rs[n] \leftarrow \text{brev}(\text{ballot}(c[n] \geq 0))$  for  $n = 0$  to  $\text{tileDim}-1$
- 9    $\text{OutActMat}_{(b)}[r \times \text{tileDim} + n] \leftarrow rs[n]$  for  $n = 0$  to  $\text{tileDim}-1$

---

**BSpMM.BBB Algorithm:** In Algorithm 1, we present the implementation of the BSpMM.BBB kernel using the FRDC technique. The binary adjacency matrix is represented using RowPtr, ColInd, and BitTiles (BitBlock)<sup>3</sup>. The algorithm is parallelized through the tile (block) row dimension, and we present tile (block) row  $r$ 's workload.

In Line 1, each tile-row's total number of tiles ( $NT$ ) is divided into several tilesets. The size of a tileset ( $TS$ ) is defined as the number of bit-row required to concatenate into a *SIMD\_unit*, which is equal to  $\frac{\text{SIMD\_unit}}{\text{tile\_dim}}$ . For example, when the adjacency matrix is stored in the block- $4 \times 4$  format with  $4 \times 4$  non-empty tiles, a non-empty tile contains four nibbles (4-bit). When we use 32 as a *SIMD\_unit*, the tileset size ( $TS$ ) equals 8. Consequently, in Line 2, the kernel will process 8 bit-tiles in each iteration. A tileset ( $TS$ ) is the processing

<sup>3</sup>We use the terms "tile" and "block" interchangeably in the paragraphs.

unit of an iteration, and the workload of each tile-row requires  $\lceil \frac{NT}{TS} \rceil$  iterations to accomplish.

In this scenario, both the adjacency matrix ( $A$  in Figure 3) and input activation ( $B$  in Figure 3) are binary, and the resulting output should also be binary. As shown in Figure 3, the algorithm includes the following steps:

Step ① & ②: Warp-based workload partitioning and loading. To efficiently utilize the GPU architecture, each warp of 32 threads is mapped to the computation of a row of  $4 \times 4$  bit-tiles (i.e., 4 nodes when representing the graph in bits). Within each warp, the row of bit-tiles is further partitioned into multiple tile groups, where each tile group contains 8 bit-blocks. For example, if there are ten bit-tiles, there will be two tile groups. The first tile group holds the 0th-7th tiles of that  $4 \times 4$  tile row, and the second tile group holds the 8th and 9th tiles, with the remaining 8 slots padded with zeros.

Next, each iteration processes a tile group as follows: the 32 threads in the warp cooperatively load the 32 uchar<sup>4</sup> from 8 bit-tiles of the sparse bit matrix  $A$  from global memory into registers. Then, the 32 threads load the 8 segments of the input activation  $B$  corresponding to the loaded tiles of  $A$  from global memory into shared memory, forming a consecutive layout, with each word used as a 32-bit vector.

Step ③ On-the-fly assembly via bit-concatenation. In this step, dynamic coarsening is performed to ensure that the bit-tiles of  $A$  are 32-bit aligned. Each of the 0th-3rd threads uses the intra-warp communication intrinsic (`shfl_sync()`) and bit shifting to quickly concatenate the neighbors of each node (in the form of bit-vectors) into a 32-bit unsigned bit-vector (only 8 bits are shown in our illustration in Figure 3).

Step ④ Bit-transpose for column-wise coalesced access. This step involves transposing the column-major packing of  $B$  into row-major. This way, when computing the bit-dot-product with  $A$ , the bits

<sup>4</sup>We store 4-bit unit as an uchar (1 byte) in our original implementation. Storing them in a smaller representation (i.e., int4) is also possible in newer GPU architectures.

can be fetched as bit-columns, and the bit-level parallelism can be fully employed. The transpose is accomplished through bit shifting and masking on the bit-vector of  $B$ . The resulting values are then evaluated and gathered using the intra-warp voting intrinsic, `ballot_sync()`. Finally, the transposition is done using the `brev()` intrinsic.

Step ⑤ Trinary-valued bit-dot-product. In this step, the algorithm computes the bit-dot-product between the 0/1 bit-vectors of  $A$  and the +1/-1 bit-vectors of  $B$ . (“Trinary” for 0/1/-1.) The loop iterates 4 times (once for each node), working on a 32-bit bit-vector from  $A$ . Each of the 32 threads is responsible for computing 1/32 of the bit-dot-product. The products are stored in registers as full-precision values.

Step ⑥ Bit-tensor store. In this step, the temporary full-precision products are packed into the bit format by element-wise evaluation of whether the product is greater than or equal to 0, which is the binarization process of binary activation tensor. The 32 threads in a warp cooperatively evaluate the full-precision values using the intra-warp voting intrinsic (i.e., `ballot_sync()`). The result is then anti-clockwise transposed by the `brev()` intrinsic to complete the bit-vector packing. The output produces 32-bit unsigned bit-vectors of the activation map.

**Other variants** The implementation of other variants of BSpMM follows a similar approach, using bit-level intrinsics for most computations with some differences in handling different precisions. For example, BSpMM.FBB loads the activation tensor differently. In Step ② (bit-tensor load), it requires 4 warps to cooperatively load all the full-precision values. Each thread in a warp is responsible for loading one of the dimensions of the feature vectors of 32 neighbor nodes. Therefore, Step ④ (Bit transpose for column-wise coalesce access) is not required. More details can be found in the supplementary material [35].

### 3.4 Tuning Utilities and Other Implementation Details

To launch our end-to-end model, which contains multiple kernels, we use `cudaLaunchCooperativeKernel()` to enable global synchronization between a specific set of thread blocks [36]. We first calculate the maximum number of blocks that fit each streaming multiprocessor (SM) using `cudaOccupancyMaxActiveBlocksPerMultiprocessor()` and then use 1024 threads per thread block to allow the maximum number of warps to execute on each SM. This ensures that we fully utilize the parallelism available on the GPU and achieve optimal performance.

BitGNN’s tuning utilities provide a convenient way to optimize binary GNNs. As described in the previous sections, BitGNN offers a range of variants to accommodate the different precision requirements of GNN inputs, weights, and outputs. The tuning utilities allow for an auto-tuning run to replace BitGNN function calls with other variants and measure their performance. The type correctness is guaranteed by ensuring that the precision of the output of a predecessor matches that of the input of its successor operation. Furthermore, the tuning utilities enable easy selection of the best solution for reconciling the inconsistency of binary value ranges discussed in Section 3.2.2. Predictors can be developed to anticipate

the optimal variant for a particular GNN and graph. Similar predictors have been extensively studied in other contexts, such as sparse matrix storage formats [37].

## 4 EVALUATION

This section reports the performance of BitGNN. We focus on the following questions: (i) How much speedup can it bring to GNN inferences? (ii) How much memory space can it save? (iii) What are the accuracy-speed tradeoffs when using BitGNN?

### 4.1 Methodology

**GPU Environment:** We evaluate the performance of BitGNN on three NVIDIA GPUs of different architecture generations: GTX 1080 (Pascal), Titan V (Volta), and RTX 3060 Ti (Ampere). Their features are summarized in Table 1. The CUDA version is 11.0. For all experiments, we use the average values of 10 repeated executions.

**Datasets:** Table 2 shows the graphs used for the evaluation. These graphs are commonly used for existing GNN research [23, 25, 26, 38–41] and are also the graphs used in prior binary GNN work Bi-GCN [18], making direct comparisons possible.

**Versions to compare:** We compare our BitGNN versions (of different revisions) with Bi-GCN [18]. As the representative of the state-of-the-art binary GNNs—which all focus on binarization algorithms rather than optimized executions, Bi-GCN uses the full-precision representation of values even though it binarizes the operations in GNNs. Meanwhile, to provide a reference point, we report the performance and accuracy of the original GNNs without binarization. Both the original and Bi-GCN versions are in PyG [22].

**GNNs:** We use four GNNs in our experiments: transductive-GCN [7], inductive-GCN [23], GraphSAGE [23], and GraphSAINT [25, 26]. We choose these GNNs because they are the most popular GNNs, and are the GNNs used in the prior binary GNN study [18] that we compare with.

### 4.2 Results and Analysis

Tables 3, 4, and 5 report the speed (at inference time), accuracy, and space usage of the baselines and the versions of our BitGNN.

Before diving into the results, it is worth mentioning that GNN learning is of two kinds: transductive and inductive learning. In transductive learning, the entire data graph is observed in the learning process, with some nodes labeled and others not. The GNN algorithm tries to iteratively refine the labels of those unlabeled nodes by learning from the entire graph structure and those labeled nodes. In inductive learning, the GNN algorithm learns from some sampled graphs and then tries to predict the labels of the nodes on other sampled graphs.

Among the four GNNs used in prior research [7, 23, 25, 26], *transductive-GCN* is for transductive learning, and the other three GNNs are for inductive learning. The prior work applies *transductive-GCN* to only small datasets (Cora, PubMed, CiteSeer) because large graphs are difficult to be loaded and processed in memory as an entirety as required by transductive GNNs. For the large datasets (Flickr and Reddit), the prior work applies the three inductive GNNs. To allow head-to-head comparisons, our experiments follow the same practice.

**Table 1: GPUs used for evaluation.** Arch refers to GPU architecture generation. CC refers to compute capability. SMs refer to the number of streaming multiprocessors in the GPU. Thrds refer to threads. Shared refers to share memory size. Reg refers to number of registers. Note, "/Block" and "/Thrd" imply the maximum resources per thread block and per thread, respectively.

GPU	Arch	CC	SMs	DRAM	Memory Bandwidth	L1 Cache Size/SM	L2 Cache Size	Warps /SM	Blocks /SM	Thrds /SM	Shared /SM	Shared /Block	Reg /SM	Reg /Block	Reg /Thrd
GTX 1080	Pascal	6.0	20	8GB	320GB/s	48KB	4096KB	64	32	2048	64KB	48KB	64K	64K	255
TITAN V	Volta	7.0	80	12GB	653GB/s	96KB	4608KB	64	32	2048	96KB	96KB	64K	64K	255
RTX 3060 Ti	Ampere	8.0	38	8GB	448GB/s	128KB	4096KB	64	32	2048	164KB	164KB	64K	64K	255

**Table 2: Graph datasets used for evaluation.**

Dataset	#Nodes	#Edges	#Features	#Classes
<b>Cora</b>	2,708	13,264	1,433	7
<b>Pubmed</b>	19,717	108,356	500	3
<b>Citeseer</b>	3,327	12,431	3,703	6
<b>Flickr</b>	89,250	899,756	500	7
<b>Reddit</b>	232,965	114,615,892	602	41

**Table 3: Evaluation results of transductive GCNs.** FP32 is the vanilla GCN [7]. "FP32 (S)" refers to the PyG scatter-gather abstraction with maximal batch size. "FP32 (T)" refers to the PyG SpMM tensor abstraction. Bi-GCN [18] is the state-of-the-art binary GCN implementation. We compare the version that binarizes both activations and weights in the MM operation. "Ours (full)" refers to the *full-precision aggregation*. "Ours (bin)" refers to the *binary aggregation* version that uses MM.FBB + BSpMM.BBB for the first layer and MM.BBF + BSpMM.FBF for the second layer. "Peak Mem" refers to peak memory usage during inference. "Acc" refers to accuracy in percentage (%).

Dataset	Model	Peak Mem (B)	Acc (%)	End-to-end Time (ms)		
				GTX1080	TitanV	RTX3060Ti
<b>Cora</b>	FP32 (S) [7]	16.73M	81.4±0.4	1.25±0.01	0.91±0.03	1.00±0.01
	FP32 (T) [7]	16.73M	81.4±0.4	1.34±0.02	1.15±0.05	1.16±0.03
	Bi-GCN [18]	16.73M	81.2±0.8	1.84±0.04	1.91±0.02	1.57±0.02
	<b>Ours (full)</b>	1.37M	81.2±0.8	0.51±0.00	0.37±0.07	0.38±0.02
	<b>Ours (bin)</b>	0.73M	81.2±1.0	0.32±0.04	0.28±0.08	0.24±0.04
<b>PubMed</b>	FP32 (S)	48.71M	79.0±0.3	2.86±0.04	1.51±0.02	1.90±0.02
	FP32 (T)	48.71M	79.0±0.3	2.26±0.01	1.49±0.02	1.77±0.01
	Bi-GCN	48.71M	78.2±1.0	2.81±0.07	2.23±0.09	1.52±0.01
	<b>Ours (full)</b>	7.31M	78.2±1.0	2.29±0.05	0.84±0.05	1.14±0.00
	<b>Ours (bin)</b>	2.65M	78.1±1.1	0.74±0.04	0.33±0.05	0.44±0.01
<b>CiteSeer</b>	FP32 (S)	49.78M	70.9±0.5	2.60±0.03	1.43±0.04	1.74±0.01
	FP32 (T)	49.78M	70.9±0.5	2.70±0.01	1.56±0.01	1.88±0.05
	Bi-GCN	49.78M	68.8±0.9	2.44±0.00	2.22±0.04	1.33±0.09
	<b>Ours (full)</b>	2.56M	68.8±0.9	0.80±0.04	0.58±0.02	0.50±0.03
	<b>Ours (bin)</b>	1.77M	68.7±0.4	0.63±0.03	0.46±0.01	0.42±0.00

The proposed flexible programming abstraction (Section 3.1.2) can easily facilitate the user's binary network development. With it, we tune the various binarization precisions and identify some model variants that perform relatively well: *full-precision aggregation* (the same as in Bi-GCN [18]) and *binary aggregation* (Use MM.FBB + BSpMM.BBB for the first layer and MM.BBF + BSpMM.FBF for the second layer). They are represented as *Ours (full)* and *Ours (bin)* in the result tables.

**Transductive case:** From Table 3, we have the following observations. (i) Both versions of BitGNN can keep most of the accuracy.

The largest loss of the average accuracy is 0.2%, 0.9%, and 2.2% on the three datasets, respectively. The largest accuracy loss (2.2%) happens on *CiteSeer*, where the normalization of edge weights has a more significant impact. (ii) Both versions can save memory usage significantly, 7–19X by *Ours (full)* and 18–28X by *Ours (bin)*. (iii) Both versions consistently show significant speedups across GPU models: 1.2–5X by *Ours (full)* and 4–7X by *Ours (bin)*. (iv) Because the previous binarized GNN (Bi-GCN) does not use a single bit but a word for a binarized value, it does not save space or time compared to the original full-precision GNNs. (v) Our more complete binarized version (*Ours (bin)*) achieves 2–3X extra space savings and 1.5–3X extra speedups than our version (*Ours (full)*) that uses full-precision aggregation, while the extra accuracy loss is only 0.1%. (vi) All those benefits are largely consistent across the datasets. One exception is the performance of *Ours (full)* on *PubMed*, where, *Ours (full)* shows modest speedups on *GTX1080* and *RTX3060Ti* over the original version while *Ours (bin)* still shows substantial speedups. We attribute this to the relatively larger `num_of_nodes` that introduces large performance gaps between BSpMM.BBB and BSpMM.FBB for the first layer.

**Inductive case:** Tables 4 and 5 report the results of the three inductive GNNs on the two large datasets. The benefits are also significant in space and time, but there are some differences from those in the transductive case. We note the following points. (i) For inductive learning, the previous work [23] uses the F1-micro score rather than accuracy to measure the quality of the inferences. The F1-micro score is a combined metric of precision and recall [23, 42]. The binarization maintains most of the quality again, causing a 0.5–2.1% accuracy loss. (ii) The memory space savings are 1.72–16X. The savings are not as much as the savings in the transductive case. The reason is that most of our space savings come from the bit representation of the values of the adjacency matrices and the node features. But the sparse representation also consists of indices of the non-empty tiles. Because most non-empty tiles contain only one non-zero value, we do not save much on the indexing data structures compared to the default CSR format. For the small graphs, the indexing data structures form only a small portion of the overall representation; but for large graphs, the portion becomes much larger. But the savings are still substantial. (iii) The speedups achieved by our versions are even more significant, ranging from 2X to 125X. The reason is that as the graphs become larger, the room for time savings also grows. Another benefit worth mentioning is that as the memory space usage is reduced substantially, the new method can load the entire graph into memory and produce the inferences of all the sampled subgraphs in one run, which can bring extra time savings than processing the subgraphs one by one.

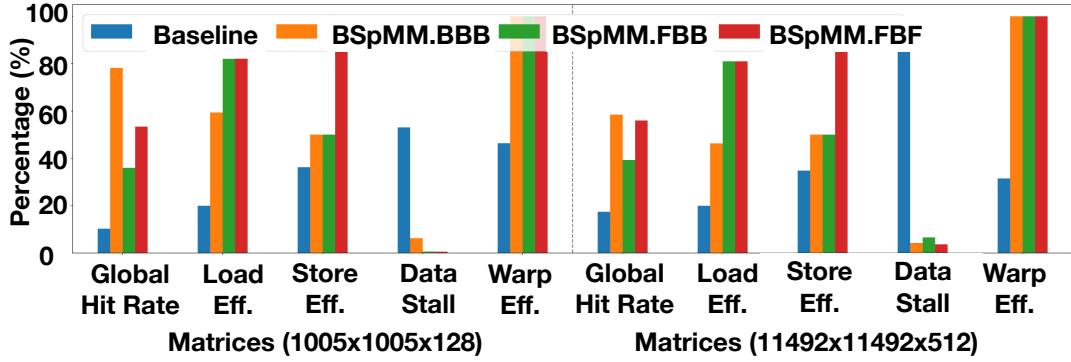


Figure 4: The profiling results of the multiplications of two pairs of sparse matrices on Nvidia GTX1080 GPU.

Table 4: Evaluation results of inductive GNNs – inductive GCN and GraphSAGE [23]. F1-micro is the metric to measure the accuracy of inductive GNNs. The *hidden size* is 256 for Flicker; 128 for Reddit. To avoid out-of-memory error, FP32 and Bi-GCN inferences are set to their maximal batch size on different GPUs.

Dataset	Model	Inductive GCN						Graph SAGE						
		Peak Mem (B)	F1-micro	End-to-end Time (s)			Peak Mem (B)	F1-micro	End-to-end Time (s)			GTX1080	TitanV	RTX3060Ti
				GTX1080	TitanV	RTX3060Ti			GTX1080	TitanV	RTX3060Ti			
Flicker	FP32 (S) [23]	358.07M	50.9±0.3	0.36±0.005	0.33±0.007	0.32±0.009	448.37M	50.9±1.0	0.36±0.006	0.32±0.004	0.32±0.008			
	FP32 (T) [23]	358.07M	50.9±0.3	0.045±0.000	0.035±0.000	0.03±0.000	448.37M	50.9±1.0	0.045±0.001	0.035±0.000	0.034±0.000			
	Bi-GCN [18]	358.07M	50.2±0.4	0.36±0.007	0.34±0.010	0.34±0.011	448.37M	50.2±0.4	0.36±0.008	0.33±0.003	0.33±0.002			
	<b>Ours (full)</b>	107.07M	50.2±0.4	0.023±0.01	0.016±0.000	0.02±0.003	196.9M	50.2±0.4	0.038±0.007	0.027±0.00	0.03±0.006			
Reddit	<b>Ours (bin)</b>	22.38M	49.9±0.3	0.006±0.004	0.002±0.000	0.005±0.000	27.52M	50.8±0.1	0.008±0.008	0.003±0.00	0.006±0.001			
	FP32 (S)	1.67G	93.3±0.0	49.01±0.25	38.19±0.10	38.70±0.28	1.81G	95.3±0.1	49.27±0.18	37.95±0.35	38.29±0.22			
	FP32 (T)	1.67G	93.3±0.0	0.86±0.02	0.45±0.001	0.52±0.007	1.81G	95.3±0.1	0.92±0.001	0.51±0.001	0.52±0.002			
	Bi-GCN	1.67G	93.1±0.2	49.30±0.28	38.22±0.10	38.97±0.34	1.81G	95.3±0.1	49.42±0.21	38.05±0.56	39.03±0.11			
<b>Ours (full)</b>	1.02G	93.1±0.2	0.82±0.02	0.38±0.08	0.45±0.03	1.17G	95.3±0.1	0.90±0.003	0.45±0.03	0.53±0.04				
	<b>Ours (bin)</b>	943.77M	92.8±0.1	0.49±0.11	0.15±0.007	0.27±0.12	983.77M	91.2±1.2	0.53±0.05	0.20±0.009	0.29±0.05			

Table 5: Evaluation results of inductive GNNs – GraphSAINT [25, 26]. The *hidden size* is 256 for Flicker; 128 for Reddit.

Dataset	Model	Peak Mem (B)	F1-micro	End-to-end Time (s)		
				GTX1080	TitanV	RTX3060Ti
Flicker	FP32 (S) [25, 26]	623.72M	51.1±0.1	0.39±0.004	0.36±0.003	0.34±0.006
	FP32 (T) [25, 26]	623.72M	51.1±0.1	0.05±0.000	0.03±0.000	0.04±0.000
	Bi-GCN [18]	623.72M	50.8±0.2	0.05±0.003	0.04±0.000	0.04±0.001
	<b>Ours (full)</b>	371.83M	50.8±0.2	0.15±0.004	0.07±0.00	0.09±0.001
Reddit	<b>Ours (bin)</b>	202.39M	49.6±0.8	0.023±0.007	0.012±0.00	0.016±0.001
	FP32 (S)	2.04G	96.6±0.1	48.79±0.23	38.41±0.32	39.77±0.22
	FP32 (T)	2.04G	96.6±0.1	1.25±0.005	0.60±0.001	0.69±0.003
	Bi-GCN	2.04G	95.7±0.1	1.27±0.002	0.61±0.003	0.73±0.011
<b>Ours (full)</b>	1.39G	95.7±0.1	0.92±0.46	0.66±0.08	0.74±0.08	
	<b>Ours (bin)</b>	1.18G	94.5±0.6	0.45±0.16	0.24±0.003	0.33±0.09

Additionally, Table 4 shows a 4.1% accuracy loss on GraphSAGE-Reddit. We attribute this to the sensitivity of the originally-trained binary GraphSAGE and the small hidden size used. While the Reddit graph is significantly larger than Flicker, it only uses as few as 128 hidden nodes. Increasing the hidden nodes to 256 and 512 results in a smaller accuracy loss (~0.67%, ~0.9%). On Flicker, there is even an 0.6% accuracy increase. GNN inference accuracy is unstable, especially on large graphs, which is not unique to GNNs. Studies have shown that a compressed DNN can sometimes achieve higher

accuracy than the original. Our slight accuracy increase resulted from the binary aggregation approximation in the first GCN layer.

Table 5 reports the results on GraphSAINT. For this GNN, patterns of the two graphs (only one non-zero in most non-zero tiles) favor tensor kernel-based implementations. Ours (bin) still achieves consistently substantial speedups across the architecture and the datasets. It benefits from our implementation that loads only the elements corresponding to non-zero elements in the tile. The space savings are still substantial.

**Hardware profiling:** Using the GPU vendor’s profiling tool NSight, we find that the performance gain mainly originates from improved memory utilization through binarization. Figure 4 shows the profiling results of three of our BSpMM kernels compared to the baseline—the default SpMM kernel in Torch Sparse when computing the multiplications of two pairs of representative matrices, measured on Nvidia GTX1080 GPU. Specifically, we observe significantly enhanced global load/store efficiency (from 19% to 80%), and L1/Tex cache hit rate (from 10% to 53–78%). In addition to that, with the data request stalls reduced from 53–89% to less than 10%, the warp execution efficiency surges from 31–46% to almost 100%.

**Discussions:** Regarding the overall number of operations to be executed, although BitGNN aggregates the multiply-accumulate operations of 32 elements into a single bit-dot-product operation upon one 32-bit operand, the actual reduction in operation count is

less than 32X due to extra overhead on indexing. Nevertheless, since SpMM is typically memory-bound, binarization can still contribute to significant performance improvement.

**Potential impact:** The reduced space and time brought by BitGNN not only improves the computing efficiency on server GPUs, but also opens new opportunities for dealing with large graphs (which cannot fit into memory) and for GNN to be used on resource-constrained devices. Quantized (non-GNN) deep neural networks have already been adopted in many domains on resource-constrained embedded scenarios, including auto-driving [43], smart agriculture [44], COVID19 face-cover detection [45], 3D object detection [46] and image processing [47]. This is mainly due to the simplified logic [48], low energy cost [49], low hardware requirement, and robustness [50]. Nevertheless, there are many scenarios the input data are non-Euclidean or can be better expressed by graphs, such as molecules [51], traffic flow [52], power-grid [53], etc. In these scenarios, the binary graph neural network, as a replacement of BNN, can play a vital role in feature extraction and real-time prediction.

## 5 RELATED WORKS

*Binary Graph Neural Network.* Binary GNNs have recently gained attention as a promising approach for applying quantization to graph learning workloads in the ML community. Despite several works proposing GNN binarization techniques and/or binary GNN models [18–21], none of them have demonstrated the full performance advantages that can be achieved through binarization, which is where BitGNN comes in. Here, we summarize some of the existing binary GNN studies.

Binary Graph Convolutional Network (Bi-GCN) [18] proposes a novel binary gradient approximation-based back-propagation technique for effectively training binary GCNs. It binarizes both the network parameters and node features with minimal accuracy loss. Bi-GCN has been applied to both transductive-learning GNNs (e.g., GCN [7]) and inductive-learning GNNs (e.g., inductive-GCN, GraphSAGE [23], and GraphSAINT [25, 26]). Alternatively, Bahri et al. [19] use knowledge distillation and multi-stage training to binarize the EdgeConv in Dynamic Graph CNNs (DGCNN) [5]. Wang et al. [20] propose a new binarized graph embedding method, named BGN, to binarize the parameters and pre-activations of Adaptive Sampling (AS-GCN) [54] and Graph Attention Network (GAT) [55]. In the back-propagation phase, they use two popular unbiased gradient estimators – the straight-through estimator and REINFORCE estimator [56] – for binary approximation. Aside from XNOR and population count for +1 and -1 bit calculation, they involve masked summation and balance functions to improve the binarization process. Meta-Aggregator [21] introduces two aggregators – the Greedy Gumbel Aggregator (GNA) and Adaptable Hybrid Aggregator (ANA) – aiming at enhancing the binary training accuracy during the aggregation phase.

While these binarization techniques for GNNs provide a stepping stone in exploring the potential of binary GNNs, they only "logically" binarize GNN at the algorithm level, and their implementations still use `sign()` and `mm()` in PyTorch, which essentially adopt full-precision tensors for storage and full-precision operations for computation at the lower level. As a result, they fail to showcase the performance potential of binary GNNs.

*Bit-Manipulation on GPUs.* Previous research has extensively explored the potential of leveraging bit operations on modern GPUs across a wide range of application scenarios. These include image classification using CNNs [14, 28, 31, 57, 58], depth-sensing with stereo vision [43, 59], fraud detection [60], and graph algorithms [30].

Courbariaux et al. [14] first introduce the concept of using XOR and population-count operations for small MLPs on GPUs. Espresso [57] builds a binary CNN library with C and CUDA backends, providing bit-packing and bit matrix multiplication functions. Khan et al. [58] extend the previous GEMM-based CNNs for real-time vehicle classification on desktop and embedded GPUs. BSTC [28] presents bit-block-based kernel designs for BMM and BConv, scaling the significant performance gains to deeper binary AlexNet, VGGNet, and ResNet. StereoBit [43] and FastFusion [59] develop BNN-based stereo matching networks with optimized implementations to reduce GPU on-chip memory footprint. They construct the network with binary feature descriptors for image pairs and weights, replacing expensive full-precision arithmetic operations with XOR and population count operations. Ye et al. [60] leverage the GPU intrinsics `__ballot_sync()`, `__match_any_sync()`, and `__popc()` to construct a Label Propagation (LP) algorithm for the fraud detection pipeline. Feng et al. [61] decompose quantized neural network matrix multiplications into batches of BMM operations and relied on the Ampere tensor cores for acceleration. Finally, Bit-GraphBLAS [30] proposes a sparse bit storage format and binary implementation of GraphBLAS operators to accelerate iteration-based graph algorithms when the graph edges are homogeneous and can be expressed as binary graphs.

These prior studies demonstrate the performance benefits of utilizing bit manipulations and operations on GPUs. However, they are not comprehensive enough to address the specific challenges that arise when dealing with binary GNNs, such as the need for operator restructuring, appropriate tensor representation, and inconsistent value multiplications.

## 6 CONCLUSION

BitGNN is the first work to comprehensively address the design and challenges of implementing binary GNNs using bit tensors and manipulations. Our proposed programming abstractions, tensor representation, and kernel design techniques maximize the performance of binary GNN models end-to-end. The optimizations and implementations provide a remarkable 8-22X acceleration in the end-to-end model performance compared to prior binary GNN implementations.

## ACKNOWLEDGEMENT

This material is based upon work supported by the U.S. Department of Energy (Office of Advanced Scientific Computing Research) under Award Numbers DE-EE0009357 and 78284, as well as work supported by the National Science Foundation (NSF) under Grant No. CNS-2107068. Any opinions, findings, and conclusions or recommendations expressed in this material are those of the authors and do not necessarily reflect the views of NSF or DOE.

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