A 10ns Delay Range 1.5GHz BW True-Time-Delay Array-Based Passive-Active Signal Combiner with Negative-Cap Stabilized RAMP for Fast Precise Localization

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***Abstract*— Maximizing gain in beamforming arrays for emerging communications-on-the-move applications is key in highly resilient networks. Recent studies have demonstrated the rainbow beamtraining method as an effective solution for spatio-spectral mapping in analog/hybrid arrays but require large delay-bandwidth products. In this work, a proof-of-concept 2-channel 1.5GHz bandwidth 10ns maximum delay spatial signal processor is proposed. The angle-of-arrival estimation error is significantly reduced to ±1.5° compared to prior implementations with a smaller delay range. Multi-stage buffer-less switched-capacitor array enables large delay-bandwidth product of 15. A passive-active amplifier-based combination scheme supports the wideband operation minimizing power and distortion. A negative-capacitance compensated ring-amplifier with stabilization is proposed as part of the wideband signal combiner. The 2-channel system consumes 37.3mW/channel and 0.45mm^2 in 65nm CMOS.**

***Keywords*— rainbow beamtraining, negative-capacitance, wideband RAMP, delay range, true-time-delay arrays.**

I. Introduction

Joint communication-sensing protocols at millimeter-wave (mmW) and sub-THz are highly reliant on beamtraining (BT) to realize the optimal gain at all times. As illustrated in Fig. 1, frequency-dependent beam probing, hereby called rainbow-BT, has been proven as a fast and energy-efficient [1], [2] method for probing multiple directions simultaneously. The rainbow-BT uses true-time-delay (TTD) arrays enabling a single-shot spatio-spectral mapping exploiting beam squint [1]–[4]. Integrated leaky-wave antenna [3] enables spatio-spectral mapping at sub-THz but is less scalable to lower mmW occupying a significantly large area. In [1], fast angle-of-arrival (AoA) estimation was studied for a linear array that shows that the AoA estimation accuracy is a strong function of diversity order, number of elements, and bandwidth. Equivalent hardware demonstrations of rainbow-BT were shown in [2], [4], [5] with a single-stage switched-capacitor array (SS-SCA). The SS-SCA with digitally-controlled delay compensation [6] is advantageous as compared to other delay lines like T-line, g_m-C all-pass filter, and digital delay units due to its balanced performance of area/power, delay range, and resolution [2]. The discrete-time delay unit in the SS-SCA that exploits beam-squint effect required for rainbow-BT had an overhead of $< 3\%$ in power consumption. However, a delay-BW product of only

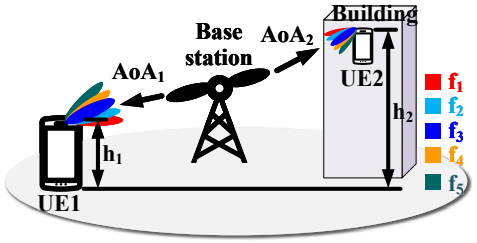

Fig. 1. Wideband comms between user element (UE) and base station.

3 limited the angle-of-arrival (AoA) estimation accuracy to 10° [4]. As the need for a larger delay in a higher bandwidth system arises, the SS-SCA suffers from considerable signal leakage and stringent settling time requirements. A multi-stage (MS-SCA) architecture first proposed in [7] can achieve larger delay ranges, breaking the fundamental delay-BW trade-off. However, only a single-element was demonstrated and inter-element delay compensation with wideband analog combining was not considered. The analog combining is particularly challenging with increasing signal BW and interleaving levels required to achieve larger delay ranges. Ring-amplifiers (RAMPs) could overcome the limitations above but are constrained by stability issues.

This work proposes a proof-of-concept 2-element 1.5GHz BW rainbow-BT array with up to 10ns reconfigurable delay range compensation. The significantly improved delay-bandwidth product realizes state-of-the-art AoA accuracy of $< 1.5°$ with only 74.6mW core power and 0.45mm^2 area in 65nm CMOS that validates the theoretical foundations in [1]. Key specific contributions are:
1) Low-power buffer-less multi-stage SCA architecture;
2) Active-passive hybrid signal combination scheme leveraging power and linearity performance;
3) Highly-digital clock generator design with reconfigurable delay compensation and leakage reduction; and
4) High-speed RAMP as active signal combiner with stabilization and passive common-mode-feedback (CMFB) network for wideband operation.

The rest of the paper is organized as follows. Section II explains the proposed system design. Circuit implementation is detailed in Section III, followed by measurements in Section IV. Section V concludes this paper.

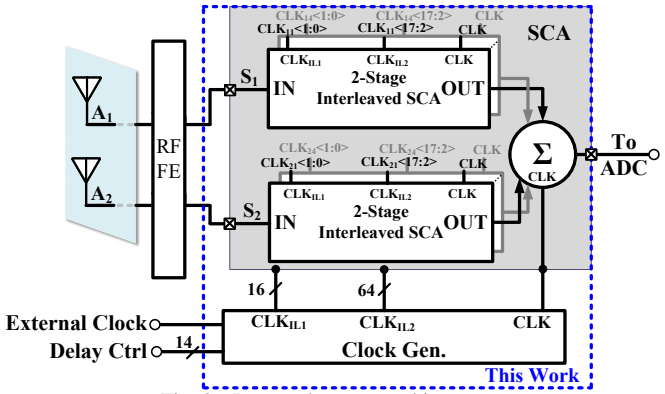

Fig. 2. Proposed system architecture.

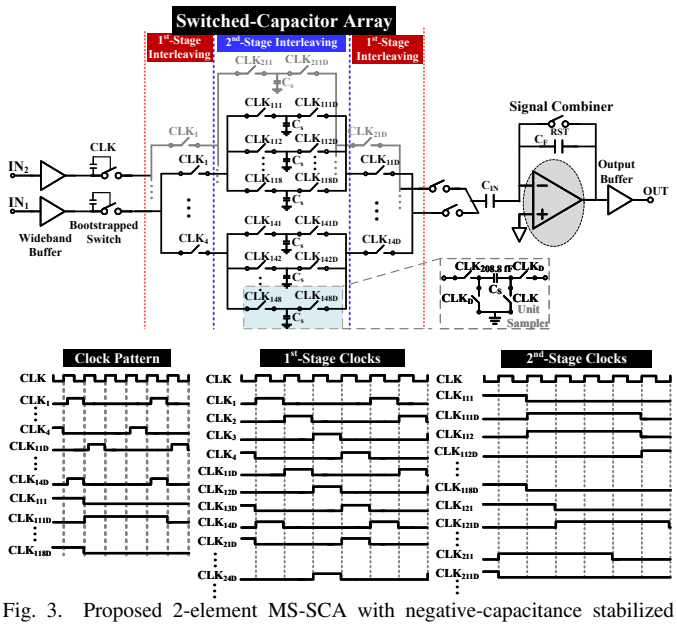

Fig. 3. Proposed 2-element MS-SCA with negative-capacitance stabilized RAMP for wideband analog combining.

II. Proposed System Implementation

We note that for high precision rainbow-BT a large delay range is required in hardware [1]. Fig. 2 shows the simplified system architecture. The proposed system consists of 3 main parts: MS-SCA, signal combiner, and clock generator. The MS-SCA and the signal combiner process the input signals with different delay, and combine signals from different channels. Fig. 3 presents the signal processing chain with more details. Time-interleaving SCA is used to extend delay range [6]. However, the basic SS-SCA [8] (Fig. 4(a)) suffers from timing skew and signal leakage as the interleaving levels are increased. In [7], MS-SCA was proposed to relax the timing requirement for large interleaving levels (Fig. 4(b)). The clock signals of the second stage overlap with those of the first stage, leading to a timing skew-insensitive design. In this work, we implement a buffer-less SCA to reduce power consumption and also minimize area (Fig. 4(c)). However, the buffer-less SCA comes at the cost of increased gain loss. A hybrid passive- and active-signal summation scheme is thus proposed to compensate for the gain loss induced in the MS-SCA (Fig. 3). The passive summation processes the signal

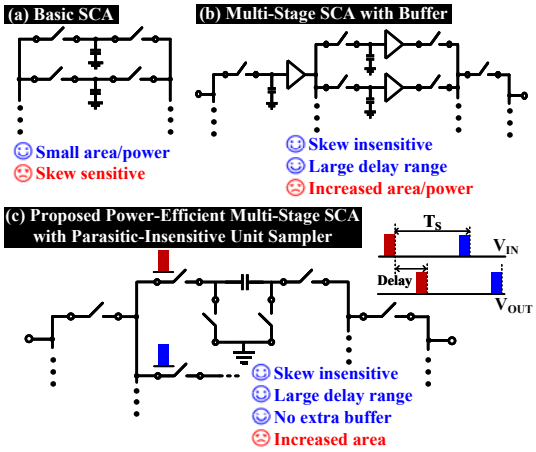

Fig. 4. Comparison of 3 different SCA architectures.

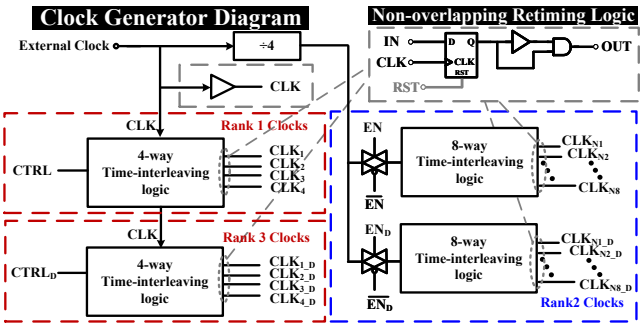

Fig. 5. Clock generator diagram.

information during phase 1 (CLK), followed by amplification and active summation in phase 2. SCA sampler charges are transferred into RAMP input capacitor C_{in}: $N \times C_s \times \Delta V_{C_s} = C_{in} \times \Delta V_{in}$, N=2 denotes the number of channels and ΔV_{C_s} is the voltage difference across sampling cap C_s. By adjusting the RAMP input capacitance, the bandwidth and gain limitation of the amplifier are also relieved: $\omega_u \geq 2 \times ln(2) \times N \times (R+1) \times f_s$, where ω_u is the unity-gain bandwidth, R is the ADC resolution, and f_s is the sampling frequency. Passive combination is inherently linear but suffers due to charge sharing. This is partly compensated using a low-power RAMP improved from [9] in section III.

III. Circuit Implementation

A. Clock Generator: A simplified clock design diagram is shown in Fig. 5. Delay is controlled by generating different start-up timing using DFFs and external digital control codes. A non-overlapping retiming logic block is used before each stage's output phases to avoid signal leakage within the same interleaving level SCA. The integrated clock generator provides multiple duty cycle clocks: 50% at 3 GHz for input sampler, 25% for Stage 1 at 750 MHz; 12.5% for Stage 2 clocks at 93.75 MHz. Fig. 6 illustrates the maximum delay case where one channel is delayed by one sampling period while the other channel is set to maximum delay.

B. Negative-Capacitance Compensated RAMP with Gain Boost: To compensate for the passive combination loss, a RAMP-based signal combiner is used. In [9], a dead-zone degenerated RAMP was demonstrated with improved gain

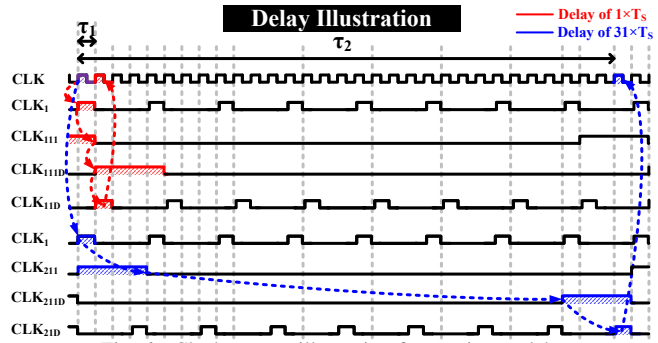

Fig. 6. Clock pattern illustration for maximum delay.

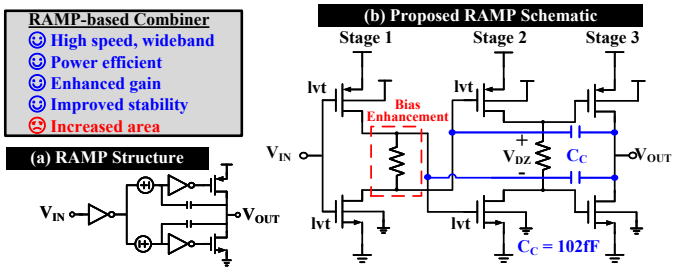

Fig. 7. Proposed (a) ring-amplifier (RAMP) cell and (b) its schematic with gain boost and negative capacitance compensation.

performance. For wideband operation, the RAMP stability is affected, leading to poor settling. To improve stability in the RAMP-based summer adding two antenna inputs, a negative capacitance compensation with gain boost RAMP scheme is proposed (Fig. 7(a)). The compensation shown in detail in Fig. 7(b) helps in the following two ways: (1) reduce the input capacitance of the second RAMP stage as the equivalent Miller capacitance at node A is negative; and (2) the output capacitance of the RAMP cell is increased due to the Miller cap at the output node. As a result, phase margin is increased, and the proposed RAMP is stabilized with a large bandwidth, as illustrated in Fig. 8. A resistive gain boost technique is further implemented to help improve the RAMP gain. We also apply resistive CMFB in the RAMP (Fig. 9) that does not require an extra reset phase in the delay compensation for the MS-SCA as compared to [6]. This enhances the maximum delay range feasible by an additional $0.5T_s$ ($T_s = 1/f_s$).

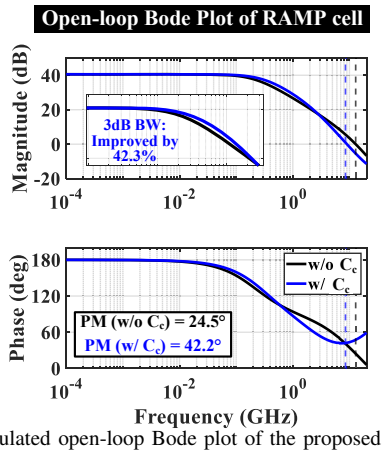

Fig. 8. Simulated open-loop Bode plot of the proposed RAMP cell.

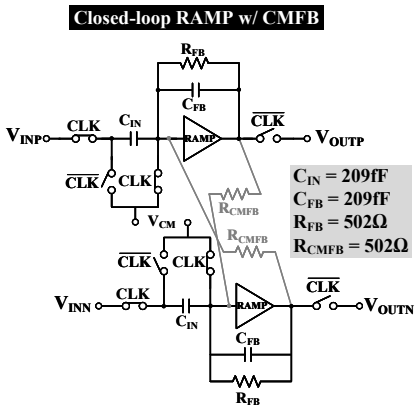

Fig. 9. Closed-loop RAMP configuration with resistive CMFB.

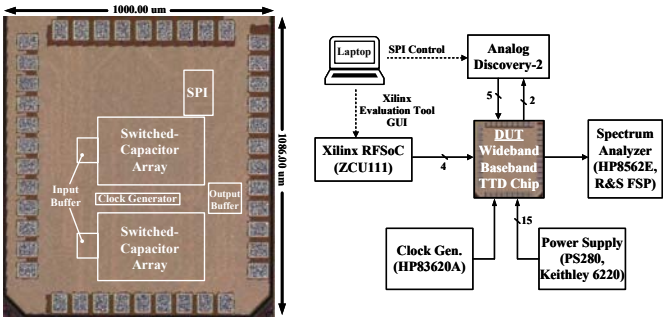

Fig. 10. (left) Die photo. (right) Testbench setup.

IV. Measurement Results

The proposed design is fabricated in a 65nm CMOS process occupying 1.086mm^2, with a core area of 0.45mm^2 and core power of 74.62mW (excluding test buffers). The test setup is shown in Fig. 10. MATLAB-generated test data is applied to the DUT (chip-on-board) using high-speed Xilinx ZCU111 DACs with the DUT output captured by R&S spectrum analyzer. Clocks and other biases, as well as on-chip serial peripheral interface (SPI) providing digital delay control codes, are shown in Fig. 10.

Fig. 11 presents the measured spectrum with interleaving spurs removed. The clock interleaving spurs are static by nature and below 3rd-harmonics tones. Thus it is reasonable to have post-processing remove interleaving spurs. Measured single-tone results show an SFDR of 40dB at low frequency and 33dB near Nyquist (with post-processing in the RFSoC).

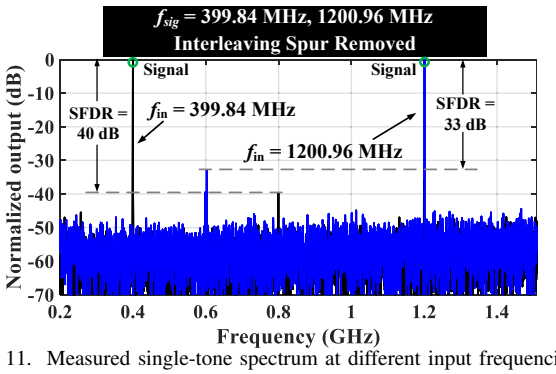

Fig. 11. Measured single-tone spectrum at different input frequencies.

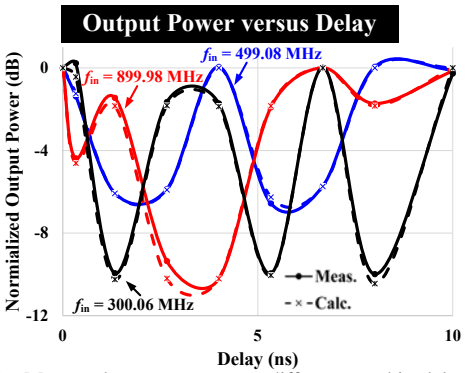

Fig. 12. Measured output power vs. different on-chip delay settings.

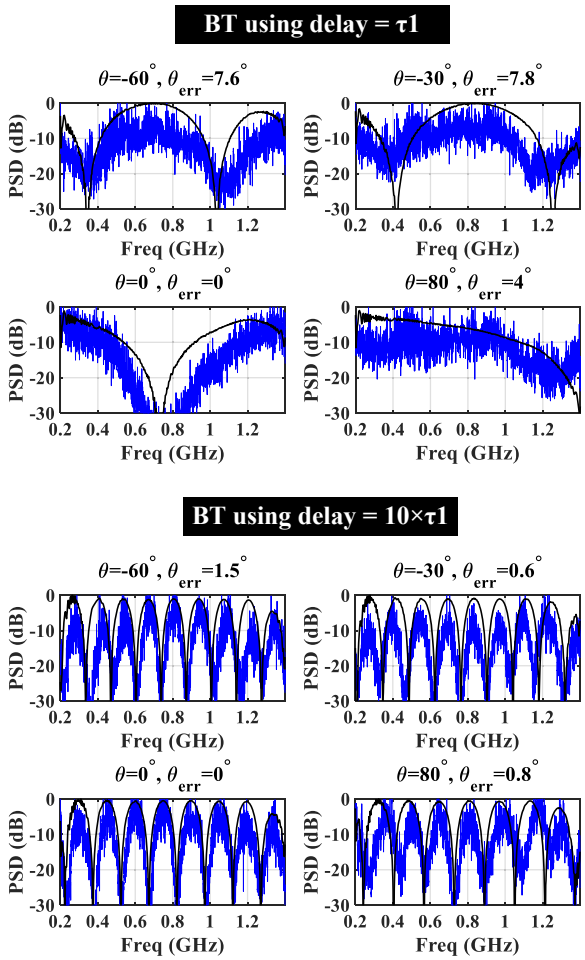

Fig. 13. Measured norm. rainbow-BT spectrum (blue) with different delay and aperture vs. theoretical (black). $\tau_1 = 0.67$ns on-chip delay.

Fig. 12 shows the combined 2-channel output with different delays between the two channels for three different single-tone inputs. The measured curves match the theoretical estimates, proving that on-chip delay can be precisely tuned within the 10ns range. With the ability to control the delay, BT power spectrum density (PSD) has been measured with delays set to 1/BW and 10/BW for a 1.5GHz chirp applied from ZCU111 in Fig. 13. As illustrated, the angle estimation error range has reduced dramatically from $\pm 7.8°$ to $\pm 1.5°$, proving that a 10X increased delay range increases BT accuracy.

Table 1. Comparison Table

	This Work	[4]	[6]	[3]	[10]
Function	BF/BT	BF/BT	BF	BF/BT	BF/BT
Tech.	65nm CMOS	65nm CMOS	65nm CMOS	65nm CMOS	45nm SOI CMOS
Delay Method	Time-interleaved multi-stage switched-cap	Time-interleaved switched-cap	Time-interleaved switched-cap	On-chip leaky-wave antenna	Time-interleaved multi-stage switched-cap
# of Channels	2	2×2	4	2	1
Freq. Range (GHz)	DC-1.5	DC-0.8	DC-0.5	360-400	0.2-2
Max Delay (ns)	10	3.8	1	N/R	448.6
Delay Range × BW	15	3.04	0.5	N/R	897.2
AoA Accuracy	±1.5°	±11.2°	N/R	±0.95°	N/A
IIP3 (dBm)	17.5-18	14	7.9	N/R	N/R
Area Effici. (ns/mm^2)	22	12.6	26.3	N/R	330
Pdc/Channel (mW)	37.3	29	40	163	74
Core Area (mm^2)	0.45	1.98	0.82	3	1.36

V. Conclusions and Future Works

This work demonstrated a spatial signal processor with an on-chip integrated delay range of 10ns supporting 1.5GHz bandwidth for wideband communications-on-the-move and fast BT applications. Table 1 compares state-of-the-art beamformers with integrated BT. In contrast to [7], this work achieves higher power efficiency with less delay while combining several channels. In [8], SS-SCA architecture is used for delay compensation but with a smaller signal bandwidth and hence a smaller delay-bandwidth product. The larger delay-bandwidth product in this work shows state-of-the-art accuracy with one of the lowest reported areas per channel. Further research will investigate simultaneous communication and training.

Acknowledgments

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References

[1] V. Boljanovic *et al.*, "Fast beam training with true-time-delay arrays in wideband millimeter-wave systems," *IEEE TCAS-1*, pp. 1727–39, 2021.
[2] C. C. Lin *et al.*, "Multi-mode spatial signal processor with rainbow-like fast beam training and wideband communications using true-time-delay arrays," *IEEE JSSC*, pp. 3348–3360, 2022.
[3] H. Saeidi *et al.*, "Thz Prism: One-shot simultaneous localization of multiple wireless nodes with leaky-wave THz antennas and transceivers in CMOS," *IEEE JSSC*, pp. 3840–3854, 2021.
[4] Q. Xu *et al.*, "A switching-less true-time-delay-based beam probing approach for ultra-low latency wireless communications: System analysis and demonstration," *IEEE TCAS-II*, pp. 4113–4117, 2022.
[5] C. C. Lin *et al.*, "A 4-element 800MHz BW 29mw true-time-delay spatial signal processor enabling fast beam-training with data communications," in *IEEE ESSCIRC*, 2021, pp. 287–290.
[6] E. Ghaderi *et al.*, "An integrated discrete-time delay-compensating technique for large-array beamformers," *IEEE TCAS-1*, pp. 3296–3306.
[7] T. Forbes *et al.*, "A 0.2–2GHz time-interleaved multistage switched-capacitor delay element achieving 2.55–448.6ns programmable delay range and 330ns/mm^2 area efficiency," *IEEE JSSC*, pp. 2349–59.
[8] A. Nagulu *et al.*, "A full-duplex receiver with true-time-delay cancelers based on switched-capacitor-networks operating beyond the delay–bandwidth limit," *IEEE JSSC*, vol. 56, no. 5, pp. 1398–1411, 2021.
[9] J. Lagos *et al.*, "A 1-GS/s, 12-b, single-channel pipelined ADC with dead-zone-degenerated ring amplifiers," *IEEE JSSC*, pp. 646–658, 2019.
[10] T. Forbes *et al.*, "A 0.2-2 GHz time-interleaved multi-stage switched-capacitor delay element achieving 448.6 ns delay and 330 ns/mm2 area efficiency," in *IEEE RFIC*, 2022, pp. 135–138.