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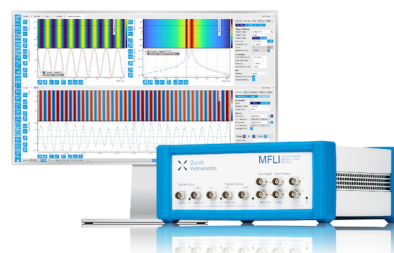
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Continuously tunable uniaxial strain control of van der Waals heterostructure devices **EP**

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ABSTRACT

Uniaxial strain has been widely used as a powerful tool for investigating and controlling the properties of quantum materials. However, existing strain techniques have so far mostly been limited to use with bulk crystals. Although recent progress has been made in extending the application of strain to two-dimensional van der Waals (vdW) heterostructures, these techniques have been limited to optical characterization and extremely simple electrical device geometries. Here, we report a piezoelectric-based *in situ* uniaxial strain technique enabling simultaneous electrical transport and optical spectroscopy characterization of dual-gated vdW heterostructure devices. Critically, our technique remains compatible with vdW heterostructure devices of arbitrary complexity fabricated on conventional silicon/silicon dioxide wafer substrates. We demonstrate a large and continuously tunable strain of up to −0.15% at millikelvin temperatures, with larger strain values also likely achievable. We quantify the strain transmission from the silicon wafer to the vdW heterostructure, and further demonstrate the ability of strain to modify the electronic properties of twisted bilayer graphene. Our technique provides a highly versatile new method for exploring the effect of uniaxial strain on both the electrical and optical properties of vdW heterostructures and can be easily extended to include additional characterization techniques.

I. INTRODUCTION

Strain is a powerful tool for directly manipulating the crystal lattice of materials, and consequently for tuning their electronic properties. For example, uniaxial strain can break the in-plane rotational symmetry of a lattice, potentially generating new electronic phases. Over the past decade, a powerful technique has been developed for applying continuously tunable uniaxial strain to three-dimensional bulk quantum materials using a device based on three piezoelectric stacks.[1] This technique has been widely used to study and tune superconductivity,[2–5] topological phases,[6,7] and nematicity[8–11] in a variety of bulk quantum materials and to investigate their thermodynamic properties.[12,13] Over the past few years, van der Waals (vdW) heterostructures have emerged as exciting new platforms for exploring related strongly correlated and topological states in two dimensions. Flat electronic bands arise when two or more vdW sheets are properly stacked and can host a wealth of emergent states including superconductivity, nematicity, ferromagnetism, generalized Wigner crystals, and both integer and fractional Chern insulators.[14–25] However, technical constraints have so far severely limited the extension of existing strain-tuning techniques to the study of these states in vdW heterostructures.

Although there have been a number of approaches developed for applying strain to vdW materials, so far none are compatible with standard electrical transport measurements of dual-gated vdW devices assembled on a silicon/silicon dioxide (Si/SiO$_2$) wafer substrate.[26–32] Prior methods have mostly focused either on suspended vdW samples, which are mechanically fragile, or devices with limited numbers of gate and contact electrodes. In this paper, we introduce a novel method that integrates traditional vdW

heterostructure device fabrication on silicon substrates with a three-piezo-stack-based strain cell.[1,8,33–36] We quantify the induced strain in the active layer of the vdW heterostructure by Raman spectroscopy and corroborate this value with estimates from metallic strain gauges either glued onto the piezo stack or evaporated onto the silicon wafer near the vdW device. We further characterize the strain transmission through multilayer vdW heterostructures by characterizing the strain induced hexagonal boron nitride (hBN) for different flake thicknesses and for twisted hBN multilayers. Our measurements indicate that strain is effectively transmitted from the silicon wafer into many layers of vdW flakes residing on top. Finally, we also showcase the capabilities of our strain technique by measuring the electrical transport properties of a twisted bilayer graphene (tBLG) device near the magic angle and show that strain can induce large changes in the device resistivity. Our technique is compatible with additional experimental probes beyond optics and transport and opens up new avenues for future experiments in vdW heterostructure devices.

II. EXPERIMENTAL METHODS

Our experimental design combines the well-established piezoelectric-based strain technique for bulk samples[1,8,36] with the standard dry-transfer technique for fabricating vdW heterostructure devices.[34] We first discuss the challenges inherent to integrating these two techniques and overview our solution of creating a bowtie-shaped silicon substrate.

A. Current challenges for straining 2D vdW devices

vdW heterostructure devices are typically fabricated on $500\,\mu m$ thick Si/SiO$_2$ wafer substrates.[34,37,38] A simple way to induce strain to the vdW heterostructure is to directly strain the substrate wafer. However, single crystalline silicon is a rigid material, with Young's modulus of $\approx 130–180\,GPa$.[39] Hence, the force required to strain a millimeter size wafer to $\approx 1\%$ is approximately 750 N, far exceeds what can be achieved in existing piezo-based strain devices. Therefore, it remains an open challenge to identify a suitable substrate that is flexible enough to achieve high levels of the strain, yet rigid enough to be compatible with the fabrication of state-of-the-art vdW heterostructure devices. One approach is to replace the silicon wafer with a flexible substrate, such as a thin metal or a polymer.[40–44] For example, large tensile and compressive strains were previously induced in a vdW material by using a two- or three-point bending geometry with flexible substrates such as polyimide-coated phosphor bronze or soft polyethylene-based thin films.[40,43,44] However, bending the substrate can additionally induce an unintentional vertical strain gradient in multilayer vdW heterostructures.

Developments of piezoelectric strain cell technology over the past decade have significantly advanced experimental capabilities for uniaxial strain tuning of bulk crystals.[1] The key innovation was the arrangement of three parallel piezo stacks, which compensates for the large (and inverse) thermal contraction of the piezo stacks. This geometry further enables the application of much larger strain values than previously possible (up to $\approx \pm 1\%$) owing by the counter motion of the central and outer piezo stacks. This strain cell is now commercially available, and it has been successfully

integrated with different experimental probes including nuclear magnetic resonance,[45] x-ray scattering,[4,9] AC specific heat,[12] and the elastocaloric effect.[13] This development naturally leads to the possibility of using the piezoelectric strain cell to apply uniaxial strain to a silicon substrate.

However, the very high Young's modulus of silicon still presents a significant challenge. Without any modification, inducing a one percent strain in a regular silicon wafer requires a force that far exceeds the blocking force of the typical piezo stacks used in commercial strain cells. Several approaches have been developed so far in an attempt to circumvent this issue. One approach is to suspend a sample across a micrometer size gap ($\sim 3–5\,\mu m$), which is created by carefully cleaving the silicon wafer.[46] Although this approach can result in the application of strain exceeding 1% to a thin vdW
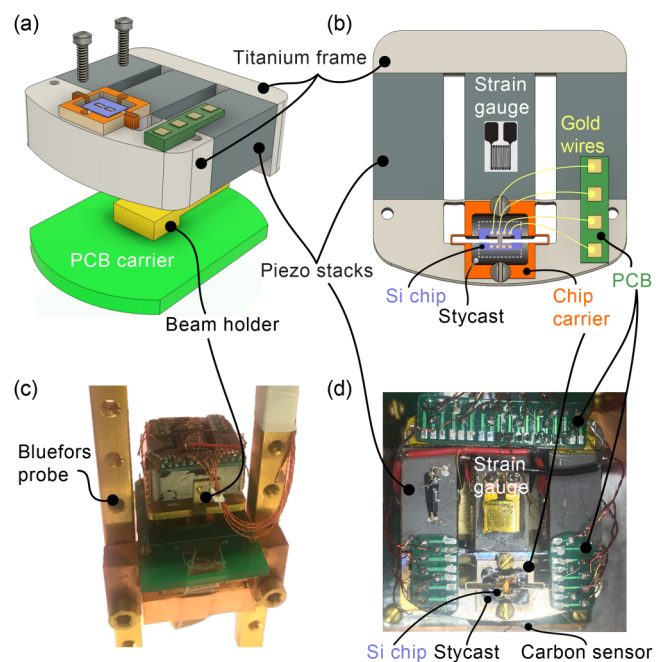
FIG. 1. (a) Schematic of the strain apparatus assembly. The light gray frame is constructed of titanium. The piezo stacks (dark gray) have dimensions of $5 \times 5 \times 9\,mm$.[48] A PCB is affixed onto the side of the strain cell on the titanium frame and hovers above the nearby piezo stack. A second PCB is affixed onto the other side of the strain cell, but is not shown here for clarity. The PCB is used to connect electrical wires to both the sample and the wiring of the cryostat insert. The strain cell is affixed to a PCB carrier by a beam holder, and the entire assembly can be mounted onto various cryostat inserts. (b) Top view of the apparatus. The chip carrier (orange) is tightly affixed onto the titanium frame by two screws. The bowtie-shaped $50\,\mu m$ thick silicon chip (purple) is epoxied onto the chip carrier with Stycast 2850FT epoxy (black). The top surface is partially enveloped by the epoxy, denoted by the white dashed lines. The $25\,\mu m$ gold wires (yellow) are bonded to the PCB pads (green) using silver paste. A commercial strain gauge is glued on the central piezo stack. (c) Side-view photograph of the strain cell attached to a Bluefors dilution refrigerator top-loading insert. (d) Top-view photograph of the strain cell. A temperature sensor made of carbon composition resistor[52] was adhered to the sidewall of the titanium block with GE vanish to monitor the local temperature of the strain cell in the cryostat.

flake, it is extraordinarily difficult to fabricate complex vdW device architectures that are suspended across the gap.

Another approach is to transfer the vdW onto a thin silicon wafer strip, ideally only a few hundred micrometers wide. The small cross section of the thin strip greatly reduces the amount of force required to strain the substrate.[46,47] However, the extremely small size of thin strip makes the fabrication of conventional vdW heterostructure devices very difficult. To address this issue, we developed a new approach in which we first shape the silicon wafer into a bowtie shape. This geometry is inspired by a similar titanium platform structure used in Refs. 8 and 36 to strain bulk crystals. The key advantage of this design is the narrow bridge of the bowtie greatly reduces the amount of force required to induce strain in that region, while the large area at two ends of the wafer simultaneously enables the fabrication of arbitrarily complex vdW heterostructure devices with top and bottom gates and many electrical contacts.

B. The design of strain cell for vdW 2D device

We use a home-built piezoelectric strain cell with a design similar to the one introduced by Hicks *et al.*[1] As depicted in Fig. 1,

the device comprises three piezo stacks ($5 \times 5 \times 9$ mm, with high stiffness constant and blocking force[48]) and custom-machined titanium frames. We further include a beam holder that affixes the strain cell to a printed circuit board (PCB) sample mount, which allows us to easily wire up the strain cell for use in different cryostats (we have so far used a PPMS from Quantum Design, Inc., and a top-loading dilution refrigerator from Bluefors[49]). Viewed from above the strain cell, the bowtie-shaped silicon chip (colored purple) is glued with Stycast epoxy[50] onto a titanium chip carrier (colored orange), which is prefixed onto the titanium sample mount by screws on each end. The glue covers roughly half of the top of the tab area of the bowtie to ensure robust mechanical anchoring, while leaving enough space for around eight electrical contacts on each side. The gold electrical pads are wired to a custom PCB that is mounted on the side of the strain cell. A commercial strain gauge[51] is glued onto one of the piezo stacks and is used to estimate the displacement of the titanium chip carrier by the piezo stacks. A small carbon resistor is adhered to the titanium frame of the strain cell in order to monitor the local temperature.[52]

We fabricate our vdW heterostructure devices atop a $50\,\mu m$ thick silicon wafer with a 285 nm SiO_2 capping layer.[53] This wafer is ten times thinner than those conventionally used for vdW
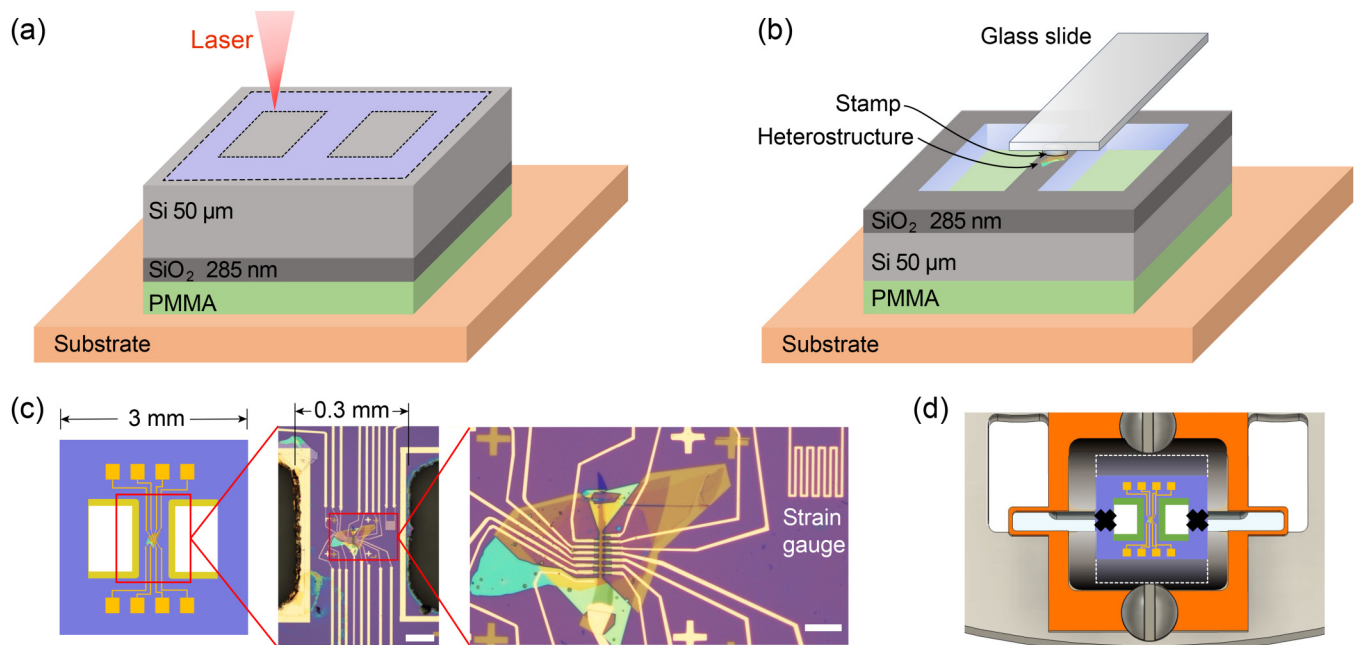
FIG. 2. (a) Cartoon schematic illustrating the laser cutting process used to create a $50\,\mu m$ thick bowtie-shaped silicon chip. The thin silicon wafer (gray) is first glued onto a thicker silicon substrate wafer with PMMA. The 285 nm thick SiO_2 capping layer faces downward to avoid overheating during laser cutting. By carefully adjusting the power, the laser can cut throughout the Si/SiO_2 layers without degrading the SiO_2 surface. The dashed lines indicate the laser cutting path. The light blue indicates that regions of the silicon wafer are removed after cutting. The outer square frame is used to isolate many bowtie-shaped chips from a single large-area wafer. (b) Schematic of a standard dry transfer process of a vdW heterostructure onto the clean SiO_2 layer, located at the center bridge of the pre-cut silicon chip, as shown in (a). (c) Layout of the final silicon chip after electron beam lithography, plasma etching, and metal deposition (left). Optical image of the central bridge region (middle), and the vdW heterostructure device with a meandering gold pattern strain gauge (right). The central bridge width is about 0.3 mm. The white scale bars represent $100\,\mu m$ (middle) and $25\,\mu m$ (right), respectively. (d) Diagram of the silicon chip glued on top of the chip carrier, which is pre-fixed by two screws on the strain cell. The epoxied area regions are outlined by the white dashed lines. The two outside arms (marked by the black crosses) are cut after the epoxy has cured.

heterostructure devices. The reduced thickness is important for lowering the spring constant and enabling the application of larger strain.[46] We first laser-cut two rectangular holes out of the wafer in order to create the bowtie shape. In contrast to previous methods used for laser cutting titanium and quartz plates,[8,36] additional steps are needed to protect the surface of SiO₂ layer when laser cutting the silicon wafer since the vdW heterostructure is extremely sensitive to the surface cleanliness. Therefore, prior to the cutting, we glue the thin wafer atop a thicker silicon substrate using poly-methyl methacrylate (PMMA) as the bonding adhesive. The SiO₂ surface of the thin wafer is arranged to face downward, in contact with the PMMA adhesive. There are two benefits of doing this: first, to provide mechanical stability for the fragile thin wafer, and second, to protect the SiO₂ layer from silicon dust generated during the laser cutting process. The substrate wafer is affixed onto an aluminum plate with double-sided tape, and the plate is mounted on the laser cutting board. We employed a laser cutting system (LPKF ProtoLaser) to cut the silicon wafer. We note that the laser power is critical since over cutting can also damage the SiO₂ layer or result in poor detachment from the PMMA. Here, we use a laser power of 1.2 W with a beam diameter of 10 μm and 1000 times cut repetition for each pattern. The square silicon wafer is cut into the designated pattern outlined by the dashed lines shown in Fig. 2(a). Note that this pattern includes two outer bridges in addition to the central bridge of the bowtie, as shown in Fig. 2(b). These outer bridges are temporary, but they are essential for providing mechanical stability during the transfer and fabrication of vdW heterostructure device. These two outer bridges are cut by hand after mounting the wafer onto the piezoelectric strain cell. The bridges of the bowtie are aligned along <110> directions of a (100) wafer.

After laser cutting, the small three-bridge-patterned thin silicon chips are detached from the Si substrate wafer by sonicating in acetone. The three-bridge-patterned chip is then glued to another rigid silicon substrate with PMMA, this time with its SiO₂ layer facing upwards [Fig. 2(b)]. A vdW heterostructure is assembled layer-by-layer using the standard dry-transfer technique with a poly-carbonate (PC) stamp. After the stack is assembled, the PC stamp is melted onto the central bridge of the thin silicon wafer and soaked in chloroform to dissolve the PC, leaving behind only the vdW heterostructure. Since the patterned wafer detaches from the thicker Si/SiO₂ substrate wafer in chloroform, it must be re-affixed to a new rigid substrate for further processing. The vdW heterostructure is then processed into a Hall bar geometry and contacted electrically following a standard series of steps involving electron beam lithography, plasma etching, and metal deposition. The bowtie pattern created in the silicon wafer does not impede PMMA spin coating and electron-beam lithography; thus, these procedures are essentially the same as in the standard fabrication process for vdW heterostructures. We arrange the Hall bar such that it is aligned along the direction of uniaxial strain. Figure 2(c) shows a typical three-bridge chip with a tBLG device at its center. In addition to the gold electrodes connected to the device, we also evaporate gold along the laser-cut edges of the chip. These gold strips are essential; otherwise, the rough wafer edges resulting from laser cutting can prevent a smooth metal liftoff procedure. Additionally, the roughness can make the wafer more prone to breaking under tensile strain, but these can be smoothed and

potentially strengthened through chemical etching. We also evaporate a meander-shaped gold wire near the device, which serves as a custom local strain gauge. The three-bridge silicon chip is then epoxied to the titanium chip carrier pre-mounted on the strain cell, as described above. The final step is to cut the outer two bridges [at positions indicated by the black crosses in Fig. 2(d)] using a scalpel blade after the epoxy has cured.

III. STRAIN CALIBRATION

In most piezoelectric strain cell experiments, the strain level of the sample was estimated by measuring the displacement of piezo stacks using a capacitance strain gauge.[8,36] The measured displacement was then converted to the strain of the sample by using a strain transmission factor or an effective length determined by the finite element analysis. We performed similar measurements and analysis and present the results in Appendix A. We have also developed two methods to directly measure the amount of strain
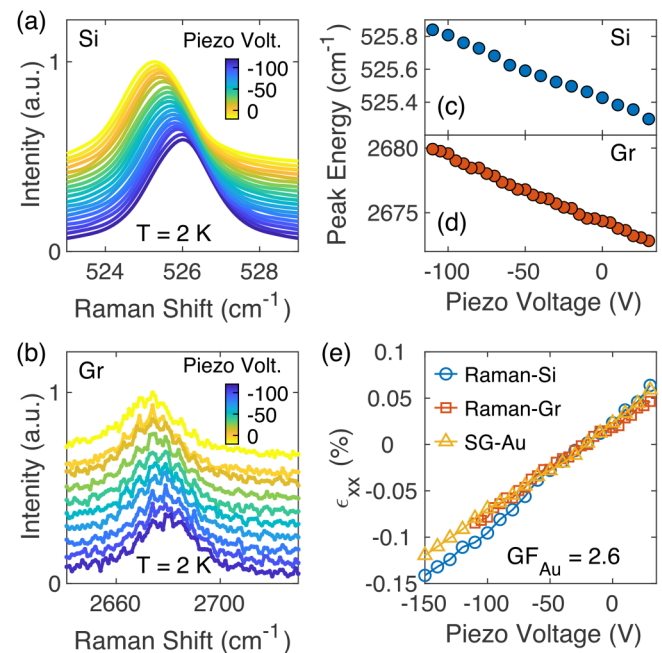
FIG. 3. (a) and (b) Raman spectra of the bowtie-shaped silicon and graphene at different piezo voltages, acquired at a temperature of 2 K. (c) and (d) The energy of the Raman peak of silicon and graphene as a function of piezo voltage, indicating a linear relationship. (e) Measured strain as a function of piezo voltage. The negative piezo voltage corresponds to the direction of compressive strain. The strain values were estimated from the position of the Raman peaks in (c) and (d) or determined by the gold SG deposited on silicon and the commercial SG glued on the piezo stack. The zero-strain point was calibrated by measuring the Raman spectrum at a strain-free spot, located far from the central bridge of the Si wafer. The Raman peak is at 525.5 cm⁻¹, corresponding to a piezo voltage of nearly −20 V. The gauge factor of the gold SG is obtained from the quadratic fitting in Fig. 6(b). The strain values calculated by the SG match well with those measured by Raman spectroscopy, with all exhibiting a linear dependence on the piezo voltage.

induced in the vdW heterostructure as we bias the piezo stacks. We discovered that these two methods provide more accurate and reliable measurement of the strain, which we discuss below.

In the first method, we perform Raman spectroscopy on both the silicon wafer and on a monolayer graphene encapsulated in hBN. We use a laser power of $300\,\mu$W, with integration times of 160 s for graphene and 10 s for silicon. These Raman spectra allow us to precisely determine the magnitude of uniaxial strain independently of graphene and silicon using the relationships previously established in Refs. 40 and 54. Figures 3(c) and 3(d) show the Raman spectra of silicon substrate and graphene taken at different piezo voltages at a temperature of 2 K. Both peaks systematically blueshift due to the effect of compressive uniaxial strain, as shown in Figs. 3(e) and 3(f). We note that the strain cell applies uniaxial stress, which induces both symmetric (A_{1g} irrep) and antisymmetric (E_g irrep, in the case of graphene) components of strain. The linear shift of Raman peak energy is due to the symmetric component of strain. The in-plane Poisson's ratio along <110> directions

of a (100) silicon is only 0.064, indicating a nearly uniaxial strain along the stress direction. This uniaxial strain condition is the same as the Raman measurement performed in Refs. 40 (Si) and 54 (graphene), hence we can reliably use the data in previous work to extract the strain value. We convert the wavenumber of the Raman peak to uniaxial strain following the previously established relationships and plot the measured strain value as a function of piezo voltage in Fig. 3(e). We note that a higher bias up to 300 V, if allowed by the instrumental setup, can be safely applied to the piezo stack at cryogenic temperatures and would likely induce a larger strain.[1,36] The strain induced in the graphene and silicon both vary linearly as a function of piezo voltage, and overlap almost perfectly. The slightly reduced strain in graphene compared with the silicon indicates that $\approx 80\%$ of the strain induced in the silicon wafer is transferred to graphene.

Although Raman spectroscopy provides the most direct means of calibrating the strain in the vdW heterostructure, it is often not possible to perform *in situ* optical measurements. For example,
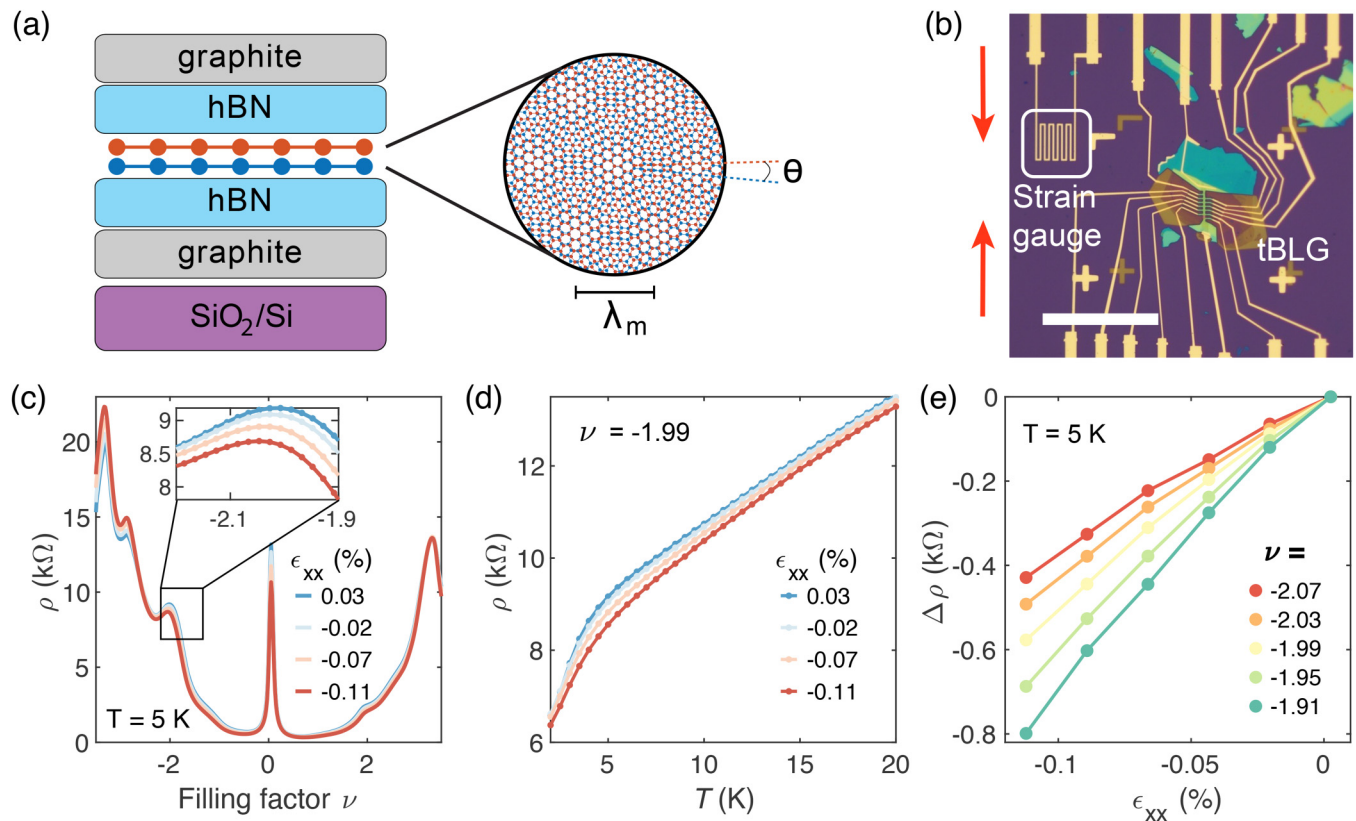
FIG. 4. (a) Schematic of a twisted bilayer graphene sample, encapsulated in hBN with graphite gates top and bottom gates. The right panel displays a cartoon illustration of the moiré pattern of tBLG. The moiré wavelength is $\lambda_m = a/[2\sin(\theta/2)]$, where $a = 0.246$ nm is the lattice constant of graphene and θ represents the twist angle. (b) Optical image of a tBLG device shaped into a Hall bar geometry resting on a bowtie-shaped silicon chip. The long axis of the Hall bar is aligned with the uniaxial strain direction, indicated by the red arrows. A nearby gold strain gauge, with a line width of $2\,\mu$m, is highlighted in the white box. The white scale bar is $100\,\mu$m. (c) Resistivity vs band filling factor at different strains for a tBLG device.[55] Inset: Zoom-in view of the resistivity nearby $\nu = -2$. (d) Temperature dependence of resistivity at different strains. (e) The relative resistivity changes as a function of strain at several filling factors, showing linearity with strain.

transport measurements performed in a dilution refrigerator are generally incompatible with Raman characterization. Therefore, we have also explored electrical means of calibrating the applied strain. The most common technique is to measure the resistance of a long metal wire as the piezo bias is tuned. We have developed custom strain gauges that we fabricate by evaporating a gold meander nearby the vdW heterostructure, as shown in Fig. 2(c). The measured elastoresistance can be converted to strain by

$$\varepsilon = \frac{\Delta R/R}{GF}, \tag{1}$$

where GF is the gauge factor of the strain gauge. There are, however, two sources of uncertainty inherent to this technique. First, the strain is measured in the silicon and not directly in the vdW material of interest. Second, the gauge factor of the gold strain gauge can vary between ≈ 2.1 and 3.3 in our experiments, based on the precise details of the device fabrication (more details can be found in Appendix B). Nevertheless, we observed a systematic variation of the gauge factor as a function of the gauge resistivity. By fitting the gauge factor vs resistivity with a quadratic function, we estimated the gauge factor of the gold strain gauge evaporated near the same device measured by the Rama spectroscopy. Figure 3(e) shows the measured strain from the gold strain gauge compared with the strain measured by the Raman spectroscopy. We see that both methods are in good agreement. Therefore, the evaporated gold strain gauges provide a reliable rough estimate of the induced strain in the vdW heterostructure and can be used to confirm that the induced strain in the wafer is linear in the applied piezo voltage.

IV. THE EFFECT OF STRAIN ON TRANSPORT IN A TWISTED BILAYER GRAPHENE DEVICE

In order to demonstrate the power of our strain technique, we measure the strain-dependent transport of a vdW heterostructure device consisting of a twisted bilayer graphene device. The twist angle of the device is $\theta = 1.2°$, very near the magic angle at which superconductivity and other correlated states are prominent. The rich correlated and topological physics of magic-angle tBLG has been explored in great detail elsewhere;[20,21] here, we use it as a model system to test our technique, given that the band structure is expected to be highly sensitive to strain. The device consists of tBLG encapsulated by flakes of hBN, all resting on a flake of graphite (further details on this device can be found in Ref. 55). The graphite acts as a back gate and can change the charge carrier density in the tBLG when a voltage is applied between the graphite and tBLG. Figure 4(c) shows a measurement of the longitudinal resistivity, ρ of the device as a function of the band filling factor, ν ($\nu = 4$ corresponds to fully filled moiré bands, where the factor of four reflects the spin and valley degeneracy of graphene). In our measurements performed at a temperature of 5 K, we see a resistive state at $\nu = 0$ indicative of the charge neutrality point, as well as resistive states at other selected integer values of ν indicative of incipient correlated insulating states. As we apply uniaxial strain by changing the bias on the piezo stacks, we see that the resistivity of the device can change by hundreds of ohms, depending on the precise value of ν.

The effect of strain is especially prominent around $\nu = -2$, which corresponds to a developing correlated insulating state at half filling of the moiré valence band in the tBLG. Figure 4(d) shows how ρ evolves both as a function of temperature and strain at a fixed band filling factor of $\nu = -1.99$. Overall, the temperature dependence is characteristic of tBLG devices previously reported.[23–25] By comparing $\rho(T)$ at different values of applied strain, we see that there is a monotonic decrease of the resistivity at all temperatures up to 20 K as compressive strain is applied. Figure 4(e) shows the relative resistivity, $\Delta\rho$, as a function of compressive strain at values of $\nu \approx -2$. In all cases, we see a nearly linear change in resistivity as strain is applied. Although future work is necessary to unravel the physics underlying the strain-tuning of these states, the large linear elastoresistance we see clearly illustrates the ability of strain to manipulate the electronic properties of tBLG.

V. CONCLUSION

In summary, we have reported the development of a new technique for applying continuously tunable strain to vdW heterostructure devices of ultrahigh quality and arbitrary complexity. The strain device is based on a commercially available three piezo stack design, with custom PCBs added in order to electrically connect to vdW heterostructure devices. We achieved a large strain in excess of -0.15% by appropriately modifying the silicon substrate. We are able to demonstrate efficient strain transfer from the piezo stacks to the vdW heterostructure. As shown in Fig. 3(e), the measured strain is linear in the applied piezo voltage over the entire range we studied. This linearity implies that the total strain we can achieve can very likely be increased by further improvements in epoxying both the top and bottom surfaces of the silicon wafer to the sample mount, and by applying larger voltages to the piezo stacks up to 300 V. Our technique paves the way for future characterization and control of the correlated and topological physics of a variety of vdW heterostructures. The technique is readily compatible with a range of other characterization tools, including scanning probe microscopes.

AUTHOR DECLARATIONS
Conflict of Interest

The authors have no conflicts to disclose.

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Author Contributions

Z.L. and X.M. contributed equally to this paper.

Zhaoyu Liu: Conceptualization (equal); Data curation (equal); Formal analysis (equal); Investigation (equal); Methodology (equal); Project administration (equal); Supervision (equal); Validation (equal); Visualization (equal); Writing – original draft (equal); Writing – review & editing (equal). **Xuetao Ma:** Conceptualization (equal); Data curation (equal); Formal analysis (equal); Investigation (equal); Methodology (equal); Validation (equal); Visualization (equal); Writing – original draft (equal); Writing – review & editing (equal). **John Cenker:** Data curation (supporting); Formal analysis (supporting); Writing – review & editing (supporting). **Jiaqi Cai:** Data curation (supporting); Writing – review & editing (supporting). **Zaiyao Fei:** Data curation (supporting); Writing – review & editing (supporting). **Paul Malinowski:** Conceptualization (supporting); Data curation (supporting); Writing – review & editing (supporting). **Joshua Mutch:** Conceptualization (supporting); Data curation (equal); Writing – review & editing (supporting). **Yuzhou Zhao:** Conceptualization (supporting); Data curation (supporting); Formal analysis (supporting); Writing – review & editing (supporting). **Kyle Hwangbo:** Data curation (supporting); Writing – review & editing (supporting). **Zhong Lin:** Conceptualization (supporting); Writing – review & editing (supporting). **Arnab Manna:** Data curation (supporting); Writing – review & editing (supporting). **Jihui Yang:** Funding acquisition (equal); Writing – review & editing (equal). **David Cobden:** Funding acquisition (supporting); Methodology (supporting); Writing – review & editing (supporting). **Xiaodong Xu:** Funding acquisition (supporting); Writing – review & editing (supporting). **Matthew Yankowitz:** Conceptualization (equal); Formal analysis (equal); Funding acquisition (equal); Investigation (equal); Methodology (equal); Project administration (equal); Resources (equal); Supervision (equal); Validation (equal); Visualization (equal); Writing – original draft (equal); Writing – review & editing (equal). **Jiun-Haw Chu:** Conceptualization (equal); Formal analysis (equal); Funding acquisition (lead); Investigation (equal); Methodology (equal); Project administration (equal); Resources (equal); Supervision (equal); Validation (equal); Visualization (equal); Writing – original draft (equal); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding authors upon reasonable request.

APPENDIX A: STRAIN ESTIMATION VIA FINITE ELEMENT ANALYSIS

In addition to the direct measurement of the strain in the silicon substrate and graphene as discussed in the main text, we also estimate the induced strain by measuring the displacement of the piezo stacks and perform finite element analysis. To do this, we epoxy a commercial strain gauge directly atop one of the piezo stacks [Figs. 1(b) and 1(d)]. Since the gauge factor of the commercial strain gauge is well calibrated, we can directly extract the strain in the piezo stacks, $\varepsilon_{\text{piezo}}$, and the displacement of the piezo stacks, $L_{\text{piezo}} \times \varepsilon_{\text{piezo}}$, where $L_{\text{piezo}} = 9$ mm is the length of the piezo stack. The displacement allows us to estimate the strain in the silicon substrate, $\varepsilon_{xx}^{\text{norm}}$, by the following relationship:

$$\varepsilon_{xx}^{\text{norm}} = \mu \frac{2L_{\text{piezo}}}{L_{\text{gap}}} \varepsilon_{\text{piezo}}, \tag{A1}$$

where $L_{\text{gap}} = 0.5$ mm is the distance between the titanium sample holder and μ is a dimensionless strain transmission factor that takes into account the strain relaxation due to the epoxy and within the silicon substrate. The factor of 2 takes into account the displacement of both the center piezo stacks and the outer two piezo stacks.

To estimate the strain transmission factor μ, we performed FEA using ANSYS Academic Research Mechanical software to investigate the strain distribution in the bowtie-shaped silicon chip model, as shown in Fig. 5(a). Young's modulus and Poisson's ratio of the silicon along the <110> directions of a (100) wafer in the simulation are 169 GPa and 0.064, respectively.[39] Young's modulus of the SiO$_2$ layer is 70 GPa. The narrow bridge of the silicon chip is 0.3 mm in width and 50 μm in thickness. Using $k = Y\frac{A}{L}$, we estimated the effective spring constants of Si and SiO$_2$ layers on a strip substrate matching the dimensions of the central bridge of the bowtie-shaped chip. The effective spring constant of the silicon substrate is $k = 5.1$ N/μm, which is significantly larger that of the SiO$_2$ layer, 0.012 N/μm. Hence, the SiO$_2$ layer can be safely ignored in our FEA simulation.

In this simulation, a 5 μm displacement was applied to both sides of the titanium plate, which results in a total 2% nominal uniaxial strain. We assume the thickness of the epoxy layer to be 50 μm. In Figs. 5(b) and 5(c), we present both the top and cross-sectional views of the strain distribution. Notably, the strain primarily aligns along the white dashed center-line of the silicon wafer. The highest strain region (colored in red) is located at the center, where the vdW heterostructure was fabricated. As shown in Fig. 5(d), in the simulation the strain at the center of the silicon bridge is 1.04%, resulting in a strain transmission factor $\mu_{\text{FEA}} = 52\%$. Nevertheless, this simulation does not take into account that the titanium strain cell itself may also deform. Using the effective spring constant of 12 N/μm for the strain cell[36] and 5.1 N/μm for the substrate, we estimate that only 70% of the displacement induced by the piezo actuator is transferred to the silicon substrate. Taking this factor into account, the strain estimated by this method is within a factor of two of the strain measured by the Raman spectroscopy [Fig. 3(e)].

Additionally, we simulate the strain at the center of the bridge as a function of the epoxy thickness, t. The results, presented in Fig. 5(f), demonstrate that the applied strain gradually decreases as the epoxy thickness exceeds 100 μm. However, in practice, achieving a precise thickness of epoxy presents a challenge. We attempt to minimize the thickness by using as little epoxy as possible and by carefully pressing the wafer down in order to extrude excess epoxy out from underneath.
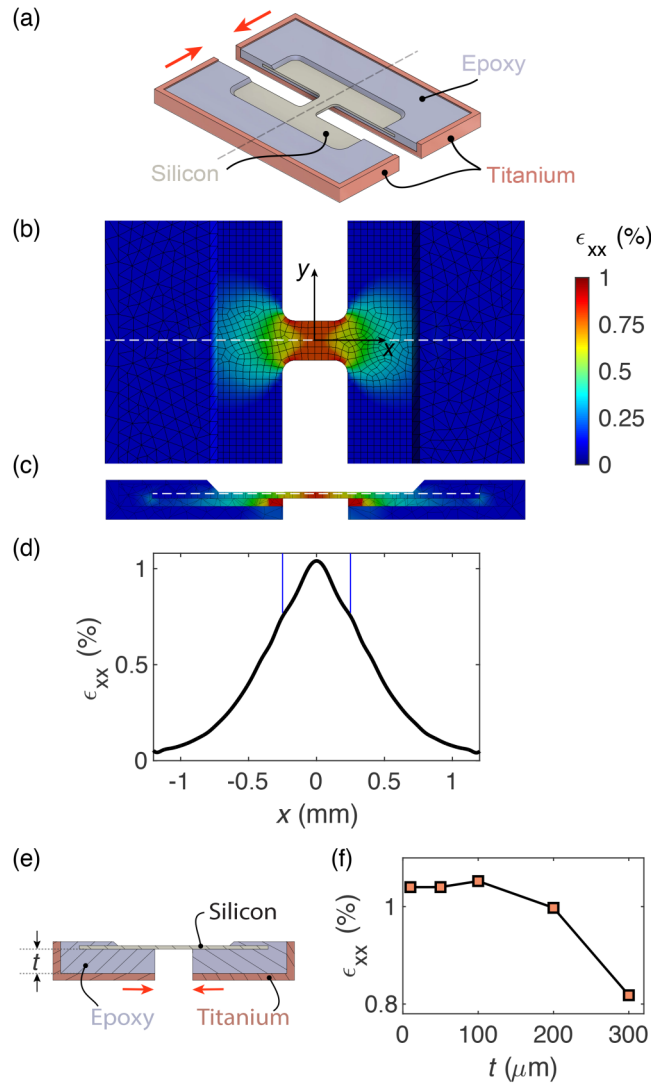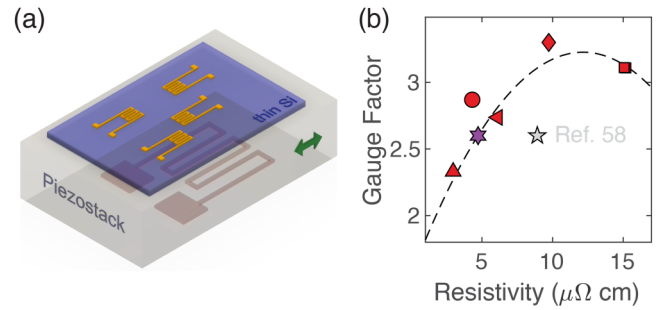
FIG. 5. (a) Illustration of a bowtie-shaped silicon chip for FEA. The chip is encapsulated with an epoxy layer (50 μm thick). The red arrows indicate the moving directions of the titanium plates. The strain distribution in a top-down view (b) and a cross-sectional view along the dashed centerline (c). (d) Strain variations along a designated path, marked by a dashed line in (c). Blue lines highlight the gap region. (e) The cross-sectional view along the dashed line in (a) exhibits the model characterized by thickness denoted as t. (f) Plot strain at the central point in (d) as a function of the epoxy thickness.

FIG. 6. (a) Configuration for measuring the gold strain gauges with a single piezo stack technique. The Si/SiO$_2$ substrate and commercial SG were glued to top and bottom of the piezo stack with epoxy, respectively. The gold SGs were directly deposited on SiO$_2$ surface. The green arrow presents the poling direction of the piezo stack. (b) Gauge factor of the gold SG as a function of the resistivity at 2 K. The different red symbols refer to different measurements. The purple hexagram indicates the gold SG in Fig. 3(e). The data can be fitted by a quadratic curve (dashed line): $GF = -0.0113\rho^2 + 0.2753\rho + 1.553$.

APPENDIX B: GOLD STRAIN GAUGE CALIBRATION

To calibrate the gold SGs, we have conducted measurements on multiple gold SGs using a single piezo stack technique.[56] The gold SGs were fabricated either directly on top of a Si/SiO$_2$ substrate or above several single-hBN flakes, as shown in Fig. 6(a). The silicon wafer is glued to one side of the piezo stack, while a commercial SG is affixed on the other side. At low temperature, the strain can be almost fully transferred to the silicon wafer which can be precisely measured by the commercial SG.[57] After determining the strain of the silicon wafer, we calibrate the gold SGs by measuring the change of resistance of the gold SGs fabricated on silicon wafer and obtain the gauge factor using Eq. (1). In Fig. 6(b), we plot the obtained gauge factor as a function of the resistivity of the gold SGs. The gauge factor ranges from 2.1 to 3.3, in agreement with the previous report,[58] and follows a quadratic behavior as a function of resistivity. The fitted quadratic function allows us to determine the gauge factor of gold SGs in other experiments. We have also estimated the strain transmission through the vdW heterostructures by taking the ratio between the strain measured from gold SGs on hBN flakes and those on the silicon wafer. The ratio is typically above 90% and remains nearly independent of temperature and thickness below 20 K. While the variation of the gauge factor between different gold SG does not allow us to directly interpret this ratio as the actual strain transmission factor, this is in broad agreement with the results of Raman measurement presented in Fig. 3 in the main text.

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