Compact Heterogeneously Integrated Optical Phase-Locked Loop for 10 GHz to 40 GHz Optical Frequency Difference Locking

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***Abstract*—An optical phase-locked loop (OPLL) is presented in this paper to lock the beat note generated by heterodyning two lasers to an electrical reference signal. The proposed OPLL is a heterogeneous integration of a photonic integrated circuit (PIC) and a CMOS electronic integrated circuit (EIC) to achieve a compact size and reduce loop delay. The photo-mixing is performed in the photodiode (PD) fabricated on the silicon photonic (SiP) chip. The generated beat note is first mixed down to a lower frequency by a millimeter-wave (mm-wave) mixer and then compared with a reference signal in the CMOS chip to generate feedback signal for the follower laser. With the help of the mm-wave mixer, the locking range is greatly extended. Moreover, impedance matching between the PIC and EIC is discussed in detail, which is critical to achieve contiguously wide frequency locking range. A prototype of the OPLL is fabricated and tested. During experiments, the frequency difference between two lasers is locked continuously from 10 GHz to 40 GHz with a significant improvement in the phase noise from -30 dBc/Hz to -70 dBc/Hz at 100 Hz offset frequency within the loop bandwidth.**

***Index Terms*—Optical phase-locked loops, photonic integrated circuits, microwave photonics, heterogeneous integration.**

I. Introduction

Interest in mm-wave and sub-terahertz (sub-THz) frequency ranges has been growning significantly in last few decades. The inherent wide bandwidth is a promising solution to meet the ever-growing demand for high data rates required by communication systems [1], [2]. The mm-wave/sub-THz signal could be generated electronically [3]–[5] or opto-electronically by mixing two lasers/comb lines (optical heterodyning) inside a photodiode (PD) [6]–[9]. Compared to purely electronic systems, microwave photonic systems may offer a promising and affordable approach to build wideband and long-range mm-wave/sub-THz communication links due to the ability to transport microwave frequencies over long distances in optical domain with little attenuation.

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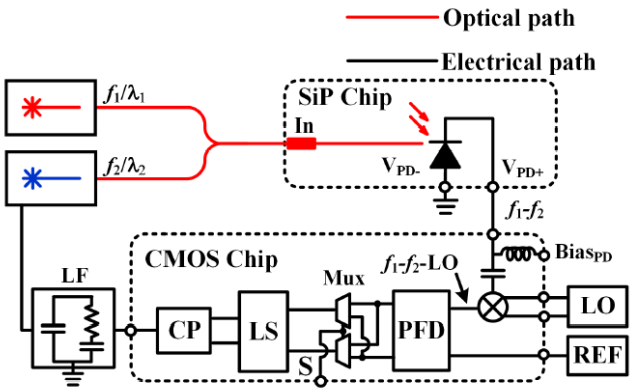

Fig. 1. System diagram of the proposed OPLL.

The frequency of the generated beat note in microwave photonic systems may drift over time because the wavelengths of the lasers/comb lines drift due to variations in temperature, pump currents, etc. Different locking technologies are proposed to solve the drifting issue, including optical injection-locking (OIL) [10] and optical phase-locked loop (OPLL) [11]–[25]. The OIL provides narrow locking range due to its homodyne nature. In comparison, OPLL is capable of locking the beat note to an electronic reference in a continuous wide frequency range. It also reduces linewidth of the beat note.

The implementation of OPLL consists of an optical part and an electronic part. In optical part, lights from two lasers are combined and fed into a wideband PD for photo-mixing to generate mm-wave beat note. Inside the electronic part, an electronic PLL will compare the phase/frequency of the beat note with an electronic reference to generate an error correction signal, fed back to one of the lasers (follower laser) through the loop filter (LF). To achieve compact size and reduce the loop delay, PIC and EIC are preferred in OPLL designs, usually leading to heterogeneous integration. Impedance matching between the optical circuit and the electrical circuit is critical to achieve wide locking range. However, few papers discuss the impedance match issue and the locking range rarely exceeds 25 GHz [11]–[25].

In this paper, a compact heterogeneously integrated OPLL is presented, which is an extension of the work published in [26]. The previous work reported an OPLL consisting of an EIC and a commercial PD with locking range up to 1.12 GHz. In

this work, the proposed OPLL is a heterogeneous integration between the PIC and CMOS EIC to achieve compact circuit size and reduce loop delay as shown in Fig. 1. The beat note is generated in the on-chip PD and will be locked to a reference single through the CMOS chip. Moreover, a mm-wave on-chip mixer is added to significantly extend the locking range. Furthermore, impedance matching between the PIC and EIC is discussed in detail to ensure a continuous wide frequency locking range from 10 GHz to 40 GHz. The rest of the paper is organized as follows: the design and fabrication of the PIC and the EIC are described in Section II, the heterogeneous integration of OPLL and impedance matching is discussed in Section III, the measurement results of the OPLL is demonstrated in Section IV and the conclusion is presented in Section V.

II. Chip Design and Fabrication

A. Silicon Photonic Chip

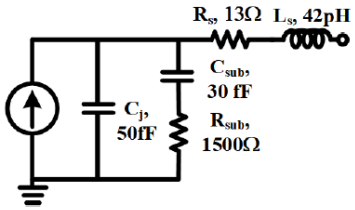

Fig. 2. Proposed circuit model for the output impedance of the PD.

The optical portion of the OPLL is fabricated on a SiP chip from AIM Photonics with the schematic shown in top-right corner in Fig. 1. It consists of one optical port and two electronic ports. Lights from two lasers are combined off-chip and fed into the photonic chip through edge-coupling. Then, the combined light is fed into a PD to generate the beat note for locking. The bias of the PD is provided from the EIC through a on-chip bias-tee.

The frequency response of a single PD is characterized in [27]. The single PD can provide output power up to 0 dBm with 3-dB bandwidth of 15 GHz. It has an external responsivity of (0.23±0.03) A/W and an internal responsivity of 0.85 A/W.

The output impedance of the PD is critical for the integration with the electronic CMOS chip. Thus, the output impedance of three PDs are measured and a circuit model is proposed to match the measured results. The proposed circuit model is drawn in Fig. 2. The PD is represented by an ideal source with parasitics, where C_j represents the junction capacitance at -1V biasing, R_s and L_s represents the series resistance and inductance, and C_{sub} and R_{sub} represent the substrate coupling effect.

Fig. 3 demonstrates the measured normalized output impedance (normalized to 50 Ω) of three PDs up to 50 GHz. Based on the measured results, fitting values of parasitics are chosen as C_j = 50 fF, R_s = 13 Ω, L_s = 42 pH, C_{sub} = 30 fF, R_{sub} = 1500 Ω. The simulated impedance is plotted in Fig. 3 for comparison. The fitting curve agrees very well with the measured ones, proving the accuracy of the circuit model up to 50 GHz.

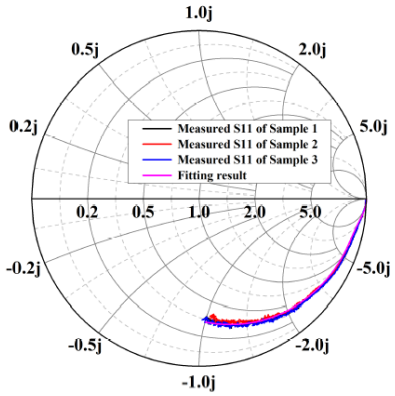

Fig. 3. Measured normalized output impedance (normalized to 50 Ω) of three PDs and the fitting result of the circuit model.

B. Electronic CMOS Chip

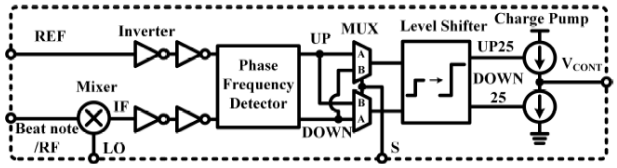

Fig. 4. System diagram of the CMOS EIC.

The electronic chip is designed based on TSMC 65nm GP CMOS process. The system diagram of CMOS EIC is depicted in Fig. 4. The beat note generated from the PIC is first input into a mm-wave mixer. When mixed with the input local oscillator (LO) signal, the beat note is mixed down to a lower intermediate frequency (IF) signal which will be compared with a reference (REF) signal provided from an off-chip signal generator. The frequency of IF signal is set at 100 MHz to minimize the phase noise from the signal generator. With the help of the mm-wave mixer, the proposed OPLL provides a wide locking range from 10 GHz to 40 GHz. The sinusoidal waves at REF and IF are converted to square waves by two inverters, facilitating the phase/frequency comparison process in next stages. The phase-frequency detector (PFD) compares the frequency/phase deference between the IF signal and the REF signal, then it generates error correction signals as pulses at UP node (or DOWN node) when the phase of the REF signal leads (or lags) of that of the IF signal. In order to increase tuning range of the OPLL, a level shifter (LS) is used to shift the voltage swing of the pulses from 1.1 V at UP/DOWN nodes to 2.5V at UP25/DOWN25 nodes. When the charge pump (CP) receives pulses at UP 25 node, it will inject current into the output V_{cont} node, raising its voltage. Similarly, when pulse exists on DOWN25 node, the CP will sink current from V_{cont} node, lowering its voltage. Thus, the voltage at V_{cont} node serves as a feedback voltage to the piezo port on the follower laser. In order to accommodate lasers with different polarity of sensitivity coefficient K_{laser} at piezo

port, the polarity of the V_{cont} can be adjusted accordingly by inserting 2x1 multiplexers (MUX) between the PFD and the LS. When the switch signal (S) is low, the polarity of V_{cont} is set as positive when REF leads IF signal, vice versa.

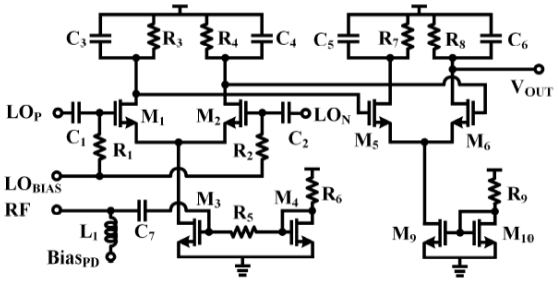

Fig. 5. Schematic of the mm-wave mixer on the electronic chip.

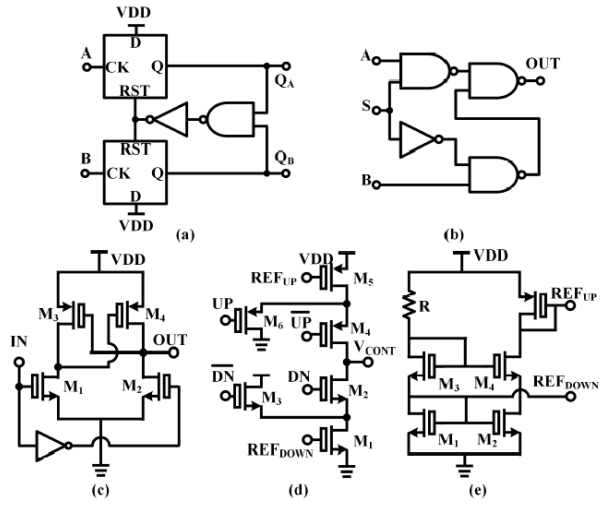

Fig. 6. Schematics of (a) PFD, (b) MUX, (c) LS, (d) CP and (e) voltage references on the electronic chip.

The circuit diagrams of fundamental building blocks inside EIC are shown in Fig. 5 and Fig. 6. The schematic of the single-balanced mm-wave mixer is shown in Fig. 5. The input RF signal from 10 GHz to 40 GHz is mixed down to 100 MHz. An on-chip bias-tee comprised of L_1 and C_7 is placed at the RF port. The beat note from the output of PD is AC coupled to the RF port through C_7 while the bias voltage of the PD is provided through L_1. Moreover, the value of L_1 is optimised to improve the impedance matching with the PIC. Details of matching between the PD and mixer is discussed in Section III. The LO port is biased through 50 Ω resistors which are important for impedance matching. An active balun is placed after the mixer to convert the differential output into a single-ended output. Capacitors C_3 to C_6 are used to reduce the signal leakage from LO port to IF port.

The schematic of the PFD is shown in Fig. 6(a). It compares the phase difference between A and B. If the waveform at A leads that at B, Q_A will rise to logic one first when rising-edge of the A arrives at the D flip-flop on the top. After a finite

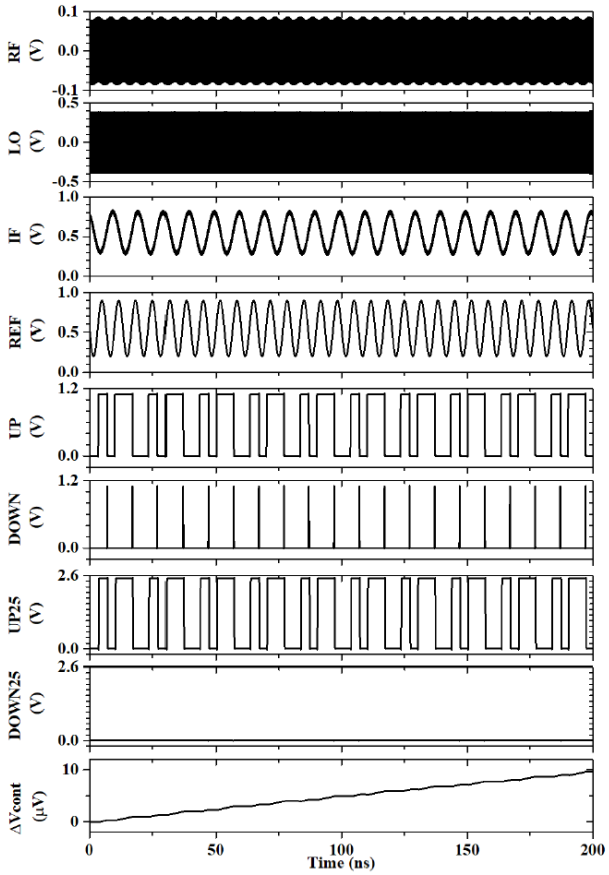

Fig. 7. Transient simulation of voltages at various nodes in Fig.4

delay, Q_A will be reset to logic zero when the rising-edge of waveform B arrives at the D flip-lop on the bottom, triggering the And gate and resets both flip-flops. Thus, the duration of the pulse at Q_A is equal to the time delay between waveform A and waveform B, which is proportional to the phase difference. Similarly, pulses will be generated at Q_B when waveform at B leads that at A.

The MUX is implemented by logic gates as shown in Fig. 4(b). It allows the pulses at UP and DOWN to be swapped in Fig. 4. When S is set to high, A passes to the output. Otherwise, B passes to the output when S is low.

The frequency tuning range of OPLL is determined by $K_{laser} * V_{cont}$. In order to increase the frequency tuning range, a LS is used to extend the voltage swing of V_{cont} from 1.1V to 2.5V. Fig. 6(c) shows the schematic of the LS, where transistors with high breakdown voltage are utilized. When input IN is high, M1 will pull down the gate voltage of M4, setting OUT as 2.5V supply voltage. When input IN is set to low, it will turn M2 on, forcing OUT to ground. In conclusion, OUT is a 2.5V level-shifted of 1.1V IN.

The structure of the CP is depicted in Fig. 6(d) with voltage references generated from Fig. 6(e). It converts the pulses at UP node into charge current at V_{cont} and pulses at DN into discharge current at V_{cont}. M1 and M5 serve as constant current sources. When pulse arrives at UP, M4 is on and M6 is off. The current from M5 is injected into V_{cont}, raising its

voltage. When pulse ends, the current is steered from M5 to M6 and is sinked to ground. Similar function can be observed with M1, M2, M3 and pulses at DN.

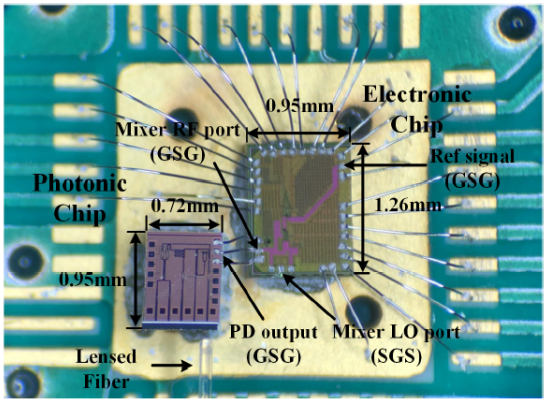

Fig. 8. Photograph of the finished integration.

Simulation is performed in Cadence Virtuoso to ensure the EIC functions as expected and the simulated results are plotted in Fig. 7 with RF set at 28GHz, LO at 27.9 GHz and REF at 150 MHz. After mixing, a 100 MHz sinusoidal signal is generated at IF node as expected. Since REF signal is faster than IF signal, PFD generates pules at UP and resetting pulses are generated at DOWN. The LS extends the swing of pulse from 1 V to 2.5 V as shown at UP25 and it also suppresses the resetting pulses at DOWN as the flat line shown at DOWN25. Finally, pulses at UP25 raises the voltage at V_{cont} by charging the capacitance at V_{cont}. The simulated delay of the EIC is 4 ns.

III. Opto-electronic Heterogeneous Integration

Fig. 1 presents the integration scheme for the heterogeneous integration of the SiP chip and the CMOS chip with Fig. 8 showing the photo of the finished integration. Lights from both lasers are combined and fed into the PD by edge-coupling through a lensed fiber. The output of the PD (GSG) is connected to the RF port (GSG) of the mm-wave mixer through wire bonding. The PD is biased through the on-chip bias-tee. Two signal generators are used as LO signal and REF signal, separately. The high-frequency differential LO signal (SGS) is provided by directly probing to reduce parasitics. The REF signal is injected in to the electronic chip via GSG wirebonds. After comparing phases between the IF signal and the REF signal, the generated voltage feedback signal is first filtered by a 2nd-order loop filter to suppress high-frequency ripples and feedbacked to the piezo port of the follower laser for locking. The photonic chip is fabricated by AIM Photonics with a size of 0.684 mm^2. The electronic chip is fabricated using TSMC 65nm GP CMOS process with a size of 1.197 mm^2. The power consumption of the electronic chip is 4.93 mW.

The impedance matching between the SiP chip and the CMOS chip is critical for successful locking in a wide frequency range specially above 20 GHz. Mismatch would result in high insertion loss between SiP chip and CMOS chip, greatly reduce the locking range. In this work, a on-chip matching network is designed to achieve good matching between two chips and to keep a compact size. Before matching, the output impedance of SiP chip, the input impedance of the CMOS chip, and the bonding wire between two chips should be carefully characterized.

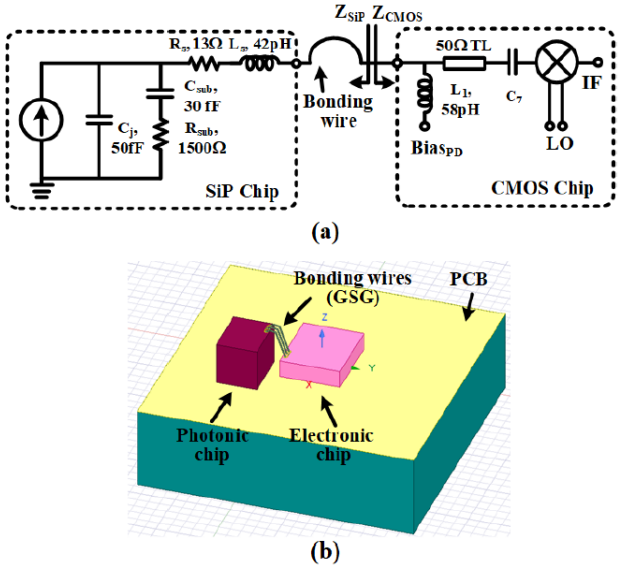

Fig. 9. (a) Circuit model for impedance matching between the SiP chip and CMOS chip and (b) the modelling of the bonding wire between EIC and PIC in HFSS.

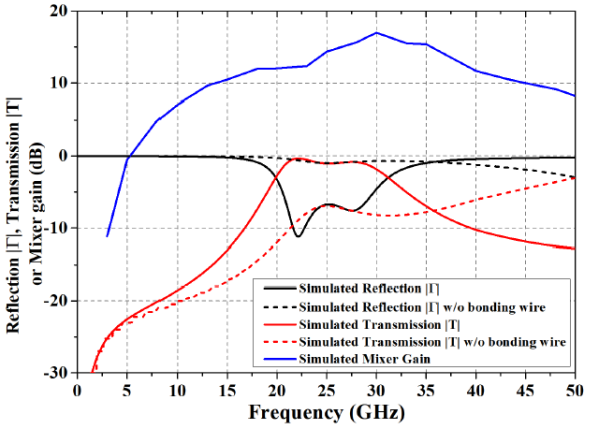

Fig. 10. Simulated reflection, transmission between chips, and simulated gain of the on-chip mm-wave mixer.

Fig. 9(a) shows the circuit model used for impedance matching. A on-chip matching network is designed to achieve good matching between two chips, consisting of inductor L_1, 50 Ω transmission line (TL) and bonding wire. At high frequency up to 50 GHz, the bonding wire can not be ignored and it plays an important role on matching. The output impedance of the PD is obtained by using the circuit model studied in Section II.A. The input impedance of the CMOS chip is simulated in Cadence with L_1 and TL EM simulated in GoldenGate. The

S-parameter of the bonding wire is obtained by simulations in Ansys HFSS up to 50 GHz as shown in Fig. 9(b). As drawn in Fig. 9(a), the impedance of the SiP chip with the bonding wire is represented by Z_{SiP} while the impedance of the CMOS chip by Z_{CMOS}. The reflection and transmission coefficients (Γ and T) between chips can be calculated according to equation (1) and (2).

$$\Gamma = \frac{Z_{SiP} - Z^*_{CMOS}}{Z_{SiP} + Z_{CMOS}} \tag{1}$$

$$T = 1 - |\Gamma|^2 \tag{2}$$

The impedance matching is achieved by optimizing the length of the bonding wire, the length of TL and the value of the inductor L_1 on the CMOS chip. After optimization, the simulated $|\Gamma|$ and $|\mathrm{T}|$ along with the mixer gain is plotted in Fig. 10. Good impedance matching is achieved from 20 GHz to 31 GHz with 3-dB insertion loss ($|\mathrm{T}|$). Higher insertion loss is experienced outside this range which could be compensated by the positive gain provided by the active on-chip mixer. Moreover, enough RF power can be transmitted to the CMOS chip by increasing photocurrent on the fabricated PD. Thus, it is possible to achieve wideband locking based on the results shown in Fig. 10.

For comparison, simulated $|\Gamma|$ and $|\mathrm{T}|$ in dashed lines without considering the bonding wire are added in Fig. 10. The simulated results show that at least 7 dB insertion loss ($|\mathrm{T}| <$ -7 dB) is introduced from 10 GHz to 40 GHz without considering the bond wire's effect on matching. It proves that the bonding wire has a substantial effect on the impedance matching at these high frequencies and proper modeling is required.

A design procedure for impedance matching between the two chips are summarized as below.

- Step 1. Characterize the impedance of PD by measurement and modeling as discussed in Section II-A. In Fig. 3, the measured results agree well with the fitting result, validating the accuracy of the proposed PD model in Fig. 2 up to 50 GHz.
- Step 2. Simulate the input impedance of the mixer on electronic chip.
- Step 3. Based on the impedances obtained in Step 1 and 2, design the impedance matching network between the PD and the mixer. In this work, the matching network includes inductor L_1, 50 Ω TL and the bonding wire. To achieve high accuracy, the bonding wire is EM simulated up to 50 GHz in the Ansys HFSS, and the inductor and the TL are EM simulated in Cadence with GoldenGate. To achieve good matching, the value of the inductor L_1, the length of the TL, and the length of the bonding wire are designed to optimize matching performance.

IV. Experimental Results

A. Measurement Setup

The measurement setup of the OPLL is depicted in Fig. 11. The two lasers used in measurement are Koheras AdjustiK

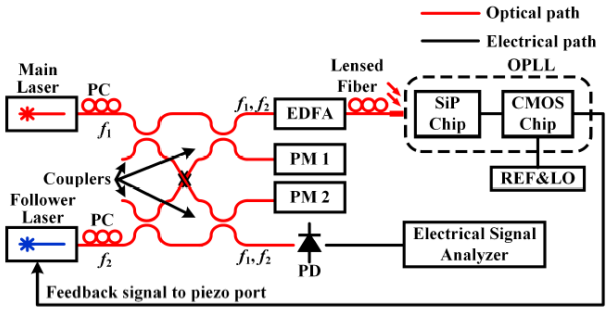

Fig. 11. Measurement setup for the proposed OPLL

E15 fiber lasers from NKT Photonics and operate nominally at 1550 nm optical wavelength with thermal tuning range of 80 GHz each, and piezoelectric tuning range of 8 GHz each. The linewidth of the lasers is 1 kHz over 120 us. Lights from both main laser (f_1) and follower laser (f_2) are first split then combined into two paths through four couplers. Polarization match is achieved by adjusting the polarization controllers (PC) after each laser and the optical power from each path is monitored by powermeters (PM1 and PM2). The top path is used for locking while the bottom path is used to monitor and measure the beat note. In the top path, the combined lights (f_1 & f_2) are amplified by the erbium doped fiber amplifier (EDFA, from Keopsys) and coupled into the SiP chip through a lensed fiber. The beat note generated by the on-chip PD is fed to the CMOS chip for locking. The high-frequency beat note will be mixed with the LO signal (from Keysight E8257D through SGS probing) to the IF band and compared with the reference signal (from Mini-circuit SSG-6001 through GSG wire bonding) to generate the feedback signal for the follower laser through the piezo port. In the bottom path, a 50 GHz commercial PD and a 50 GHz electrical signal analyzer (ESA, Keysight N9030A) are utilized to monitor the beat note and measure the phase noise of the locked beat note.

In measurements, the wavelength of the main laser is constantly set at 1550.32 nm while the wavelength of the follower laser is adjusted accordingly to generate beat notes at desired frequencies. The LO signal is set 100 MHz below the beat note. After mixing, the generated drifting 100 MHz IF signal is compared and locked to the stable reference signal at 100 MHz.

B. Measurement at 28 GHz

The beat note is first locked at 28 GHz to demonstrate the compatibility of the proposed OPLL with 5G communications. The wavelength of main laser is set at 1550.32 nm while the follower laser is adjusted to have a frequency difference of 28 GHz with respect to the main laser. Lights from both lasers are polarization matched and fed into an EDFA for edge-coupling. The photocurrent is 1.5 mA during measurement. A 27.9 GHz LO signal is used to mix the 28 GHz beat note down to 100 MHz for comparison with the 100 MHz reference signal. The feedback control voltage is send back to the piezo port of the follower laser for locking. Since the piezo port of the follower

laser has a limited bandwidth of 10 kHz, the loop bandwidth is set as 10 kHz as well.

Fig. 12 shows the comparison of the measured instantaneous waveforms of the locked and the free-running beat notes at 28 GHz with a span of 50 kHz. The locked signal achieved phase locking, demonstrating a clear peak at 28 GHz. Moreover, phase noise is improved within the 10 kHz loop bandwidth. For comparison, the measured free-running beat note shows a broad linewidth and it drifted over time. To prove the stability of the locking over time, Fig. 13 shows the measured free-running and locked beat notes over 72 seconds using the max hold function on the ESA. The free-running beat note drifted back and forth within 5 MHz during this time period. In comparison, the locked beat note stayed consistently at 28 GHz.

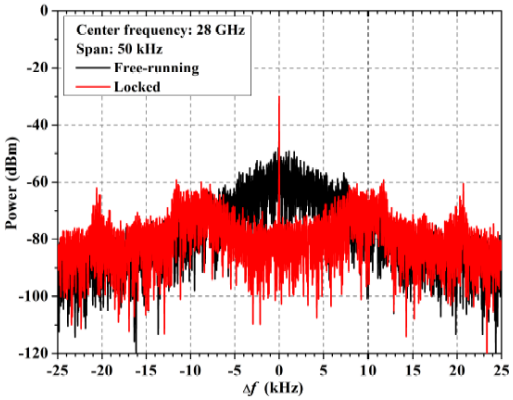

Fig. 12. Comparison of measured free-running and locked beat notes at 28 GHz.

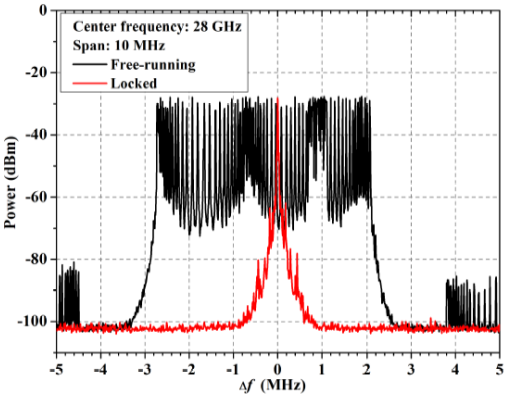

Fig. 13. Measured free-running and locked beat notes at 28 GHz over 72 seconds.

In order to show the phase noise improvement in locking condition, the phase noises of the locked beat note and the free-running beat note along with the phase noises of the LO signal and the reference signal are measured. The measured results are plotted in Fig. 14 with offset frequency up to 1 MHz. The loop bandwidth is 10 kHz which is limited by the bandwidth of the piezo port on lasers.

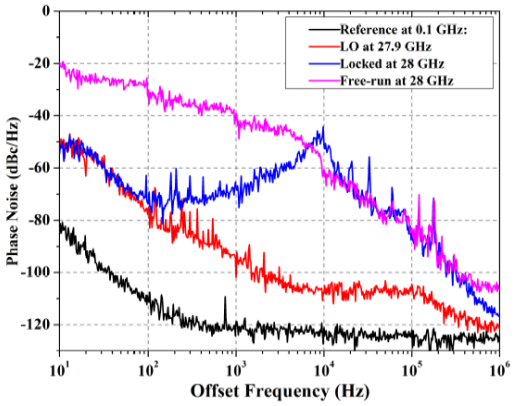

Fig. 14. Measured phase noises of the free-running beat note at 28 GHz, locked beat note at 28 GHz and the phase noises of the LO at 27.9GHz and reference at 0.1 GHz.

The free-running beat note has a high phase noise with -20 dBc/Hz at 10 Hz offset frequency and -50 dBc/Hz at 10 kHz offset frequency. When locked, the system phase noise within the loop bandwidth is determined by the phase noise from the LO signal and the phase noise from the reference signal. Their noises are considered uncorrelated because they are provided by independent signal generators. Since the frequency of the LO signal (27.9 GHz) is much higher than the reference signal (0.1 GHz), phase noise from the LO signal is worse than that from the reference signal, dominating the system phase noise performance within loop bandwidth. As shown in Fig. 14, the phase noise of the LO signal starts at -50 dBc/Hz at 10 Hz to -105 dBc/Hz at 10 kHz. When the beat note is locked, the phase noise is improved within the 10 kHz loop bandwidth. At lower offset frequency where the open-loop gain is sufficiently high, the phase noise of the locked beat note is improved to be as good as that of LO signal up to 60 Hz. As offset frequency increases close to the loop bandwidth of 10 kHz, the phase noise of the locked signal is still improved but not as good as the phase noise of the LO. As offset frequency is higher than loop bandwidth, the phase noise of the locked beat note is same as that of the free-running one as expected. The phase noise of the locked beat note could be improved as good as the LO signal to a higher offset frequency if commercial lasers with wider loop bandwidth are available. However, the piezo port of the current lasers have a limited bandwidth of to 10 kHz, limiting the phase noise performance of the whole system. In another approach, the driving circuit for the laser diode could be custom designed on the electronic chip to achieve wide loop bandwidth if the model of the laser is well-understood.

C. Measurement from 10 GHz to 40 GHz

In this section, the beat note is locked in a wide frequency range continuously from 10 GHz to 40 GHz, showing the compatibility with various communication standards within this range.

Fig. 15 shows that beat note is successfully locked at 10 GHz, 20 GHz, 30 GHz and 40 GHz, demonstrating a wide

continuous locking range. During these measurements, the wavelength of the main laser is constantly set at 1550.32 nm and the wavelength of the follower laser is set accordingly to have proper offset frequency. The frequency of the LO signal is set 100 MHz below the beat note, resulting to a 100 MHz IF signal to be compared with the reference signal. It should be noted that the proposed OPLL is capable of locking any arbitrary frequency from 10 GHz to 40 GHz due to the analog nature.

Fig. 16 demonstrates the improved phase noise within the loop bandwidth of 10 kHz when locked from 10 GHz to 40 GHz. As discussed in Section IV.B, the system phase noise is determined by the phase noise from the LO signal within the loop bandwidth because the phase noise of the LO signal is higher than that from the reference signal as shown in Fig. 16. The free-running beat note has a high phase noise with -20 dBc/Hz at 10 Hz offset frequency and -50 dBc/Hz at 10 kHz offset frequency. When the beat note is locked, the phase noise improved significantly within the 10 kHz loop bandwidth. The loop bandwidth is limited by the bandwidth of the piezo port on lasers. At lower offset frequency, the phase noise of the locked beat note is as good as that of the LO signal due to the sufficiently high open-loop gain. As the offset frequency increases up to loop bandwidth of 10 kHz, phase noise of the locked beat notes gradually increases due to the drop in open-loop gain. When offset frequency is higher than loop bandwidth, the phase noise of the locked beat note is same as that of the free-running one because the OPLL cannot improve phase noise outside loop bandwidth. If lasers with wider bandwidth at piezo port are available, the proposed OPLL could improve the phase noise of the locked beat note in a wider offset frequency.

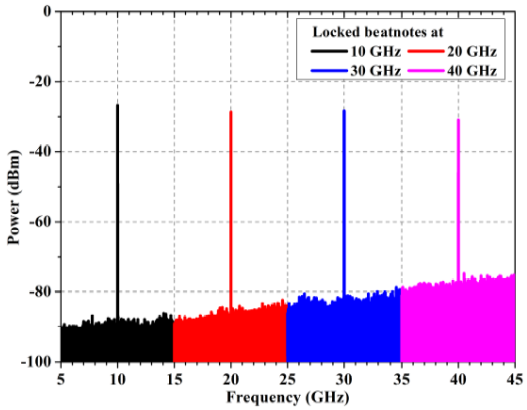

Fig. 15. Measured locked beat notes at 10 GHz, 20 GHz, 30 GHz and 40 GHz.

V. Conclusion

A compact integrated OPLL is presented in paper. It is a heterogeneous integration of a PIC with an EIC to achieve compact circuit size and reduce loop delay. With the help of the on-chip mm-wave mixer, the locking range is greatly extended. Moreover, impedance matching between the PIC and the EIC is detailed discussed to ensure a continuous wide frequency locking range from 10 GHz to 40 GHz. In measurement, the phase noise is significantly improved within the loop bandwidth from -30 dBc/Hz to -70 dBc/Hz at 100 Hz offset frequency.

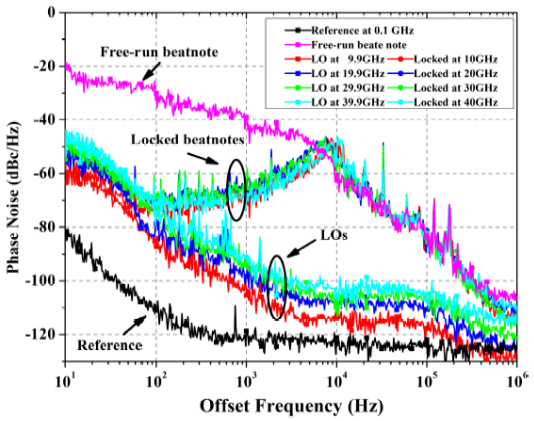

Fig. 16. Measured phase noises of the free-running beat note and the locked beat notes from 10 GHz to 40 GHz, and the phase noises of reference signal and the associated LOs.

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