*Signal Processing to Improve Speed and Accuracy of Electrical Impedance Tomography Imaging

Hoang Van Tran*[a], Vu Huu Pham [b], Thong Chi Le [b], Hargsoon Yoon [ab]
[a] Center for Materials Research, [b] Department of Engineering,
Norfolk State University, 700 Park Avenue, Norfolk, VA, USA, 23504

ABSTRACT

Electrical impedance tomography (EIT) is a rising and emerging imaging technique with great potential in many areas, especially in functional brain imaging applications. An EIT system with high speed and accuracy can have many applications to medical devices supporting in diagnosis and treatment of neurological disorders and diseases. In this research, EIT algorithms and hardware are developed and improved to increase reconstructed images' accuracy and decrease the reconstruction time. Due to multiplexer design limitations, EIT measurements are subject to strong capacitive effects from charging and discharging in switching cycles around 300 to 400 samples per 1280 samples (in 10 milliseconds sampling). We developed an algorithm to choose data in steady-state condition only selectively. This method improves the signal-to-noise ratio and results in better reconstruction images. An algorithm to effectively synchronize the beginning points of data was developed to increase the system's speed. This presentation also presents the EIT system's hardware architecture based on Texas Instruments Fixed-Point Digital Signal Processor - TMS320VC5509A, which is low-cost, high potential in popularity the community in the future. For high operation speed, we propose the EIT system used Sitara™ AM57x processors of Texas Instruments.

Keywords: Electrical Impedance Tomography, Brain Imaging, Speed, Accuracy

1. INTRODUCTION

Electrical Impedance Tomography (EIT) is the imaging technique for reconstructing the human body's impedance distribution. By injecting alternative electrical current to electrodes attached to the human body's surface, the voltage values at all electrodes are collected and processed to reconstruct the image for displaying the impedance distribution of the human's tissues. EIT is a non-invasive, radiation-free, and low-cost imaging method that is very potential in medical diagnosis applications [1][3].

Neural electrical impedance tomography reconstructs the image that monitors impedance change of brain tissue associated with neural activity [2][4]. For monitoring the fast impedance change in the brain, the continuous injecting current and measurement voltage are implemented with high speed and accuracy in addition to the improvement of the algorithm in image reconstruction. Successfully implementing the neural EIT system will bring brain function monitoring devices more popular in the future, preventing many people from brain stroke.

In this paper, we propose some techniques that can be applied to improve the accuracy and speed of neural EIT. First, we reduced the charging and discharging effect of the capacitor each time the multiplexer switching. The data at the beginning time of multiplexer switching is invalid in contributing to the image reconstruction step and making noise to overall data capture. By choosing only the data at the steady-state, we reduce the duration of data capture, the amount of data, and noise that increase the overall EIT system's performance. Second, because the data, the voltage values at all electrodes, contain much noise, included offset voltage and high-frequency noise, we apply the band-pass filter to improve the data's quality. Then an algorithm synchronizes the beginning point of data capture that only records two cycles of sine wave but still guarantees data sufficiency for image reconstruction. This technique reduces the amount of computation and increases system speed significantly.

Our neural EIT system includes multiplexers, analog-to-digital converter (ADC), alternative electrical current source, and processor for control and data processing. The alternative electrical current source generates the current source with 50 μA amplitude, 1725 Hz frequency used for injecting to a pair of the electrode over 16 electrodes total [5].

* h.v.tran@spartans.nsu.edu; nsu.edu/cmr

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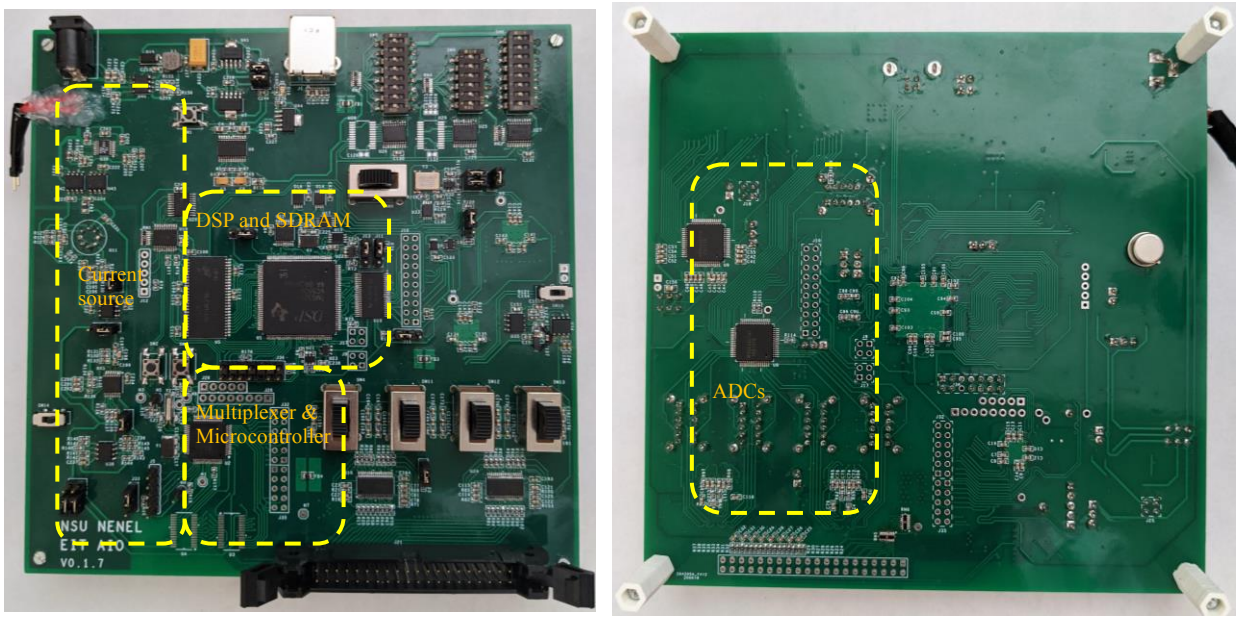
Multiplexers are used to switch the injecting current source to the next pair of electrodes after a period. ADC samples the voltage values at all 16 electrodes to store temporarily in SDRAM by the processor before sent to the computer to reconstruct the image that describes the impedance distribution in the brain. The hardware design was considered to ensure the total cost is at a low price aimed at low-cost devices that could be popular in the community in the future. The measurements are performed based on the round phantom model that is attached with 16 electrodes.

The architecture of our EIT system is introduced in section 2. Signal processing for improvement system's performance is described in section 3. The experiment setup and measurement results are indicated in section 4 and section 5. Finally, some discussion and propose for further developing the system is presented in section 6.

2. SYSTEM DESCRIPTION

The Neural EIT prototype board is shown in Figure 1; it includes an Alternative Electrical Current Source, two 16-to-1 Multiplexers chips & Microcontroller (ARM-Cortex M4), two 8-channels ADC chips (ADS1278), Digital Signal Processor (DSP - TMS320VC5509A) & SDRAM.



(a) Top (b) Bottom

Figure 1. The Neural EIT system prototype board based on Fixed-Point Digital Signal Processor - TMS320VC5509A

Figure 2 presents the block diagram of the Neural EIT system. The DSP is responsible for communication with PC, getting sample data from ADCs, and sending control signals to ADC and Microcontroller & Multiplexer (Section 2.1). Two ADC chips are used to convert the voltage at all electrodes to the digital signal temporarily stored in SDRAM by DSP before was transferred to PC for further image reconstruction algorithm (Section 2.2). Analog alternative electrical current source creates the alternative current with 50 μA amplitude and 1725 Hz frequency (Section 2.3). Multiplexers & Microcontroller receive the DSP control signal and switching pair of electrodes for injecting the current source every ten milliseconds (Section 2.4).

2.1 Digital Signal Processor and SDRAM

We used TMS320C5509 DSP, a fixed-point DSP with 8.33ns instruction cycle time with a 120 MHz clock rate. DSP communicates with the PC via the USB connector. DSP receives the configuration signals from PC, includes ADC data sampling rate, duration in injecting current to pair of electrodes before switching to next pair. Besides, the time that begins to run the system is also sent from PC to DSP. DSP is responsible for sending a trigger signal to Multiplexer & Microcontroller to synchronize ADC data capture and the current source injection. Finally and most importantly, DSP gets data from ADCs temporarily stored at SDRAM before packaged to the data block and sent to the PC. These data are processed and used for reconstructing images by EIDORS [6].

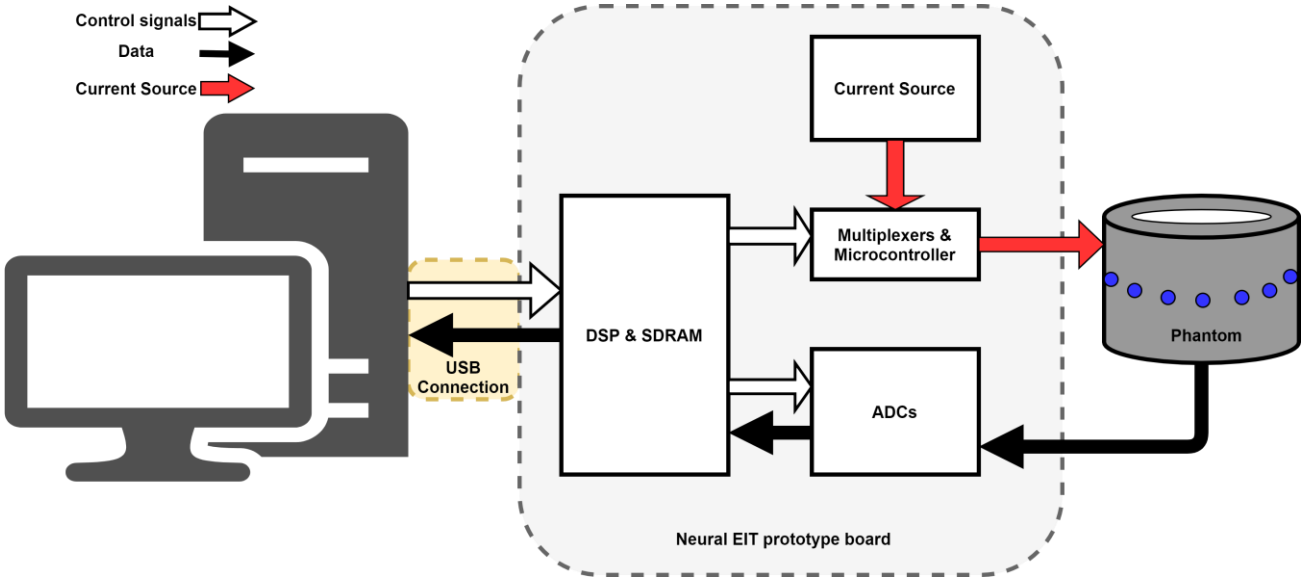


Figure 2. Block diagram of Neural Electrical Impedance Tomography system

2.2 Analog to Digital Converter (ADC)

For system integration of EIT hardware and improved performance, the 24-bit, delta-sigma (ΔΣ) ADC has been set up with ADS1278 for a data rate of up to 144k samples per second, allowing simultaneous sampling of 8 channels in parallel. Our neural EIT system uses two ADS1278 chips that provide 16 channels that can digitize 16 input signals in parallel. Serial Peripheral Interface (SPI) or Frame Synchronization (Frame-Sync) protocol can be used to communicate between ADS1278 and DSP. Daisy-Chaining of two ADS1278 is used to output data on a single pin that can reduce the usage pins of DSP. The DOUT1 data output pin of one device is connected to the DIN of the next device.

2.3 The analog alternative electrical current source

We designed a Neural EIT system's current source to build a pure analog current source with low amplitude, stable and undistorted current of 50μA. In this current source block, there are six different stages, including 1) a fixed 1725Hz analog oscillator circuit using a 3-stage RC phase shift oscillator, 2) a voltage follower buffer to avoid source loading, 3) a high pass filter, 4) a low pass filter, 5) an attenuator, and 6) an improved Howland current source. The simulation of the design using all the stages mentioned above was performed with various electrical parameters using MultiSim software. Besides, the real current source circuit was tested to make sure its operations are correct.

2.4 Multiplexers and Microcontroller

Two analog 16-to-1 multiplexers are used in our Neural EIT system, responsible for routing the source and sink pins of the current source to the pair of electrodes of the phantom every ten milliseconds. ADG1606 is monolithic iCMOS® analog multiplexers comprising 16 single channels. The ADG1606 switches one of 16 inputs to a common output, as determined by the 4-bit binary address lines (A0, A1, A2, and A3). The ultralow on resistance and on-resistance flatness of these switches make them ideal solutions for data acquisition and gain switching applications where low distortion is critical.

The Microcontroller that is used in this block is ARM Cortex-M4F based microcontrollers from Texas Instruments, TM4C123GH6PM. We use this Microcontroller to reduce the DSP task load since DSP only needs to send a trigger signal to the ARM microcontroller via Inter-Integrated Circuit (I2C) protocol or General-purpose input/output (GPIO). ARM Cortex-M4F, after that, is responsible for controlling two multiplexer ADG1606 chips.

For supplying power for the whole Neural EIT system to operation, the voltage regulators are implemented to provide dual voltage +15V/-15V and +5V/-5V, 3.3 V, and 1.8 V. The 2.5V reference voltage circuit is also designed to provide an accurate reference for ADC when sampling data.

3. SIGNAL PROCESSING FOR SYSTEM IMPROVEMENT

3.1 Reducing the capacitor charging and discharging effect each time switching the current source

At each time switching current source from the one pair of electrodes to the new pair of electrodes, the capacitor charge or discharge causes unstable data from the channels (electrodes). This inconsistent data affects the root mean square (RMS) value of the channel's data at this duration. Although the charging and discharging occur at the beginning of switching the current source and this process's duration is short. Still, this effect reduces the accuracy of the RMS value of the signal in the electrode channel, affecting the accuracy of the final reconstruction image. Figure 3 shows the data in Channel 1 in which the red rectangle notes the effect of charging and discharging of the capacitor to the data at the time switching current source.

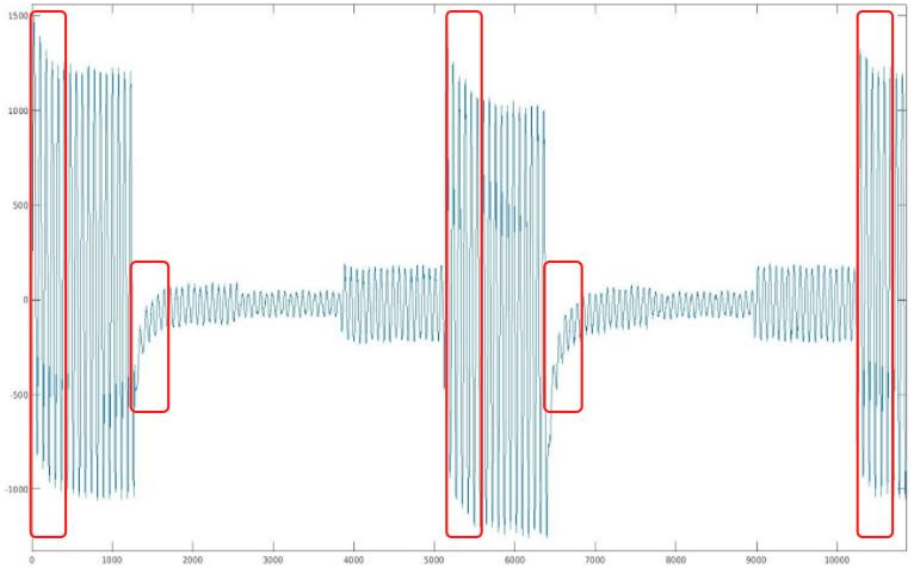


Figure 3. Data got from Channel 1. The red rectangles note the effect of capacitor charging and discharging to the data on Channels.

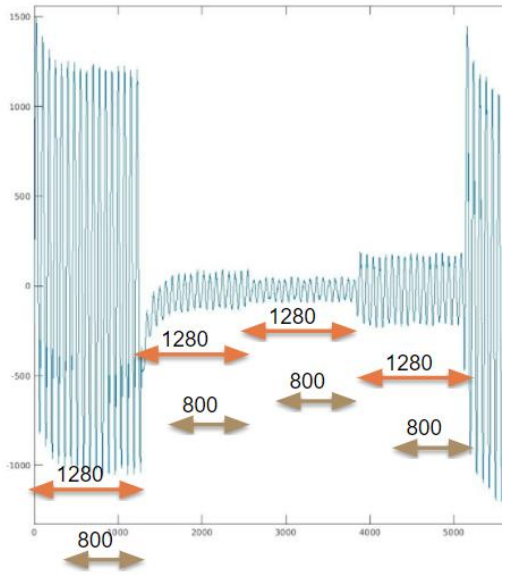


Figure 4. Ignoring the data at the time of the capacitor charging or discharging each time switching the current source. Only get 800 samples per 1280 samples at the position that the data is stable.

In our project, the duration of injecting the current source to the electrodes is ten milliseconds before switching to the new pair of electrodes. With the sampling rate of Analog-Digital-Converter (ADC) is 128 Ksps, every ten milliseconds, we will get 1280 samples. The EIT system with a strong effect from the capacitor, the charging or discharging time may hold 300 to 400 samples per 1280 samples (in 10 milliseconds sampling) like Figure 3.

By ignoring the sample data at the time of the capacitor charging and discharging each time switching the current source to the new pair of electrodes and only getting the data when the data sample is stable (Figure 4), using this stable data to the next steps in the reconstruction image, we figure out the improvement in the results.

3.2 Improvement in synchronous and collecting data to speed up the system

From Figure 3, the duration of injecting the current source to the pair of electrodes is ten milliseconds. The current source frequency is 1725 Hz; thus, in 10 milliseconds, we can get more than 17 cycles of sine wave samples. In the next steps of reconstruction image processing, we use 17 cycles to calculate the root mean square (RMS) value of this sine wave. For the EIT system that incurs the high effect of noise, more cycles sine wave for calculating the RMS value can reduce noise and increase accuracy, but this leads to reducing the system's speed.

By applying the bandpass-filter (1000 Hz – 3000 Hz) right after collecting the ADC data, we reduce the noise from the data. Zero-point was detected on the data at channel one and get only two since wave cycles. The data of other channels (channel 2, 3, 4, …) were aligned with channel 1. Figure 5 shows the data on channel 1 with two sine wave cycles for each time of injecting the current source to the pair of electrodes.

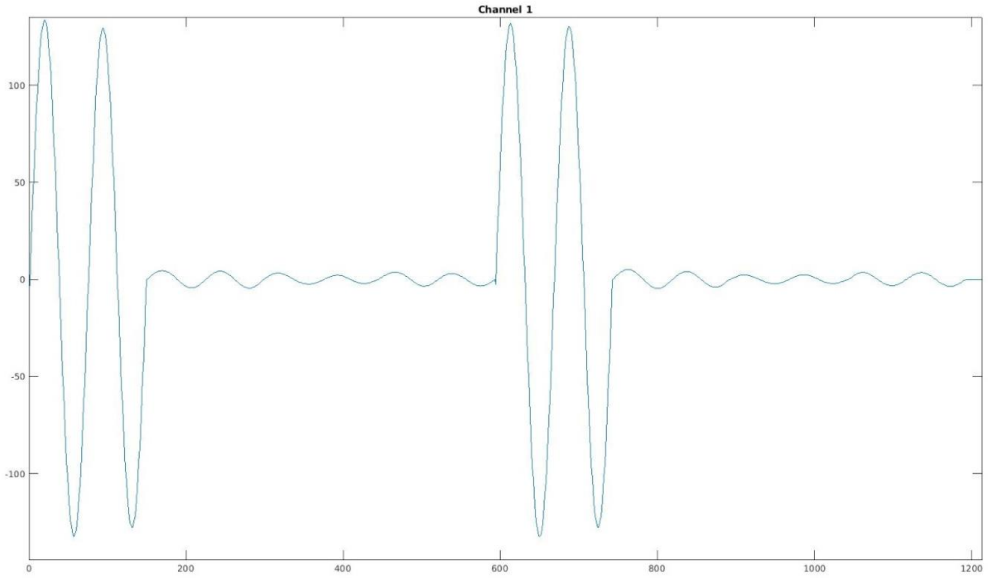


Figure 5. Two sine wave cycles data with the detected zero-point for each time of injecting current source to the pair of electrodes

The results that will be shown in the Results Section (Section 5.2) can confirm that the image reconstruction from the two sine wave cycles data (Figure 5) still has a good quality and stability.

4. EXPERIMENT SETUP

Although our Neural EIT system can operate with 16 channels input, we used 8 channels phantom model for measurements and testing our proposed improvement techniques. The reason is 8 channels EIT system has less data collection for image reconstruction, and therefore this system is harder to produce the image that describes the impedance distribution correctly inside the phantom. This system also incurs more affective from the noise that will clearly show improvement after applying the proposed technique. Figure 6 shows the eight channels phantom with an object inside. The phantom is filled with Phosphate-buffered saline (PBS).

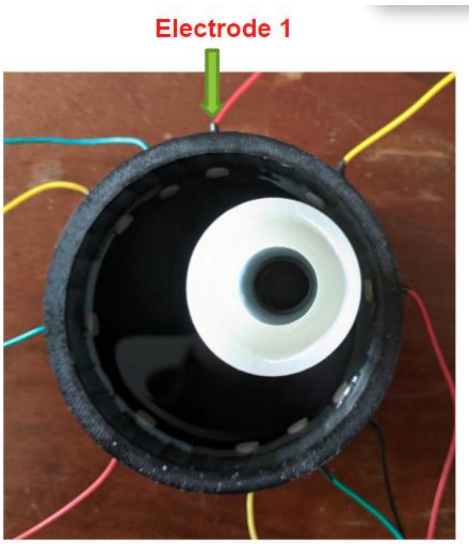


Figure 6. Eight electrodes phantom with an object inside.

5. RESULTS

5.1 Results from reducing the capacitor charging and discharging effect each time switching the current source

Figure 7 and Figure 8 show the reconstruction image results between the original data (1280 samples in 10 milliseconds) and selected 800 stable samples (by ignoring the data at the beginning of the switching time of the current source). Figure 7 indicates the effect of charging and discharging can make the unstable results in reconstruction image. In this case, the conductivity distribution in the real device does not change, but the reconstruction image shows the unstable or incorrect reconstruction process that was caused by the effect of charging and discharging of the capacitor. Better results were shown in Figure 8. By only getting 800 stable samples and ignoring unstable data, the results in reconstruction images are better. The conductivity distribution of reconstruction images is more correctly compared to in the real device.

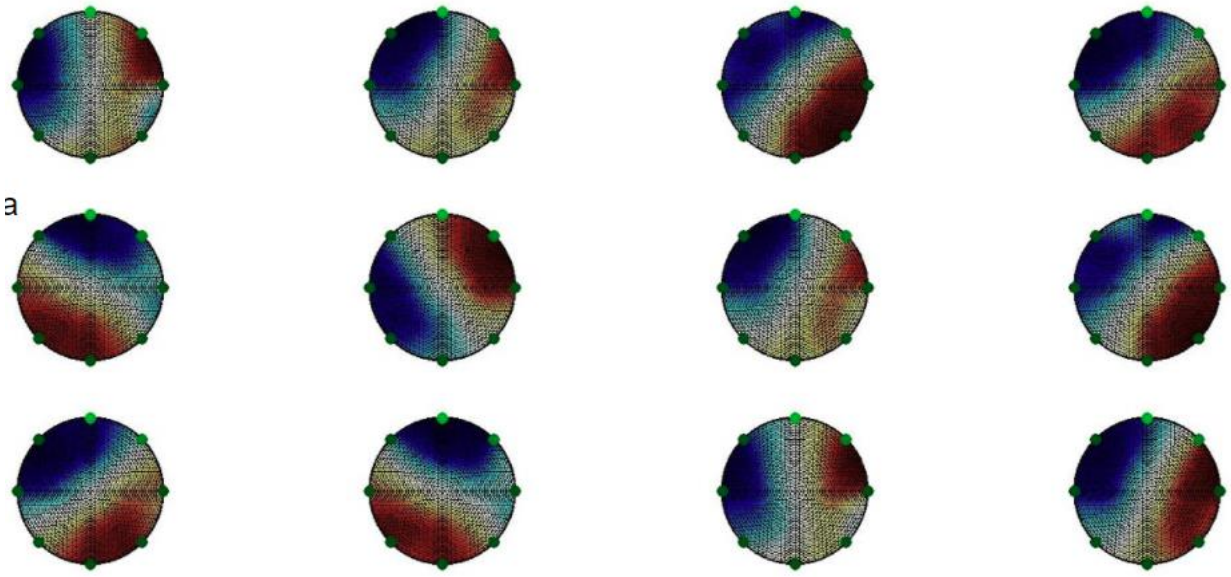


Figure 7. Reconstruction images that reconstruct from the full-data (1280 samples per 10 milliseconds)

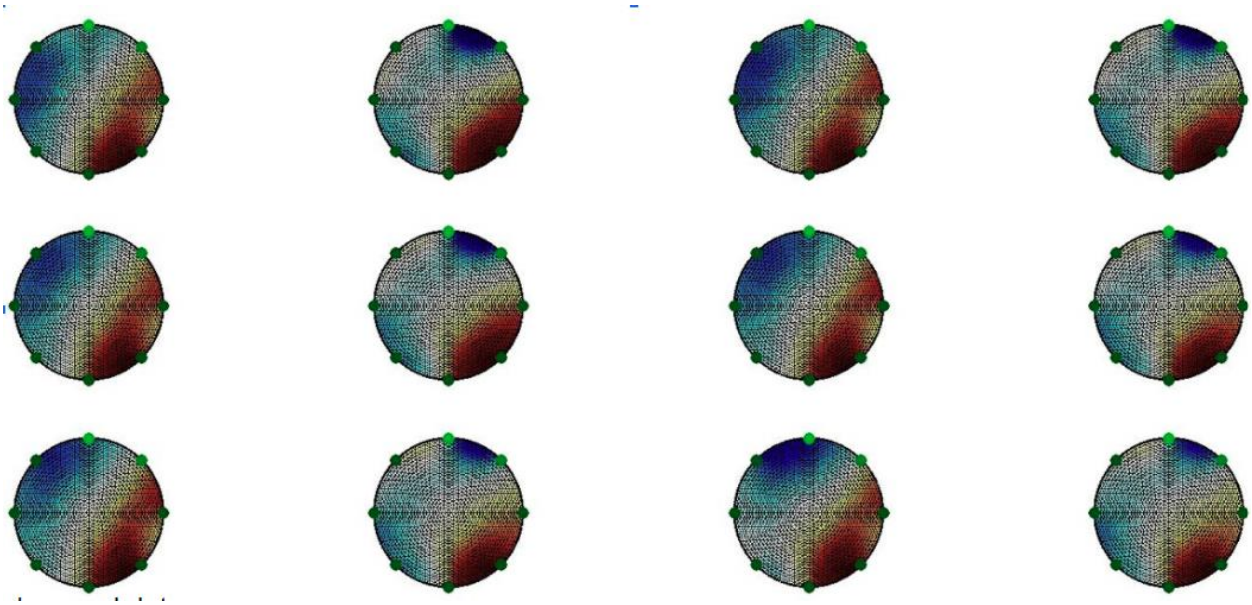


Figure 8. Reconstruction images that reconstruct from the 800 samples stable data (only use 800 stable samples / 1280 samples)

5.2 Improvement results in synchronous and collecting data to speed up the system

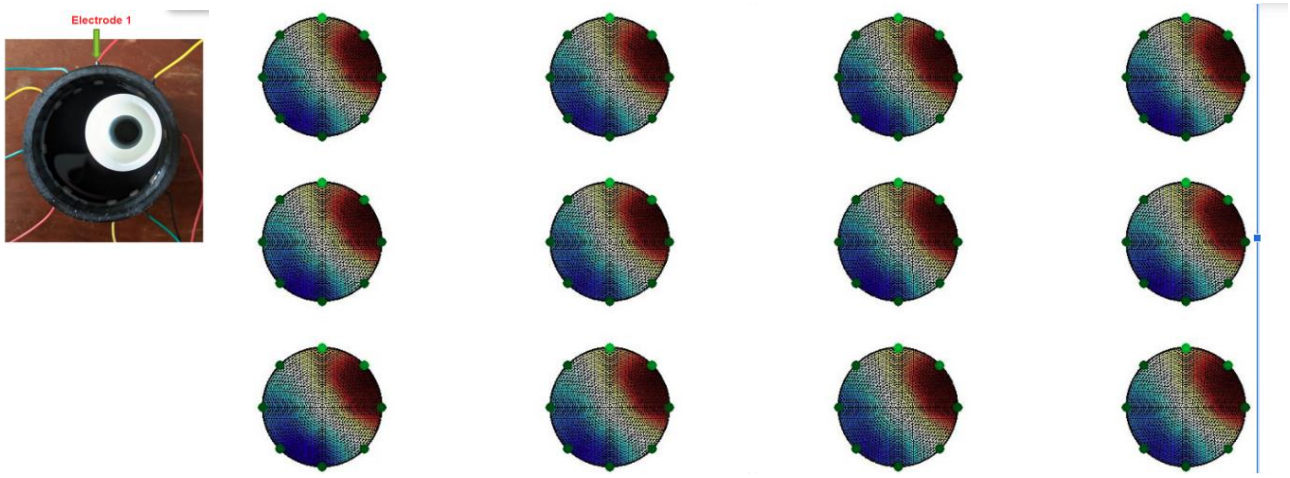


Figure 9. Reconstruction images were created from the data that were collected by the method illustrated in Figure 5

As shown in Figure 9, the reconstruction images that were created from the data collected by the above method are good and very stable. By improving synchronous and collecting data in this way, the system's speed also much more increase.

6. DISCUSSIONS AND CONCLUSIONS

Our main goal is the improvement of the EIT system's speed and accuracy. Although these techniques can use to increase the speed and accuracy of the EIT system, the limitation of hardware is easily recognized. The TMS320VC5509A fixed-point digital signal processor (DSP) is the single-core low-power DSP. This DSP is more suitable for low-power consumption applications than high-performance systems. DSP provides the USB 1.1, which has bandwidth limited to about 1 MB/s. The limitation of USB 1.1 does not allow all 8 channels or 16 channels utilization with a high sampling rate for a long time. Transfers are performed using the maximal possible buffer size for BULK transfers (close to TMS320VC5509A's limit 64kB), which maximizes performance. We used 16 MB of SDRAM memory as cyclic buffer stores data before the transfer, and in case of overflow, the acquisition is stopped but gathered

data can be transferred to PC. This reduces the limitation of USB 1.1 transfer possibilities, but the buffer still overflow if the ADC runs with a high sampling rate for a long time.

To increase the EIT system's performance, we propose to use BeagleBoard-X15, which has Sitara™ AM572x processors. Sitara AM572x possesses dual-core Arm Cortex-A15, two TI C66x floating-point DSP cores, two Arm Cortex-M4 cores, and especially four programable real-time units (PRU) (Figure 10). We propose two cores of PRU are used to control the current source and other peripheral, while the other two cores of PRU are used to reading ADC data from two ADS1278 chips. Two DSP cores and two ARM Cortex-M4 cores support ARM Cortex-A15 in processing data to increase the EIT system's speed.

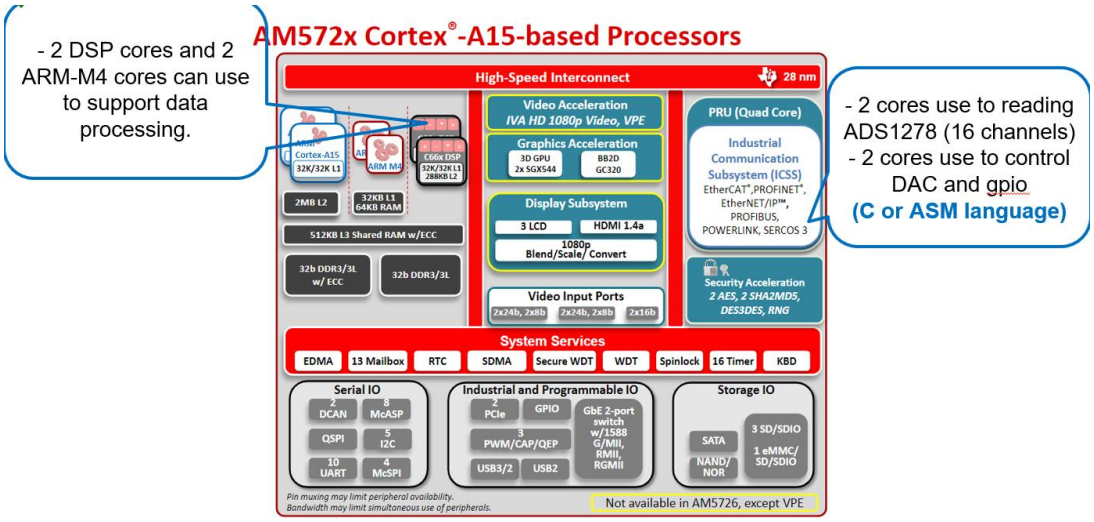


Figure 10. Sitara™ AM572x processors architecture (Texas Instruments)

ACKNOWLEDGMENT

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