CHEMISTRY OF MATERIALS

pubs.acs.org/cm

Article

Pathway to Increase the Tolerance of Organic Transistors to Semiconductor Purity

Published as part of the Chemistry of Materials virtual special issue "In Honor of Prof. Elsa Reichmanis".

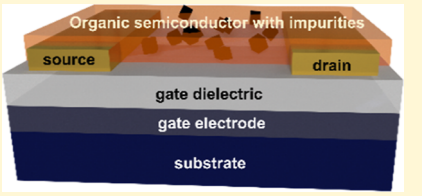
Matthew Waldrip, Yue Yu, Rudolph Holley, III, Yueh-Lin Loo, John E. Anthony, and Oana D. Jurchescu*

Cite This: *Chem. Mater.* 2023, 35, 8645−8653

Read Online

ACCESS | Metrics & More | Article Recommendations | Supporting Information

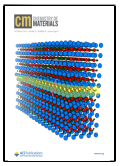
ABSTRACT: Organic semiconductors (OSCs) have attracted rapidly growing interest given their potential to create innovative optoelectronic applications. One major drawback is the sensitivity of the electrical properties to the presence of impurities in the OSC film: even small traces can significantly alter the properties of the OSC layer by introducing electronic trapping states, leading to efficiency losses and degraded charge carrier mobility. Since impurities can be introduced at many stages of device fabrication, from synthetic impurities to process solvents to the lining on syringes used to deposit solutions, identifying device structures that are more tolerant of their presence is necessary. Here, we employ a data-driven device design, wherein simulations are combined with experiment to reveal organic field-effect transistor (OFET) geometries that enable the use of lower standards of semiconductor purity without impacting the performance. The phenomenon is attributed to how the filling of trap states is modulated by the gate potential. Guided by the simulation results, we were able to recover the performance of a pure device in OFETs with optimal geometry containing 2% known impurity. These results provide a pathway for developing high-performance organic devices at a lower cost by adopting a device architecture that is more tolerant of defects..



1. INTRODUCTION

Organic semiconductors (OSCs) have evolved from intriguing materials decades ago to serious contenders for many technologies, currently being incorporated in several market applications.[1,2] The appeal comes from the fact that they can be casted from solution, which facilitates low-cost processing at room temperature on a wide variety of substrates, including flexible and bendable.[3] Additionally, due to the nearly infinite number of possible chemical structures, their composition can be tuned for specific applications, from optimizing mechanical flexibility to sensing and energy technologies.[4−6] The presence of impurities in the OSC layers can alter their properties significantly, from enhancing the conductivity in the case of doping[7−10] to severely restricting the device performance when unintentional impurities create electronic trapping states.[11−13] Damaging effects include radiative losses and accelerated degradation in organic solar cells and organic light-emitting diodes (OLEDs)[14−17] and reduction in charge carrier mobility, increase in the off-currents, subthreshold slope, and the threshold voltages in transistors, all resulting in greater power consumption. This is not surprising since even a few parts per million of impurity (dopant) can completely flip the behavior of inorganic semiconductors like silicon from p- to n-type and vice versa. Impurities are ubiquitous in OSCs—even high-quality single crystals can contain up to 100 ppm impurities—and they result from unreacted starting materials, which can form during processing and subsequent handling, or upon exposure to environment and bias stress.[16,18−26] Extensive material purification is an effective way to lower the impurity content, but it reduces the reaction yields and raises the final cost, making it even more challenging for scaling-up production. Several alternative approaches have been proposed that rely on mitigating the impurity content via material processing. For example, applying multiple sublimation cycles during single-crystal growth by physical vapor transport results in better purity and higher mobilities, but it adds to complexity, time, and cost.[23,27] Strategies for controlling thin-film microstructure and impurity distribution include incorporation of cosolvents;[28−31] postprocessing via solvent vapor annealing;[19] and adding dopants to neutralize the trap states generated by the presence of impurities.[32−37] While these methods do indeed improve device quality, they require extra processing steps or materials and each must be tuned to an individual semiconductor system.

Received: July 18, 2023
Revised: September 18, 2023
Published: October 13, 2023



Here, we employ a simulation-guided device design for organic field-effect transistors (OFETs), wherein simulations are used in conjunction with experiment to uncover the geometries by which the standards of semiconductor purity can be relaxed with minimal effect on the device performance. Running simulations on over 2000 distinct OFETs, we identified a general trend that increasing the capacitance of the dielectric layer minimizes the effect of the impurity-generated electronic traps, allowing us to incorporate a much broader range of semiconductor purities with minimal impact to charge carrier mobility. More specifically, the samples with 2% impurity concentration exhibited properties similar to those made on the pure OSC layer in OFETs with optimized geometry. To explain the results, we took a comprehensive look at the data provided by simulations and found that the magnitude of the dielectric capacitance affects the process of trap filling within the semiconductor layer. Specifically, OFETs based on high-capacitance dielectrics have a larger number of trap states neutralized at a given voltage, providing a greater fraction of free vs trapped charges. These results provide a strategy for fabricating low-cost, high-performance organic transistors by identifying the device architectures that are more tolerant of defects.

2. EXPERIMENTAL SECTION

2.1. TCAD Simulations. Numerical TCAD simulations were carried out in the Silvaco Atlas program suite. These simulations are physically based; differential equations based on Maxwell's laws are solved between nodes on a finite element analysis (FEA) grid that represents the volume of the transistor, ensuring that Coulomb's law, Boltzmann statistics, and drift-diffusion models are all satisfied. Each simulation used over 200,000 FEA connections to ensure the accuracy of solutions. Simulated OFETs were in the coplanar bottom gate, bottom contacts (BGBC) configuration. The channel length L was 30 μm, and the obtained $I-V$ curves were normalized to a channel width W of 1000 μm. The semiconductor lowest unoccupied molecular orbital (LUMO) and highest occupied molecular orbital (HOMO) levels were set to −3.7 and −5.4 eV, respectively. Source and drain contacts were modeled as conductors with a work function of 5.4 eV to simulate an OFET with a minimal Schottky injection barrier; this work function value well-represents the Au treated with pentafluorobenzene thiol (PFBT) used in the experimental effort. The "Universal Schottky Tunneling model" was selected for charge injection at the contact/semiconductor interface with surface recombination enabled.[38] The dielectric constant of the gate dielectric was set to ε_r = 2.1, and C was varied from 1.4 to 372 nF/cm^2 by altering the dielectric thickness from 5 to 1300 nm. Bias conditions were as follows: drain−source voltage V_{DS} = −3 V, with the source contact grounded, and gate−source voltage V_{GS} ranged from 0 to −60 V to create the transfer $I-V$ curve in the linear regime. Simulated OFET mobility μ was extracted from the transfer curves using standard procedures.[39]

The trap density of states (trap-DOS) spectra were programmed as a sum of two or three exponential terms, following the form

$$N(E) = n_1 \times e^{-E/E_1} + n_2 \times e^{-E/E_2} + n_3 \times e^{-E/E_3} \quad (1)$$

where $N(E)$ is the number density per eV per cm^3 as a function of energy E above the valence band; n_i is the amplitude of the respective exponential; and E_i is the characteristic energy of the exponential.

2.2. Transistor Fabrication. Substrates consisted of heavily doped silicon (n-type Si^{++}), acting as the gate electrode, with a 200 nm layer of thermally grown SiO_2. They were cleaned by rinsing with acetone for 30 s, followed by a 10 min acetone bath; acetone and isopropyl alcohol (IPA) rinse for 10 s each; 10 min IPA bath; IPA rinse (10 s); N_2 compressed gas drying; 10 min UV-ozone; deionized water rinse for 30 s; N_2 compressed gas drying. Next, the organic gate dielectric layers were deposited over SiO_2, to form a double or triple dielectric layer, as described below. To obtain a high-capacitance dielectric, parylene-C was deposited directly onto the SiO_2: substrates were loaded into a bespoke reactor, and parylene film growth was carried out in a quartz tube under vacuum (∼1 mTorr) to a thickness of 190 nm (evaluated postdeposition). Three temperature zones were used: first, the dimer di-*para*-xylene (Acros Organics) was heated to 120 °C to sublimate the dimer. The material then passes through a 700 °C furnace, which splits the dimer into monomers. The monomers then polymerize on the sample surfaces at room temperature to provide a conformal coating. Parylene has a surface energy high enough to allow OSC deposition by solution casting while also maintaining minimal gate leakage. The dielectric capacitance was reduced by spin-coating a layer of Cytop (CTL-809-M, AGC Chemicals) prior to parylene deposition, resulting in an 800 nm film of Cytop between the SiO_2 and parylene in triple-layer dielectrics. The Cytop films were cured by placing substrates in a vacuum oven at 50 °C for 8.5 h (including warming time, ∼20 min).

Au contacts were thermally deposited at a rate of 0.5 Å/s and a thickness of 40 nm through a shadow mask by using a Kurt Lesker (KJLC) Spectros deposition system at ∼10^{-7} Torr. Substrates where then rinsed with ethanol (EtOH) and placed in a 30 mM solution of PFBT (Sigma-Aldrich) in high-purity EtOH at room temperature for 30 min. Finally, the substrates were rinsed with EtOH for 30 s and dried with N_2 gas.

The small-molecule 2,8-difluoro-5,11-bis(triethylsilylethynyl) anthradithiophene (diF-TES-ADT) was synthesized following the known procedures.[40] The solutions used for device fabrication were 1.5 wt % in room-temperature chlorobenzene. To create the films with added impurities, 6,13-bis(triisopropylsilylethynyl)pentacene (TIPS-pentacene, aka TIPS-Pn) was added to the diF-TES-ADT solution in quantities of 2 and 10% by weight. Solutions were spin-cast at 1000 rpm for 80 s with a 7 s ramp; there was a 10 s hold from depositing the solution on the substrate to starting the spin-coater. Samples were annealed at room temperature under vacuum overnight.

2.3. Transistor Characterization. Transfer (I_D vs V_{GS}) and output (I_D vs V_{DS}) characteristics were measured with an HP 4155C semiconductor parameter analyzer in ambient atmospheric conditions and in dark. Gate leakage current was negligible for all devices. Mobility was extracted from the saturation regime curves by using the following equation

$$\mu_{sat} = \frac{2L}{WC}\left(\frac{\partial\sqrt{I_D}}{\partial V_{GS}}\right)^2 \quad (2)$$

where the partial derivative was extracted from a best-fit line of the square root of I_D vs V_{GS}. Uncertainty was reported as the standard deviation of the corresponding set of measured devices.

Quasi-static capacitance measurements were used to determine the dielectric capacitance of each dielectric. The semiconductor was gently scrubbed off the contacts of each substrate, leaving MIS structures of Si^{++}, SiO_2, Cytop (C_{low} devices only), parylene, and Au. Additionally, MIS structures of Si^{++}, SiO_2, Cytop, and Au; and Si^{++}, SiO_2, and parylene were fabricated at the same time as the transistors, and the CV measurements taken on these samples agreed with the transistor CV measurements. The directly measured capacitance values were used for the mobility calculation.

Grain size was computed from scaled optical micrographs by manually tracing grain boundaries and analyzing the resulting traced grains in ImageJ. Averages were weighted by grain size so as to give the probability of grain size for a random point on the sample. Error is the 95% confidence interval (CI).

2.4. Structural Characterization. Grazing incidence wide-angle X-ray scattering (GIWAXS) measurements were performed at National Synchrotron Light Source II at Brookhaven National Laboratory on the 11-BM beamline. An average wavelength of 0.918 Å (13.5 keV) was used, and the incident angle was set to be 0.08°, which is between the critical angles of the substrate and the films. The scattered X-rays were collected on a hybrid pixel detector, and all GIWAXS images have been background-subtracted. The

https://doi.org/10.1021/acs.chemmater.3c01792
Chem. Mater. 2023, 35, 8645−8653

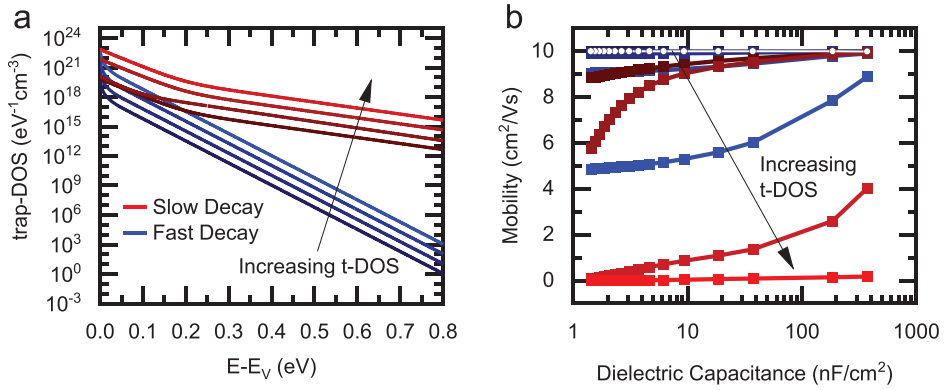


Figure 1. (a) t-DOS spectra as a function of energy above the valence band (0.0 eV is band edge) used in simulation. Two types are displayed: exponentials that decay quickly (blue curves) or slowly (red curves) into the bandgap. (b) Device mobility as extracted from simulations on coplanar OFETs incorporating the trap-DOS spectra from panel (a). White corresponds to a trap-free device.

background-subtracted GIWAXS patterns were fit using the DPC Toolkit to identify structural parameters and trends.[41]

3. RESULTS

3.1. Simulated Device Properties in OSCs of Varying Trap Spectra. Traps are omnipresent in OSCs due to the weak nature of the intermolecular interaction characteristic to these materials, and they manifest themselves as tail states that trail into the semiconductor bandgap.[11] Semiconductor purity, microstructure, thermal motion, interaction with environment, the processes occurring at the semiconductor/dielectric interface, electrical bias stress, and even light exposure can alter the trap density of states (t-DOS) from subtle variations to orders of magnitude.[11,13,34,42,43] To investigate the effect of the t-DOS on charge carrier mobility, we performed physically based, 2D numerical simulations of OFETs using Silvaco Atlas TCAD (technology computer-aided design) software. The t-DOS spectra in the OSC have been varied, as shown in Figure 1a: the curves are either a sum of two (red) or three exponential fits (blue) to t-DOS spectra. Functions of multiple exponentials are used to describe states in different regions in the bandgap; for instance, one term can describe the states near the mobility edge and another for deeper in the bandgap.[44−46] Here, the sum of two exponentials has been assigned terms with characteristic energies (E_i in eq 1) of 24 and 71 meV, while the triple sum has two terms to describe the behavior near the band edge at 1.7 and 6.3 eV and one term for deeper states at 19 meV (these values were the results of best fits to experimental data). To expand the scope of the simulation, the spectra were changed by varying the exponential coefficients (n_i in eq 1) over 4 orders of magnitude; the spectra with larger values of n_i are brighter in Figure 1.

The properties of transistors in the coplanar geometry and with areal dielectric capacitance (C) values ranging from 1.4 to 370 nF/cm^2 were calculated for each t-DOS spectrum, and the results are shown in Figure 1b. A trap-free device provided a baseline (white line/circles), and the programmed intrinsic semiconductor mobility was μ_i = 10 cm^2/(V s) for all calculations. The mobility in the devices consisting of a hypothetical trap-free OSC was identical to the intrinsic OSC mobility and exhibited no dependence on C, as expected from the gradual channel approximation.[39,47,48] However, in the presence of traps, our simulations predict that the OFET device mobility μ is inversely related to the t-DOS for a given C and increases drastically with C, up to the point that at large values of C there is almost no discernible difference in performance between the trap-free and realistic OSC t-DOS for several t-DOS cases. There appears to be nuances in the nature of the dependence of μ on C based on the shape of the profile: for devices with a slowly decaying t-DOS (red), the major increase in mobility occurs in the lower regime of C (less than 10 nF/cm^2), with the exception of two types with a large number of traps such that mobility near 10 cm^2/(V s) is never reached. On the contrary, for the devices with a faster decaying t-DOS (blue), the mobility has a larger dependence on C in the high-C range. The ability to minimize the effect of traps, as predicted by these results, means that when impurities or other defects are present in the semiconductor layer, OFET performance should be able to be recovered to the level of a device with a trap-free OSC in carefully controlled device architectures.

3.2. Recovering Device Performance in Experimental Transistors with Impurities. To test the predictions that device performance can be recovered by increasing the dielectric capacitance, we fabricated OFETs based on the small-molecule diF-TES-ADT, where we purposefully introduced known amounts of TIPS-pentacene impurity to represent an unrefined semiconductor, at concentrations of 2 and 10% by weight. DiF-TES ADT has been studied extensively in both single-crystal and thin-film configurations and was shown to form p-type transistor channels with mobilities up to 20 cm^2/(V s) in highly optimized films and device structures.[49−51] This molecule has excellent compatibility with solution casting, and high-quality films are achievable with a wide variety of processing methods, including those that are large-area compatible.[28,52−57] While the high-mobility OFETs were demonstrated in a staggered geometry, here we focused on OFETs in the coplanar BGBC geometry, despite the fact that they yield a lower mobility due to higher contact resistance (Figure 2).[58] This geometry was chosen since it provides a more facile fabrication of OFETs with a wide range of dielectric capacitance values, thus allowing us to screen a larger number of devices more efficiently.

We chose TIPS-pentacene as an impurity as it is similar in size to the diF-TES ADT; thus, the incorporation of the impurity should not introduce drastic strains in the diF-TES ADT crystals that would be detrimental to electrical properties.[55,59] The addition of TIPS-pentacene resulted in a substantial change to the properties of the solution, as can

https://doi.org/10.1021/acs.chemmater.3c01792
Chem. Mater. 2023, 35, 8645−8653

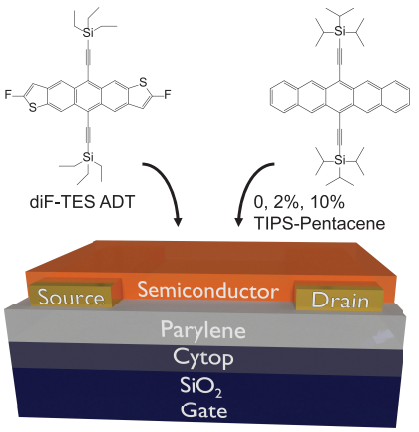


Figure 2. Bottom-gate, bottom-contact coplanar device structure used for the experimental OFETs. The small-molecule semiconductor diF-TES ADT was used in pure form or with 2 and 10% TIPS-Pentacene as an added impurity. The dielectric consisted of parylene on top of SiO_2 for high capacitance devices and Cytop/parylene on top of SiO_2 for low capacitance devices.

be observed by the considerable darkening in color, from a bright red in the pure diF-TES ADT solution to an almost-black crimson (Figure 3a–c); accordingly, there are differences in the morphology of the semiconductor films obtained from these solutions (Figure 3d–f). The thin films made from pure diF-TES ADT show a weighted average grain size of 560 μm^2 (95% CI: 485–632 μm^2; see Figure S1, Supporting Information), which is comparable to other films of diF-TES ADT deposited under similar conditions.[60−62] These films are characterized by platelet-like crystallites that span the length of the channel (a channel length maximum of 40 μm); this facilitates efficient charge transport, as it has been shown that there is a sharp decrease in mobility when these crystallites no longer span the channel.[60−62]

The samples containing the added impurity exhibit smaller grain sizes when compared to the pure film, with the 2 and 10% samples measuring 460 μm^2 (95% CI: 412–510 μm^2) and 425 μm^2 (95% CI: 384–463 μm^2), respectively. While the 2% samples have a slightly higher average domain size, the two spectra of domain size largely overlap. It should be noted that the local concentration of impurities may differ from the average composition in solution, for instance due to phase separation, and it is possible that some majority TIPS-pentacene domains are formed.[53,59] Additionally, the impurities can act as crystal seeding sites, which tends to decrease the crystal size as they are more densely seeded and start their growth closer to adjacent crystallites.[59] This in turn leads to a higher density of grain boundaries in the OFET channel that will degrade charge transport, amplifying the detrimental effects of impurities beyond creating discrete trapping centers.[60]

Representative $I-V$ curves for transfer characteristics in the saturation regime and output characteristics are shown in Figure 4a,b (these are taken from a pure sample; $I-V$ curves for the other samples are shown in Figures S2 and S3, Supporting Information). Turn-on and threshold voltage are less than 1 V, with a sharp subthreshold slope of 500 mV/dec, and the transfer curve exhibits a reliability factor of r = 98%

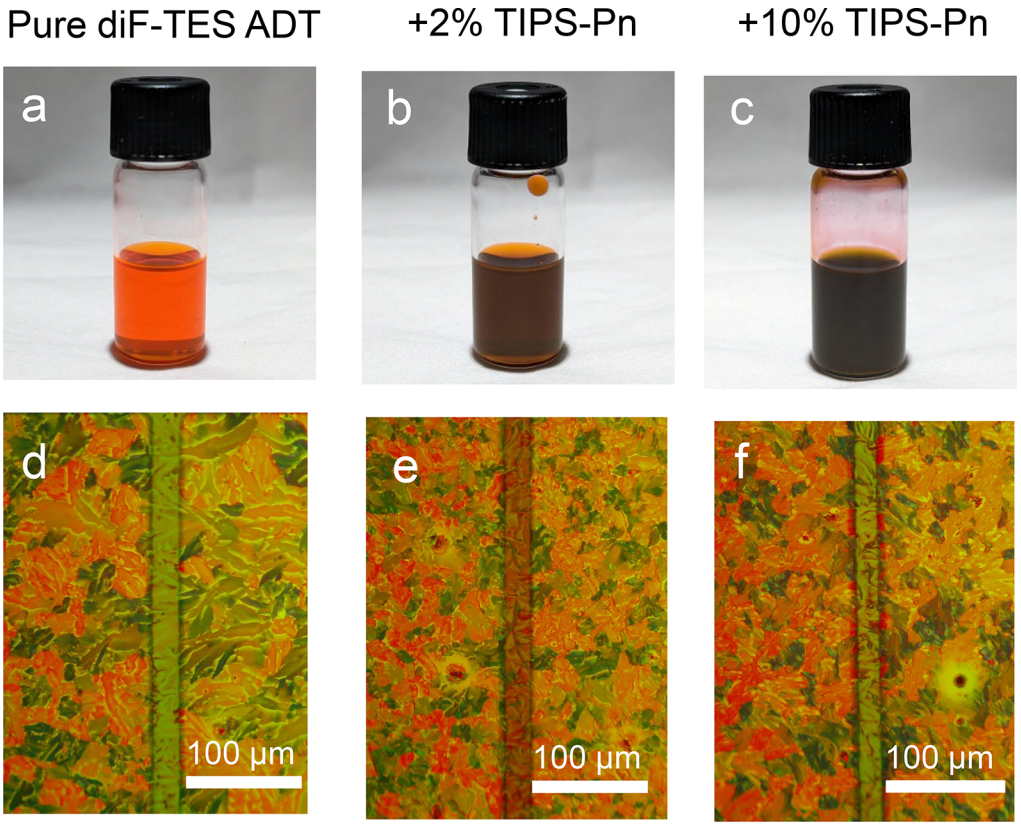


Figure 3. Photographs of diF-TES ADT solution in its (a) pure state and with TIPS-pentacene impurity added at (b) 2 and (c) 10%. (d) Corresponding film crystallization on OFETs for the pure solution and (e) 2% TIPS-pentacene and (f) 10% TIPS-pentacene.

https://doi.org/10.1021/acs.chemmater.3c01792
Chem. Mater. 2023, 35, 8645−8653

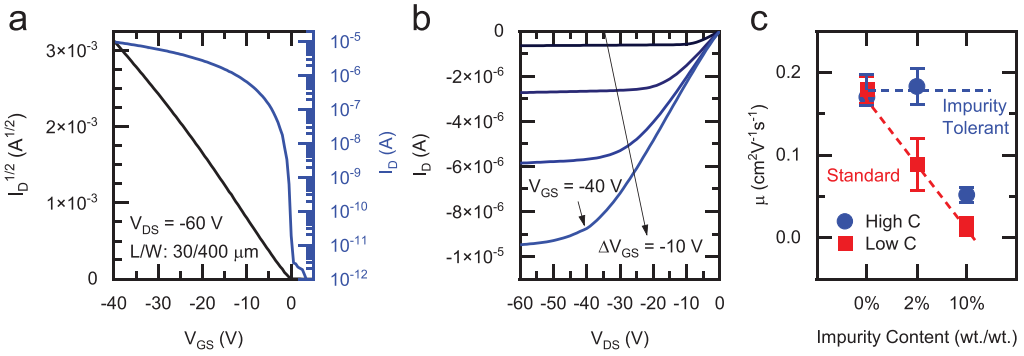


Figure 4. (a) Typical experimental transfer *IV* curve in the saturation regime and (b) corresponding output *IV* curves. (c) Experimental device mobility for samples of differing semiconductor purity. Error bars are the 95% CI. The blue horizontal line is a guide for the eye, representing the mobility value corresponding to the "pure" sample.

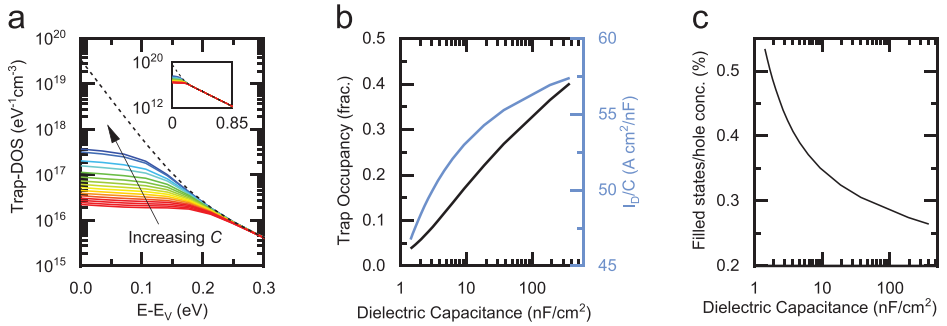


Figure 5. (a) Simulated occupation of trap-DOS with varying levels of dielectric capacitance (from C = 1.4 nF/cm^2 in red; to C = 370 nF/cm^2, in blue). Inset shows trap occupation from the HOMO level to semiconductor midgap. (b) Simulated trap occupancy as a fraction of the total trap-DOS spectrum and drain current normalized by C plotted as a function of C. (c) Simulated filled trap density as a fraction of hole concentration as a function of C.

(note that the reliability factor was greater than 80% in all tested devices and care was taken in extracting mobility to avoid overestimation).[63] OFETs of each of the three types of OSC purity levels were made with a high-capacitance dielectric (C_{high} = 7.9 ± 1.2 nF/cm^2) and a low-capacitance dielectric (C_{low} = 1.8 ± 0.3 nF/cm^2). Despite the smaller capacitance range tested experimentally versus simulation, due to the limitations in device fabrication, we still observed significant changes in device mobility (Figure 4c). The "pure" diF-TES ADT (as received, without additional purification) samples exhibited similar mobilities independent of the capacitance of the dielectric, namely, 0.2 ± 0.03 and 0.2 ± 0.02 cm^2/(V s) for the high- and low-capacitance devices, respectively, in accordance with the simulation predictions. These experimental mobility values are on par with values reported in the literature for OFETs based on this semiconductor in the coplanar configuration.[61,62,64] When TIPS-Pn impurities were added at the 2% level, the mobility decreased by half to 0.09 ± 0.03 cm^2/(V s) (red). Utilizing a high-C device design, however, we were able to completely recover the mobility to that of the pure samples, 0.2 ± 0.02 cm^2/(V s). Nevertheless, when increasing the level of impurities to an extremely high value, namely 10%, we could not recover the performance in the high-C samples, where we obtained a μ = 0.05 ± 0.01 cm^2/(V s). Even so, these devices still performed better than the devices with the low-C dielectric, where the mobility averaged 0.01 ± 0.01 cm^2/(V s). The threshold voltage exhibited a similar dependence, as shown in Table S1, Supporting Information. These results confirm the phenomenon predicted by the simulations that high-C OFETs are more resilient to trap states due to impurities.

GIWAXS measurements were performed on pure diF-TES ADT and TIPS-Pn films as well as diF-TES ADT films with 2 and 10% TIPS-Pn impurities to probe their structure. Interestingly, the diffractograms in Figure S4 (Supporting Information) suggest that diF-TES ADT films with 2% and 10% impurities cocrystallize and are structurally more similar to pure TIPS-Pn than they are to pure diF-TES ADT. As evidence of this, prominent diF-TES ADT features can be observed at q_{xy} = 0.94 and 1.1 which are qualitatively different than those in the 2% (0.80, 0.88, 1.1, and 1.3), 10% (0.80, 0.86, 1.1, and 1.3), and pure TIPS-Pn films (0.83, 0.85, 1.1, and 1.3). The GIWAXS patterns thus do not suggest a structural origin for the observed differences in mobility between the films containing impurities but may partially explain the mobility drop going from pure diF-TES ADT to impurity-containing films.

3.3. Dynamics of Trap Filling: Simulation Results. In order to understand the effect of the dielectric capacitance on the device mobility, we evaluated the trap-DOS occupancy for a given t-DOS spectra as a case study; here, C varied from 1.4 to 370 nF/cm^2 (Figure 5a—dashed line represents the complete trap-DOS spectra, i.e., 100% occupancy). The majority of the trap states from the midgap to roughly 0.25 eV above the HOMO level are occupied, i.e., neutralized, meaning that they are no longer affecting the response of the OFET to applied bias. When looking at the shallower trap states (energy below 0.25 eV), the occupation increases with increasing C, especially close to the HOMO level.

https://doi.org/10.1021/acs.chemmater.3c01792
Chem. Mater. 2023, 35, 8645−8653

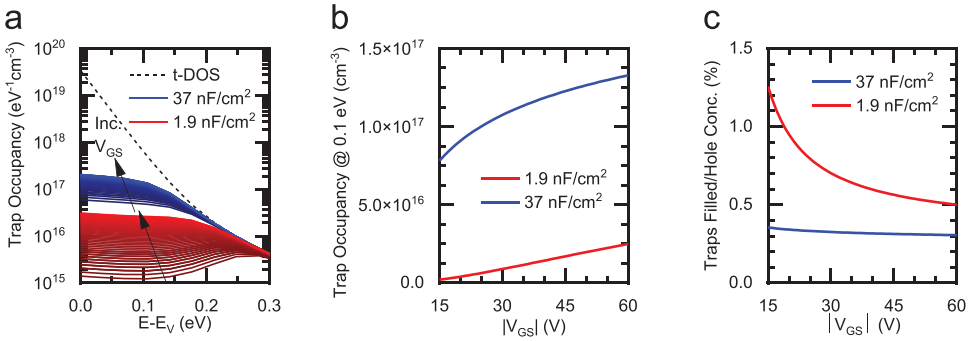


Figure 6. (a) Trap occupancy of the t-DOS spectra for C_{high} = 37 nF/cm^2 (blue) and C_{low} = 1.9 nF/cm^2 (red). V_{GS} = 0 to 60 V. (b) Trap occupation at E = 0.1 eV, plotted vs V_{GS}. (c) Trap occupation, integrated over energy and normalized to the hole concentration, plotted as a function of V_{GS}.

The number of occupied states plotted as a fraction of the total number of trap states shows that there is an order of magnitude difference in the trap occupancy upon going from C = 1.4 to 370 nF/cm^2 (Figure 5b, black). This means that the charge carriers in the low-C devices "see" a much larger number of unoccupied traps. As a result, the drain current normalized for capacitance (I_D/C) is reduced in the low-C devices compared to high-C (Figure 5b, blue). This hypothesis is supported by the results in Figure 5c, which shows that the total fraction of charge carriers that are trapped is smaller in high-C devices, indicating that there is a greater percentage of free vs trapped charges, which leads to the improved charge transport efficiency and, by extension, better device mobility.

Because mobility is a rate-of-change parameter, proportional to the change in drain current with respect to applied bias, we also examined the filling of t-DOS as a function of V_{GS}. We choose two representative values of C, with C_{high} = 37 nF/cm^2 and C_{low} = 1.9 nF/cm^2, and compared the trap occupation during a sweep of V_{GS} (Figure 6a). Figure 6b shows a vertical slice of Figure 6a, the trap occupancy at 0.1 eV, as a function of V_{GS}: in the C_{high} device, more trap states are filled at each bias step. Even so, the fraction of trapped charge carriers is lower (more favorable) in the C_{high} device (Figure 6c), which contributes to greater device mobility.

Raising the value of C has other benefits beyond the trap-neutralizing effects discussed above. Because drain current is proportional to both C and V_{GS}, increasing C implies a lower operating voltage range, which is critical for OFETs to be integrated into portable consumer electronics. Additionally, the switching speed of field-effect transistors is directly proportional to the value of C.[65] There are two basic means of increasing the capacitance of the dielectric layer: raising the dielectric constant or decreasing the layer thickness. High-k dielectrics have been investigated to reduce the operating voltages of OFETs; however, the mismatch of k at the semiconductor/dielectric interface may lead to Fröhlich polaron formation and dynamic disorder, which can counteract the desired effect.[66] It is also theorized that a high-k dielectric will increase the contact resistance in coplanar OFETs.[67] Decreasing the dielectric thickness avoids these issues, but it is limited by an increase in gate leakage, especially through pinholes, and even shorting can occur; even so progress has occurred, and single-layer dielectrics with capacitances in the 10 nF/cm^2 range have been demonstrated.[66]

A solution to the issues encountered with both high-k and thin dielectrics is to use a bilayer dielectric. The dielectric interfacing with the gate electrode can be high-k, thin and have a high breakdown voltage. Then, only a thin second dielectric layer is necessary to interface with the semiconductor, and it can be selected for the desired surface properties, such as surface roughness, hydrophobicity, trap density, and dielectric constant. For instance, oxides of hafnium or aluminum have been combined with a polymer dielectric to achieve values of C above 20 nF/cm^2.[68−71] Multiple layers of polymers have also achieved the same effect.[72] Exposing a polymer dielectric to plasma to form a thin oxide layer resulted in values of C = 160 nF/cm^2, with the dielectric layer only 15 nm thick.[73] Pushing the boundaries even further, a layer of oxide on Al or Ti was created through oxygen plasma exposure and then functionalized with densely packed self-assembled monolayers to form a dielectric thickness in the sub-10 nm range, with an incredible capacitance on the order of 1000 nF/cm^2 and minimal gate leakage.[74−76]

4. CONCLUSIONS

In summary, we investigated the impact of impurities and the trap density of states on organic field-effect transistor performance using a combined experimental/theoretical approach and detailed a device design route in OFETs with impurities to recover the performance to the level of a pure sample. TCAD simulations, wherein the programmed trap density was varied along with the dielectric capacitance, revealed that if the capacitance of the dielectric layer is sufficiently high, the detriments of the charge carrier traps are effectively neutralized. We attribute this phenomenon to the differences in the dynamics of trap-filling with respect to C: in OFETs based on low-C dielectrics, trap states are filled gradually with respect to applied bias. Each state that is filled (i.e., occupied) is neutralized and no longer contributes to device operation, but unoccupied traps can still be activated and scatter charges. Thus, with a low value of C, there is a greater density of unoccupied states in which active charge carriers become trapped, which decreases the drain current and device mobility. On the contrary, when C is high, the trap states fill rapidly, and so additional charges accumulated through applied bias will experience a lower density of unoccupied states; consequently, a smaller fraction of accumulated charges become trapped, and the trap spectrum has a weaker effect on device mobility. Our results promote a widely applicable strategy to address impurity-related performance losses with no alterations to the semiconductor layer. Nevertheless, we expect that the quantitative details will be dependent on the chemical nature of the impurity.

https://doi.org/10.1021/acs.chemmater.3c01792
Chem. Mater. 2023, 35, 8645−8653

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acs.chemmater.3c01792.

Histogram for grain size measurements, transistor transfer and output curves for transistors with different purity OSCs, and GIWAXS patterns for all film types (PDF)

■ AUTHOR INFORMATION

Corresponding Author

Oana D. Jurchescu − *Department of Physics and Center for Functional Materials, Wake Forest University, Winston−Salem, North Carolina 27106, United States;* orcid.org/0000-0003-2204-2909; Email: jurchescu@wfu.edu

Authors

Matthew Waldrip − *Department of Physics and Center for Functional Materials, Wake Forest University, Winston−Salem, North Carolina 27106, United States*

Yue Yu − *Department of Physics and Center for Functional Materials, Wake Forest University, Winston−Salem, North Carolina 27106, United States*

Rudolph Holley, III − *Department of Chemical and Biological Engineering, Princeton University, Princeton, New Jersey 08544, United States*

Yueh-Lin Loo − *Department of Chemical and Biological Engineering, Princeton University, Princeton, New Jersey 08544, United States;* orcid.org/0000-0002-4284-0847

John E. Anthony − *University of Kentucky Center for Applied Energy Research, Lexington, Kentucky 40511, United States;* orcid.org/0000-0002-8972-1888

Complete contact information is available at: https://pubs.acs.org/10.1021/acs.chemmater.3c01792

Author Contributions

The manuscript was written through contributions of all authors. All authors have given approval to the final version of the manuscript.

Notes

The authors declare no competing financial interest.

■ ACKNOWLEDGMENTS

The device effort was supported by the National Science Foundation (NSF), under grants ECCS-1810273 and DMR-1627925. OSCs were synthesized with support from the NSF (DMR-1627428). Structural characterizations were supported by the NSF Graduate Research Fellowship Program under Grant No. DGE-2039656. Computations were performed using the Wake Forest University (WFU) High Performance Computing Facility, a centrally managed computational resource available to WFU researchers including faculty, staff, students, and collaborators.

■ REFERENCES

(1) Someya, T.; Bao, Z.; Malliaras, G. G. The Rise of Plastic Bioelectronics. *Nature* **2016**, *540* (7633), 379−385.

(2) Jiang, H.; Hu, W. The Emergence of Organic Single-Crystal Electronics. *Angew. Chem., Int. Ed.* **2020**, *59* (4), 1408−1428.

(3) Arias, A. C.; MacKenzie, J. D.; McCulloch, I.; Rivnay, J.; Salleo, A. Materials and Applications for Large Area Electronics: Solution-Based Approaches. *Chem. Rev.* **2010**, *110* (1), 3−24.

(4) Dong, H.; Fu, X.; Liu, J.; Wang, Z.; Hu, W. 25th Anniversary Article: Key Points for High-Mobility Organic Field-Effect Transistors. *Adv. Mater.* **2013**, *25* (43), 6158−6183.

(5) Zhang, X.; Dong, H.; Hu, W. Organic Semiconductor Single Crystals for Electronics and Photonics. *Adv. Mater.* **2018**, *30* (44), 1801048.

(6) Bronstein, H.; Nielsen, C. B.; Schroeder, B. C.; McCulloch, I. The Role of Chemical Design in the Performance of Organic Semiconductors. *Nat. Rev. Chem* **2020**, *4* (2), 66−77.

(7) He, T.; Stolte, M.; Wang, Y.; Renner, R.; Ruden, P. P.; Würthner, F.; Frisbie, C. D. Site-Specific Chemical Doping Reveals Electron Atmospheres at the Surfaces of Organic Semiconductor Crystals. *Nat. Mater.* **2021**, *20* (11), 1532−1538.

(8) Tietze, M. L.; Benduhn, J.; Pahner, P.; Nell, B.; Schwarze, M.; Kleemann, H.; Krammer, M.; Zojer, K.; Vandewal, K.; Leo, K. Elementary Steps in Electrical Doping of Organic Semiconductors. *Nat. Commun.* **2018**, *9* (1), 1182.

(9) Tietze, M. L.; Pahner, P.; Schmidt, K.; Leo, K.; Lüssem, B. Doped Organic Semiconductors: Trap-Filling, Impurity Saturation, and Reserve Regimes. *Adv. Funct. Mater.* **2015**, *25* (18), 2701−2707.

(10) Kiefer, D.; Kroon, R.; Hofmann, A. I.; Sun, H.; Liu, X.; Giovannitti, A.; Stegerer, D.; Cano, A.; Hynynen, J.; Yu, L.; Zhang, Y.; Nai, D.; Harrelson, T. F.; Sommer, M.; Moulé, A. J.; Kemerink, M.; Marder, S. R.; McCulloch, I.; Fahlman, M.; Fabiano, S.; Müller, C. Double Doping of Conjugated Polymers with Monomer Molecular Dopants. *Nat. Mater.* **2019**, *18* (2), 149−155.

(11) Haneef, H. F.; Zeidell, A. M.; Jurchescu, O. D. Charge Carrier Traps in Organic Semiconductors: A Review on the Underlying Physics and Impact on Electronic Devices. *J. Mater. Chem. C* **2020**, *8* (3), 759−787.

(12) Hu, P.; He, X.; Jiang, H. Greater than 10 Cm2 V-1 S-1: A Breakthrough of Organic Semiconductors for Field-Effect Transistors. *InfoMat* **2021**, 3 (6), 613−630.

(13) Diemer, P. J.; Lamport, Z. A.; Mei, Y.; Ward, J. W.; Goetz, K. P.; Li, W.; Payne, M. M.; Guthold, M.; Anthony, J. E.; Jurchescu, O. D. Quantitative Analysis of the Density of Trap States at the Semiconductor-Dielectric Interface in Organic Field-Effect Transistors. *Appl. Phys. Lett.* **2015**, *107* (10), 103303.

(14) Song, X.; Gasparini, N.; Nahid, M. M.; Chen, H.; Macphee, S. M.; Zhang, W.; Norman, V.; Zhu, C.; Bryant, D.; Ade, H.; McCulloch, I.; Baran, D. A Highly Crystalline Fused-Ring N-Type Small Molecule for Non-Fullerene Acceptor Based Organic Solar Cells and Field-Effect Transistors. *Adv. Funct. Mater.* **2018**, *28* (35), 1802895.

(15) Scholz, S.; Kondakov, D.; Lüssem, B.; Leo, K. Degradation Mechanisms and Reactions in Organic Light-Emitting Devices. *Chem. Rev.* **2015**, *115* (16), 8449−8503.

(16) Giovannitti, A.; Rashid, R. B.; Thiburce, Q.; Paulsen, B. D.; Cendra, C.; Thorley, K.; Moia, D.; Mefford, J. T.; Hanifi, D.; Weiyuan, D.; Moser, M.; Salleo, A.; Nelson, J.; McCulloch, I.; Rivnay, J. Energetic Control of Redox-Active Polymers toward Safe Organic Bioelectronic Materials. *Adv. Mater.* **2020**, *32* (16), 1908047.

(17) Liu, S.; Peng, C.; Cruz, A.; Chen, Y.; So, F. Degradation Study of Organic Light-Emitting Diodes with Solution-Processed Small Molecule Phosphorescent Emitting Layers. *J. Mater. Chem. C* **2016**, *4* (37), 8696−8703.

(18) Nikolka, M.; Nasrallah, I.; Rose, B.; Ravva, M. K.; Broch, K.; Sadhanala, A.; Harkin, D.; Charmet, J.; Hurhangee, M.; Brown, A.; Illig, S.; Too, P.; Jongman, J.; McCulloch, I.; Bredas, J.; Sirringhaus, H. High Operational and Environmental Stability of High-Mobility Conjugated Polymer Field-Effect Transistors through the Use of Molecular Additives. *Nat. Mater.* **2017**, *16* (3), 356−362.

(19) Zeidell, A. M.; Filston, D. S.; Waldrip, M.; Iqbal, H. F.; Chen, H.; McCulloch, I.; Jurchescu, O. D. Large-Area Uniform Polymer Transistor Arrays on Flexible Substrates: Towards High-Throughput Sensor Fabrication. *Adv. Mater. Technol.* **2020**, *5* (8), 2000390.

(20) Hunter, S.; Anthopoulos, T. D. Observation of Unusual, Highly Conductive Grain Boundaries in High-Mobility Phase Separated Organic Semiconducting Blend Films Probed by Lateral-Transport Conductive-AFM. *Adv. Mater.* **2013**, *25* (31), 4320−4326.

(21) Tietze, M. L.; Rose, B. D.; Schwarze, M.; Fischer, A.; Runge, S.; Blochwitz-Nimoth, J.; Lüssem, B.; Leo, K.; Brédas, J. L. Passivation of Molecular N-Doping: Exploring the Limits of Air Stability. *Adv. Funct. Mater.* **2016**, *26* (21), 3730−3737.
(22) Wu, X.; Jia, R.; Jie, J.; Zhang, M.; Pan, J.; Zhang, X.; Zhang, X. Air Effect on the Ideality of P-Type Organic Field-Effect Transistors: A Double-Edged Sword. *Adv. Funct. Mater.* **2019**, *29* (51), 1906653.
(23) Jurchescu, O. D.; Baas, J.; Palstra, T. T. M. Effect of Impurities on the Mobility of Single Crystal Pentacene. *Appl. Phys. Lett.* **2004**, *84* (16), 3061−3063.
(24) Iqbal, H. F.; Ai, Q.; Thorley, K. J.; Chen, H.; McCulloch, I.; Risko, C.; Anthony, J. E.; Jurchescu, O. D. Suppressing Bias Stress Degradation in High Performance Solution Processed Organic Transistors Operating in Air. *Nat. Commun.* **2021**, *12* (1), 2352.
(25) Ruan, X.; Cheng, S.; Deng, W.; Tan, Y.; Lu, Z.; Shi, J.; Zhang, X.; Jie, J. Insights into the Origins of Minority Carrier Traps in Solution-Processed Organic Semiconductors and Their Effects on Transistor Photostability. *Adv. Electron. Mater.* **2022**, *8*, 2200355.
(26) Yang, J. P.; Bussolotti, F.; Kera, S.; Ueno, N. Origin and Role of Gap States in Organic Semiconductor Studied by UPS: As the Nature of Organic Molecular Crystals. *J. Phys. D Appl. Phys.* **2017**, *50* (42), 423002.
(27) Podzorov, V. Organic Single Crystals: Addressing the Fundamentals of Organic Electronics. *MRS Bull.* **2013**, *38* (1), 15−24.
(28) Rubinger, C. P. L.; Haneef, H. F.; Hewitt, C.; Carroll, D.; Anthony, J. E.; Jurchescu, O. D. Influence of Solvent Additives on the Morphology and Electrical Properties of DiF-TES ADT Organic Field-Effect Transistors. *Org. Electron.* **2019**, *68* (December 2018), 205−211.
(29) Jo, G.; Cho, S. H.; Kim, H.; Yoon, H.; Han, S.; Chang, M. Impacts of Secondary Solvents on Morphology and Charge Transport of Conjugated Polymer Thin Films. *Org. Electron.* **2020**, *81* (February), 105688.
(30) Zhang, G.; Yang, H.; He, L.; Hu, L.; Lan, S.; Li, F.; Chen, H.; Guo, T. Importance of Domain Purity in Semi-Conducting Polymer/Insulating Polymer Blends Transistors. *J. Polym. Sci., Part B: Polym. Phys.* **2016**, *54* (17), 1760−1766.
(31) Chen, M. S.; Lee, O. P.; Niskala, J. R.; Yiu, A. T.; Tassone, C. J.; Schmidt, K.; Beaujuge, P. M.; Onishi, S. S.; Toney, M. F.; Zettl, A.; Fréchet, J. M. J. Enhanced Solid-State Order and Field-Effect Hole Mobility through Control of Nanoscale Polymer Aggregation. *J. Am. Chem. Soc.* **2013**, *135* (51), 19229−19236.
(32) Ghamari, P.; Niazi, M. R.; Perepichka, D. F. Controlling Structural and Energetic Disorder in High-Mobility Polymer Semiconductors via Doping with Nitroaromatics. *Chem. Mater.* **2021**, *33* (8), 2937−2947.
(33) Nikolka, M.; Schweicher, G.; Armitage, J.; Nasrallah, I.; Jellett, C.; Guo, Z.; Hurhangee, M.; Sadhanala, A.; McCulloch, I.; Nielsen, C. B.; Sirringhaus, H. Performance Improvements in Conjugated Polymer Devices by Removal of Water-Induced Traps. *Adv. Mater.* **2018**, *30* (36), 1801874.
(34) Nasrallah, I.; Ravva, M. K.; Broch, K.; Novak, J.; Armitage, J.; Schweicher, G.; Sadhanala, A.; Anthony, J. E.; Bredas, J.; Sirringhaus, H. A Novel Mitigation Mechanism for Photo-Induced Trapping in an Anthradithiophene Derivative Using Additives. *Adv. Electron. Mater.* **2020**, *6*, 2000250.
(35) Paterson, A. F.; Lin, Y.; Mottram, A. D.; Fei, Z.; Niazi, M. R.; Kirmani, A. R.; Amassian, A.; Solomeshch, O.; Tessler, N.; Heeney, M.; Anthopoulos, T. D. The Impact of Molecular P-Doping on Charge Transport in High-Mobility Small-Molecule/Polymer Blend Organic Transistors. *Adv. Electron. Mater.* **2018**, *4* (10), 1700464.
(36) Lüssem, B.; Keum, C.-M.; Kasemann, D.; Naab, B.; Bao, Z.; Leo, K. Doped Organic Transistors. *Chem. Rev.* **2016**, *116* (22), 13714−13751.
(37) Gwinner, M. C.; Di Pietro, R.; Vaynzof, Y.; Greenberg, K. J.; Ho, P. K. H.; Friend, R. H.; Sirringhaus, H. Doping of Organic Semiconductors Using Molybdenum Trioxide: A Quantitative Time-Dependent Electrical and Spectroscopic Study. *Adv. Funct. Mater.* **2011**, *21* (8), 1432−1441.
(38) Matsuzawa, K.; Uchida, K.; Nishiyama, A. A Unified Simulation of Schottky and Ohmic Contacts. *IEEE Trans. Electron Devices* **2000**, *47* (1), 103−108.
(39) Lamport, Z. A.; Haneef, H. F.; Anand, S.; Waldrip, M.; Jurchescu, O. D. Tutorial: Organic Field-Effect Transistors: Materials, Structure and Operation. *J. Appl. Phys.* **2018**, *124* (7), 071101.
(40) Subramanian, S.; Park, S. K.; Parkin, S. R.; Podzorov, V.; Jackson, T. N.; Anthony, J. E. Chromophore Fluorination Enhances Crystallization and Stability of Soluble Anthradithiophene Semiconductors. *J. Am. Chem. Soc.* **2008**, *130* (9), 2706−2707.
(41) Hailey, A. K.; Hiszpanski, A. M.; Smilgies, D.-M.; Loo, Y.-L. The Diffraction Pattern Calculator (DPC) Toolkit: A User-Friendly Approach to Unit-Cell Lattice Parameter Identification of Two-Dimensional Grazing-Incidence Wide-Angle X-Ray Scattering Data. *J. Appl. Crystallogr.* **2014**, *47* (6), 2090−2099.
(42) Waldrip, M.; Iqbal, H. F.; Wadsworth, A.; McCulloch, I.; Jurchescu, O. D. Organic Thin-Film Transistors with Flame-Annealed Contacts. *Flexible Printed Electron.* **2020**, *5* (1), 014015.
(43) Diemer, P. J.; Hayes, J.; Welchman, E.; Hallani, R.; Pookpanratana, S. J.; Hacker, C. A.; Richter, C. A.; Anthony, J. E.; Thonhauser, T.; Jurchescu, O. D. The Influence of Isomer Purity on Trap States and Performance of Organic Thin-Film Transistors. *Adv. Electron. Mater.* **2017**, *3* (1), 1600294.
(44) Häusermann, R.; Willa, K.; Blülle, B.; Morf, T.; Facchetti, A.; Chen, Z.; Lee, J.; Batlogg, B. Device Performance and Density of Trap States of Organic and Inorganic Field-Effect Transistors. *Org. Electron.* **2016**, *28*, 306−313.
(45) Tietze, M. L.; Burtone, L.; Riede, M.; Lüssem, B.; Leo, K. Fermi Level Shift and Doping Efficiency in P-Doped Small Molecule Organic Semiconductors: A Photoelectron Spectroscopy and Theoretical Study. *Phys. Rev. B: Condens. Matter Mater. Phys.* **2012**, *86* (3), 035320.
(46) Ramachandhran, B.; Huizing, H. G. A.; Coehoorn, R. Charge Transport in Metal/Semiconductor/Metal Devices Based on Organic Semiconductors with an Exponential Density of States. *Phys. Rev. B: Condens. Matter Mater. Phys.* **2006**, *73* (23), 233306.
(47) Paterson, A. F.; Singh, S.; Fallon, K. J.; Hodsden, T.; Han, Y.; Schroeder, B. C.; Bronstein, H.; Heeney, M.; McCulloch, I.; Anthopoulos, T. D. Recent Progress in High-Mobility Organic Transistors: A Reality Check. *Adv. Mater.* **2018**, *30* (36), 1801079.
(48) Sirringhaus, H. 25th Anniversary Article: Organic Field-Effect Transistors: The Path Beyond Amorphous Silicon. *Adv. Mater.* **2014**, *26* (9), 1319−1335.
(49) Lamport, Z. A.; Barth, K. J.; Lee, H.; Gann, E.; Engmann, S.; Chen, H.; Guthold, M.; McCulloch, I.; Anthony, J. E.; Richter, L. J.; DeLongchamp, D. M.; Jurchescu, O. D. A Simple and Robust Approach to Reducing Contact Resistance in Organic Transistors. *Nat. Commun.* **2018**, *9* (1), 5130.
(50) Lamport, Z. A.; Li, R.; Wang, C.; Mitchell, W.; Sparrowe, D.; Smilgies, D.-M.; Day, C.; Coropceanu, V.; Jurchescu, O. D. Organic Thin Films with Charge-Carrier Mobility Exceeding That of Single Crystals. *J. Mater. Chem. C* **2017**, *5* (39), 10313−10319.
(51) Jurchescu, O. D.; Subramanian, S.; Kline, R. J.; Hudson, S. D.; Anthony, J. E.; Jackson, T. N.; Gundlach, D. J. Organic Single-Crystal Field-Effect Transistors of a Soluble Anthradithiophene. *Chem. Mater.* **2008**, *20* (21), 6733−6737.
(52) Diemer, P. J.; Lyle, C. R.; Mei, Y.; Sutton, C.; Payne, M. M.; Anthony, J. E.; Coropceanu, V.; Brédas, J. L.; Jurchescu, O. D. Vibration-Assisted Crystallization Improves Organic/Dielectric Interface in Organic Thin-Film Transistors. *Adv. Mater.* **2013**, *25* (48), 6956−6962.
(53) Niazi, M. R.; Li, R.; Abdelsamie, M.; Zhao, K.; Anjum, D. H.; Payne, M. M.; Anthony, J.; Smilgies, D.-M.; Amassian, A. Contact-Induced Nucleation in High-Performance Bottom-Contact Organic Thin Film Transistors Manufactured by Large-Area Compatible Solution Processing. *Adv. Funct. Mater.* **2016**, *26* (14), 2371−2378.
(54) Fukuda, K.; Yoshimura, Y.; Okamoto, T.; Takeda, Y.; Kumaki, D.; Katayama, Y.; Tokito, S. Reverse-Offset Printing Optimized for

https://doi.org/10.1021/acs.chemmater.3c01792
Chem. Mater. 2023, 35, 8645−8653

Scalable Organic Thin-Film Transistors with Submicrometer Channel Lengths. *Adv. Electron. Mater.* **2015**, *1* (8), 1500145.
(55) Mei, Y.; Diemer, P. J.; Niazi, M. R.; Hallani, R. K.; Jarolimek, K.; Day, C. S.; Risko, C.; Anthony, J. E.; Amassian, A.; Jurchescu, O. D. Crossover from Band-like to Thermally Activated Charge Transport in Organic Transistors Due to Strain-Induced Traps. *Proc. Natl. Acad. Sci. U.S.A.* **2017**, *114* (33), E6739−E6748.
(56) Park, S. K.; Jackson, T. N.; Anthony, J. E.; Mourey, D. A. High Mobility Solution Processed 6,13-Bis(Triisopropyl-Silylethynyl) Pentacene Organic Thin Film Transistors. *Appl. Phys. Lett.* **2007**, *91* (6), 063514.
(57) Zhou, Z.; Zhang, Z.; Wu, Q.; Ji, X.; Wang, J.; Zeng, X.; Feng, S.-P.; Chan, P. K. L. Inch-Scale Grain Boundary Free Organic Crystals Developed by Nucleation Seed-Controlled Shearing Method. *ACS Appl. Mater. Interfaces* **2018**, *10* (41), 35395−35403.
(58) Waldrip, M.; Jurchescu, O. D.; Gundlach, D. J.; Bittle, E. G. Contact Resistance in Organic Field-Effect Transistors: Conquering the Barrier. *Adv. Funct. Mater.* **2020**, *30* (20), 1904576.
(59) Lee, S. S.; Kim, C. S.; Gomez, E. D.; Purushothaman, B.; Toney, M. F.; Wang, C.; Hexemer, A.; Anthony, J. E.; Loo, Y. L. Controlling Nucleation and Crystallization in Solution-Processed Organic Semiconductors for Thin-Film Transistors. *Adv. Mater.* **2009**, *21* (35), 3605−3609.
(60) Li, R.; Ward, J. W.; Smilgies, D. M.; Payne, M. M.; Anthony, J. E.; Jurchescu, O. D.; Amassian, A. Direct Structural Mapping of Organic Field-Effect Transistors Reveals Bottlenecks to Carrier Transport. *Adv. Mater.* **2012**, *24* (41), 5553−5558.
(61) Ward, J. W.; Loth, M. a.; Kline, R. J.; Coll, M.; Ocal, C.; Anthony, J. E.; Jurchescu, O. D. Tailored Interfaces for Self-Patterning Organic Thin-Film Transistors. *J. Mater. Chem.* **2012**, *22* (36), 19047.
(62) Jurchescu, O. D.; Hamadani, B. H.; Xiong, H. D.; Park, S. K.; Subramanian, S.; Zimmerman, N. M.; Anthony, J. E.; Jackson, T. N.; Gundlach, D. J. Correlation between Microstructure, Electronic Properties and Flicker Noise in Organic Thin Film Transistors. *Appl. Phys. Lett.* **2008**, *92* (13), 132103.
(63) Choi, H. H.; Cho, K.; Frisbie, C. D.; Sirringhaus, H.; Podzorov, V. Critical Assessment of Charge Mobility Extraction in FETs. *Nat. Mater.* **2018**, *17* (1), 2−7.
(64) Iqbal, H. F.; Holland, E. K.; Anthony, J. E.; Jurchescu, O. D. Real-Time Monitoring of Trap Dynamics Reveals the Electronic States That Limit Charge Transport in Crystalline Organic Semiconductors. *Mater. Horiz.* **2020**, *7* (9), 2390−2398.
(65) Klauk, H. Will We See Gigahertz Organic Transistors? *Adv. Electron. Mater.* **2018**, *4* (10), 1700474.
(66) Nketia-Yawson, B.; Noh, Y. Y. Recent Progress on High-Capacitance Polymer Gate Dielectrics for Flexible Low-Voltage Transistors. *Adv. Funct. Mater.* **2018**, *28* (42), 1802201.
(67) Zojer, K.; Zojer, E.; Fernandez, A. F.; Gruber, M. Impact of the Capacitance of the Dielectric on the Contact Resistance of Organic Thin-Film Transistors. *Phys. Rev. Appl.* **2015**, *4* (4), 044002.
(68) Raghuwanshi, V.; Bharti, D.; Tiwari, S. P. Flexible Organic Field-Effect Transistors with TIPS-Pentacene Crystals Exhibiting High Electrical Stability upon Bending. *Org. Electron.* **2016**, *31*, 177−182.
(69) Kim, G.; Fuentes-Hernandez, C.; Jia, X.; Kippelen, B. Organic Thin-Film Transistors with a Bottom Bilayer Gate Dielectric Having a Low Operating Voltage and High Operational Stability. *ACS Appl. Electron. Mater.* **2020**, *2* (9), 2813−2818.
(70) Hwang, D. K.; Fuentes-Hernandez, C.; Kim, J.; Potscavage, W. J.; Kim, S. J.; Kippelen, B. Top-Gate Organic Field-Effect Transistors with High Environmental and Operational Stability. *Adv. Mater.* **2011**, *23* (10), 1293−1298.
(71) Jia, X.; Fuentes-Hernandez, C.; Wang, C.-Y.; Park, Y.; Kippelen, B. Stable Organic Thin-Film Transistors. *Sci. Adv.* **2018**, *4* (1), No. eaao1705.
(72) Stucchi, E.; Dell'Erba, G.; Colpani, P.; Kim, Y. H.; Caironi, M. Low-Voltage, Printed, All-Polymer Integrated Circuits Employing a Low-Leakage and High-Yield Polymer Dielectric. *Adv. Electron. Mater.* **2018**, *4* (12), 1800340.
(73) Seong, H.; Baek, J.; Pak, K.; Im, S. G. A Surface Tailoring Method of Ultrathin Polymer Gate Dielectrics for Organic Transistors: Improved Device Performance and the Thermal Stability Thereof. *Adv. Funct. Mater.* **2015**, *25* (28), 4462−4469.
(74) Borchert, J. W.; Peng, B.; Letzkus, F.; Burghartz, J. N.; Chan, P. K. L.; Zojer, K.; Ludwigs, S.; Klauk, H. Small Contact Resistance and High-Frequency Operation of Flexible Low-Voltage Inverted Coplanar Organic Transistors. *Nat. Commun.* **2019**, *10* (1), 1119.
(75) Borchert, J. W.; Zschieschang, U.; Letzkus, F.; Giorgio, M.; Weitz, R. T.; Caironi, M.; Burghartz, J. N.; Ludwigs, S.; Klauk, H. Flexible Low-Voltage High-Frequency Organic Thin-Film Transistors. *Sci. Adv.* **2020**, *6* (21), No. eaaz5156.
(76) Geiger, M.; Lingstädt, R.; Wollandt, T.; Deuschle, J.; Zschieschang, U.; Letzkus, F.; Burghartz, J. N.; van Aken, P. A.; Weitz, R. T.; Klauk, H. Subthreshold Swing of 59 MV Decade-1 in Nanoscale Flexible Ultralow-Voltage Organic Transistors. *Adv. Electron. Mater.* **2022**, *8*, 2101215.

https://doi.org/10.1021/acs.chemmater.3c01792
Chem. Mater. 2023, 35, 8645−8653