

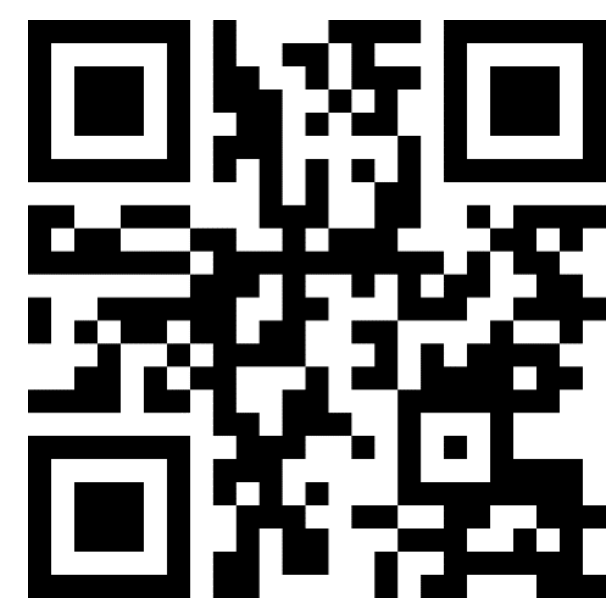
A Heterogeneous SoC for Bluetooth LE in 28nm

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University of California, Berkeley

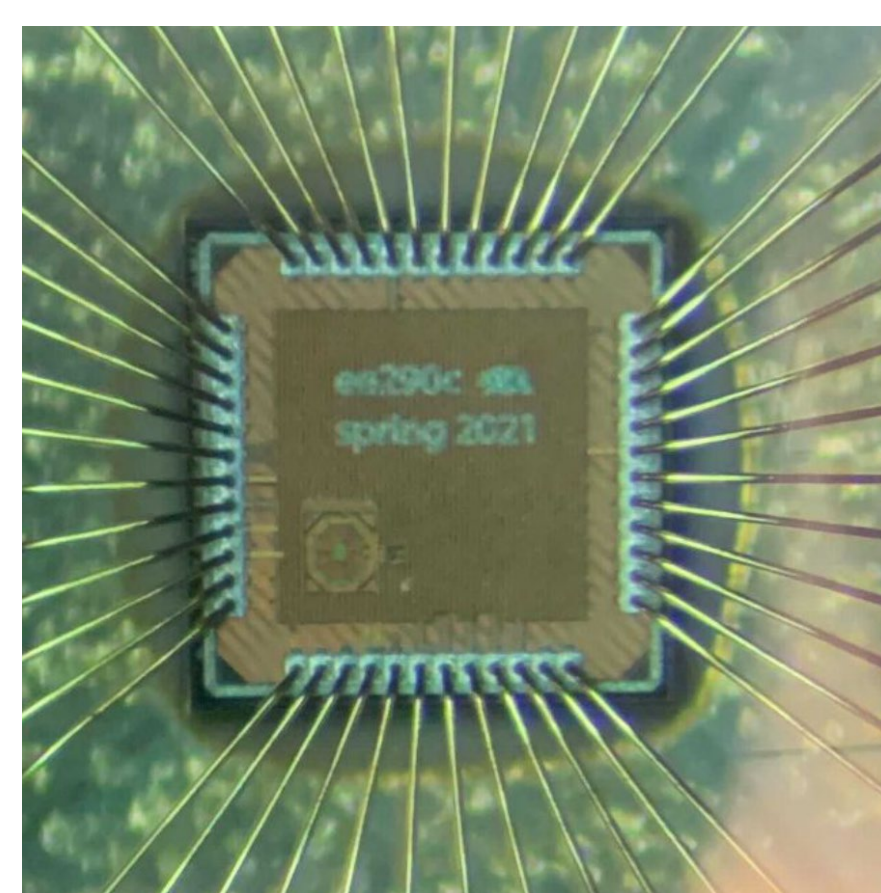
Motivation

- Create a system-on-chip (SoC) (dubbed OsciBear) featuring:
 - RISC-V 32-bit 5-stage in-order scalar processor
 - AES accelerator
 - BLE 1M baseband-modem
 - 2.4 GHz radio front end (RFE) transceiver
 - On chip power regulation and distribution
- Tape out in 14 weeks with 19 students (4 Ph.D students, 6 masters students, and 8 undergraduates)
- Demonstrate Berkeley-developed agile hardware tools and flow
- More about UC Berkeley's tapeout course can be found at <https://ucb-ee290c.github.io> and here:

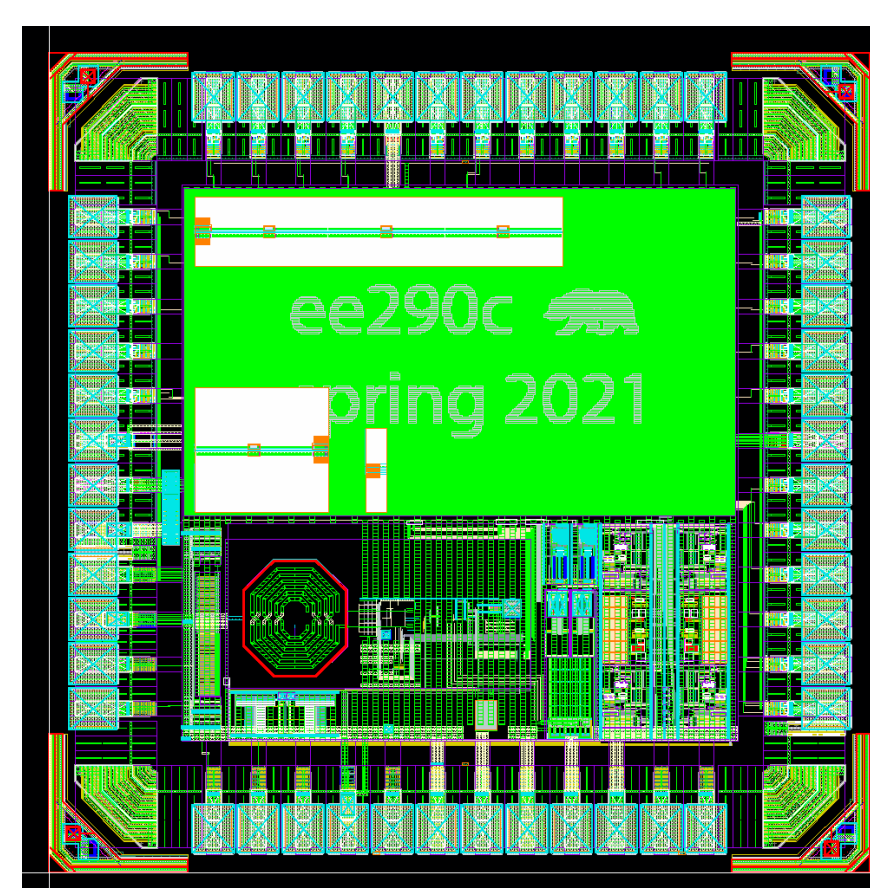


Verification

Chip Photos



Wirebonded Die

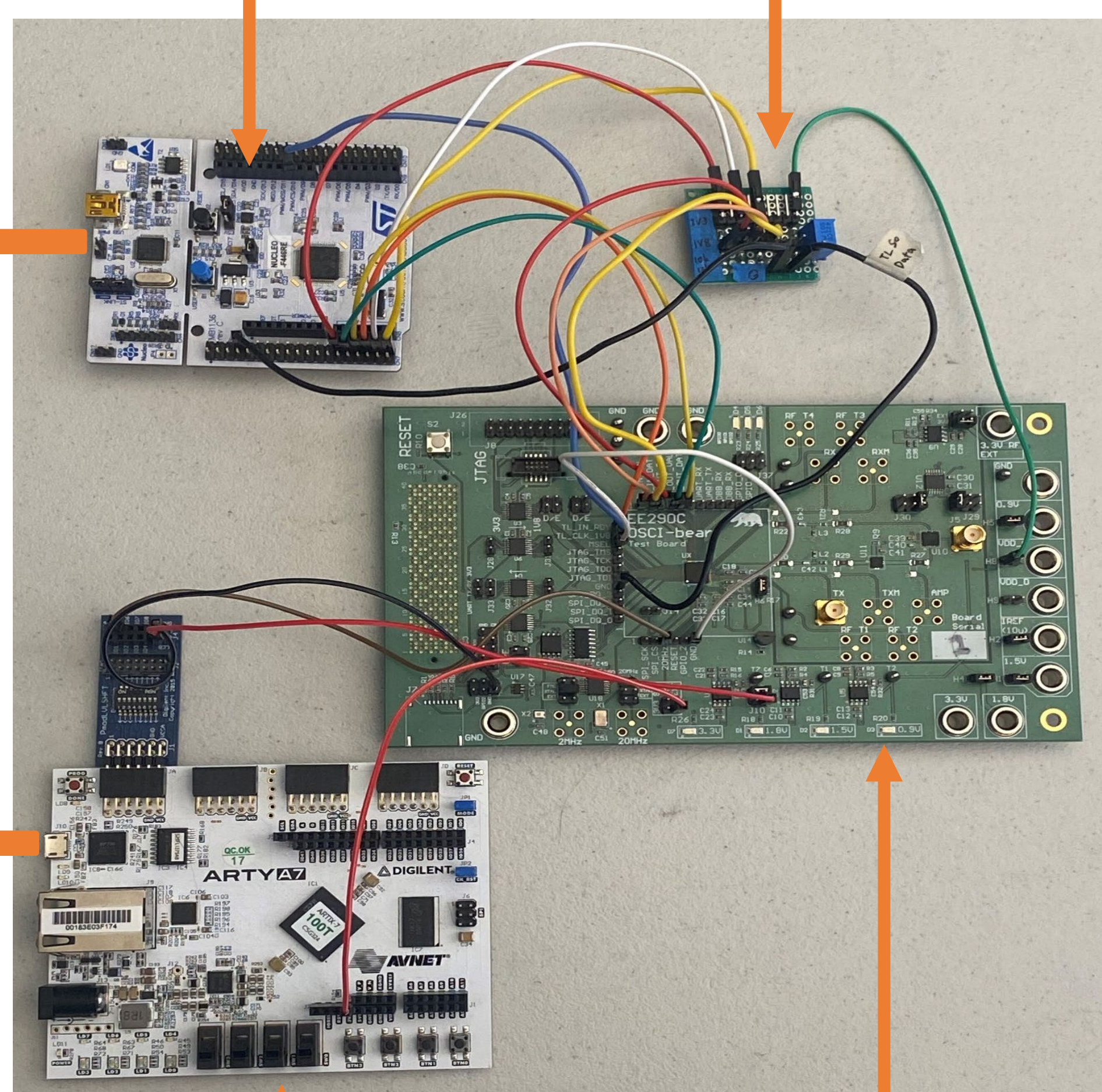


Chip Layout

Demonstration Setup

STM32 microcontroller programming chip through TileLink interface

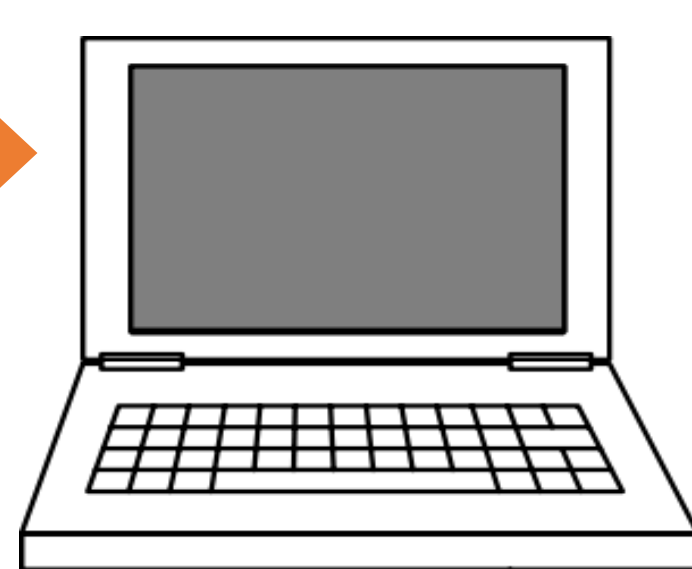
Radio tuning & level shifter board



Arty A7 providing CPU clock and power

Student designed PCB

USB connection to laptop



Chip Specs

- Digital Components
 - Compute
 - RV32IMAF Core
 - Interrupt Controller
 - UART and TSI peripherals
 - Digital Baseband
 - TX/RX packet control
 - Digital RF tuning constants
- Analog Components
 - Radio Front End
 - Low-IF receiver architecture
 - TX and LO generation through VCO
 - Digital GFSK modulation tuning interface
 - Power Regulation
 - Three domains – analog, digital, and I/O
- <10mW of static power
- 74% density on digital portion of chip

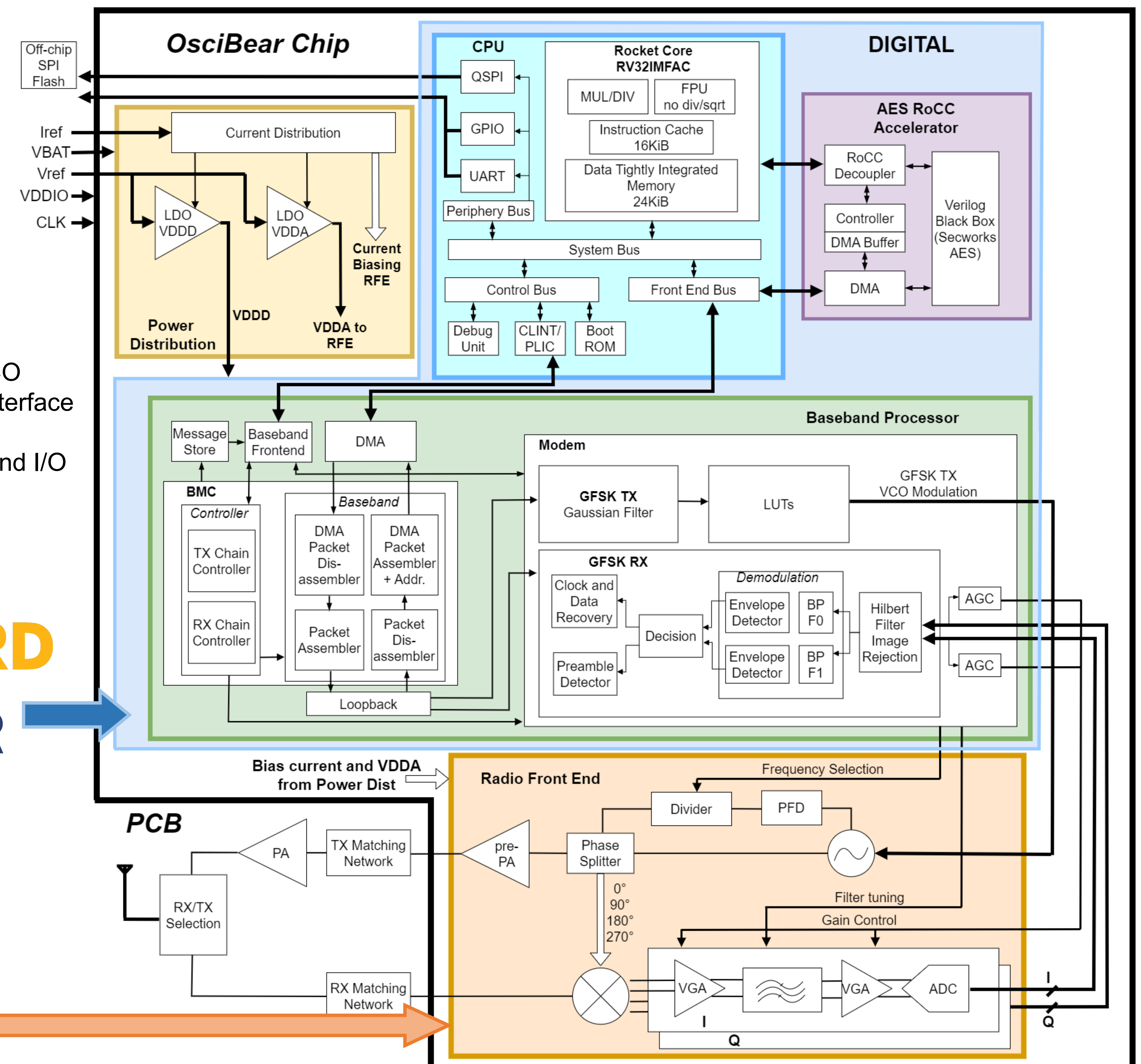
Research Infrastructure



Analog

BAG
Berkeley Analog
Generator
(ADC Only)

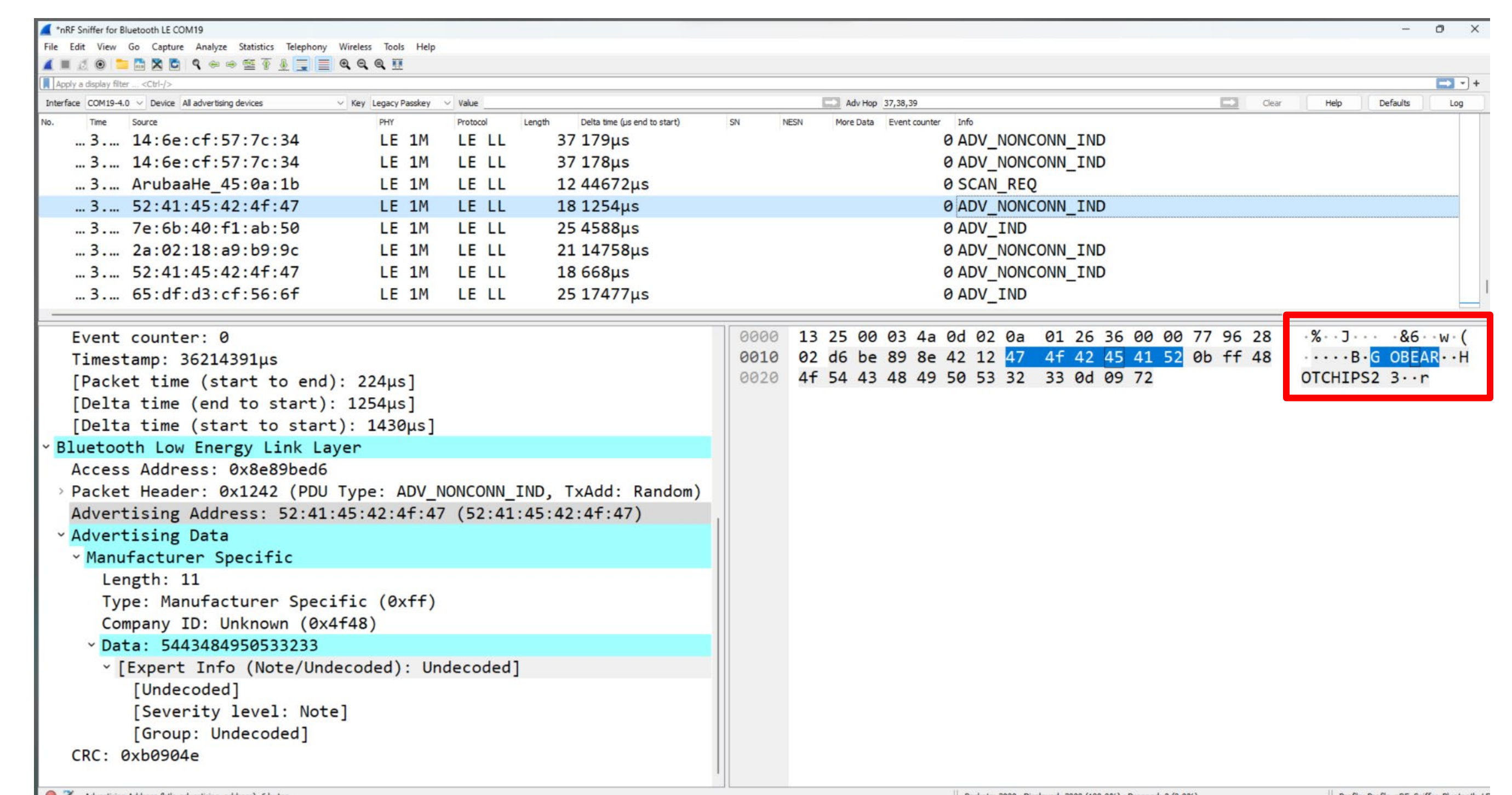
Chip Architecture



Bluetooth LE Transmit and Receive Measurements

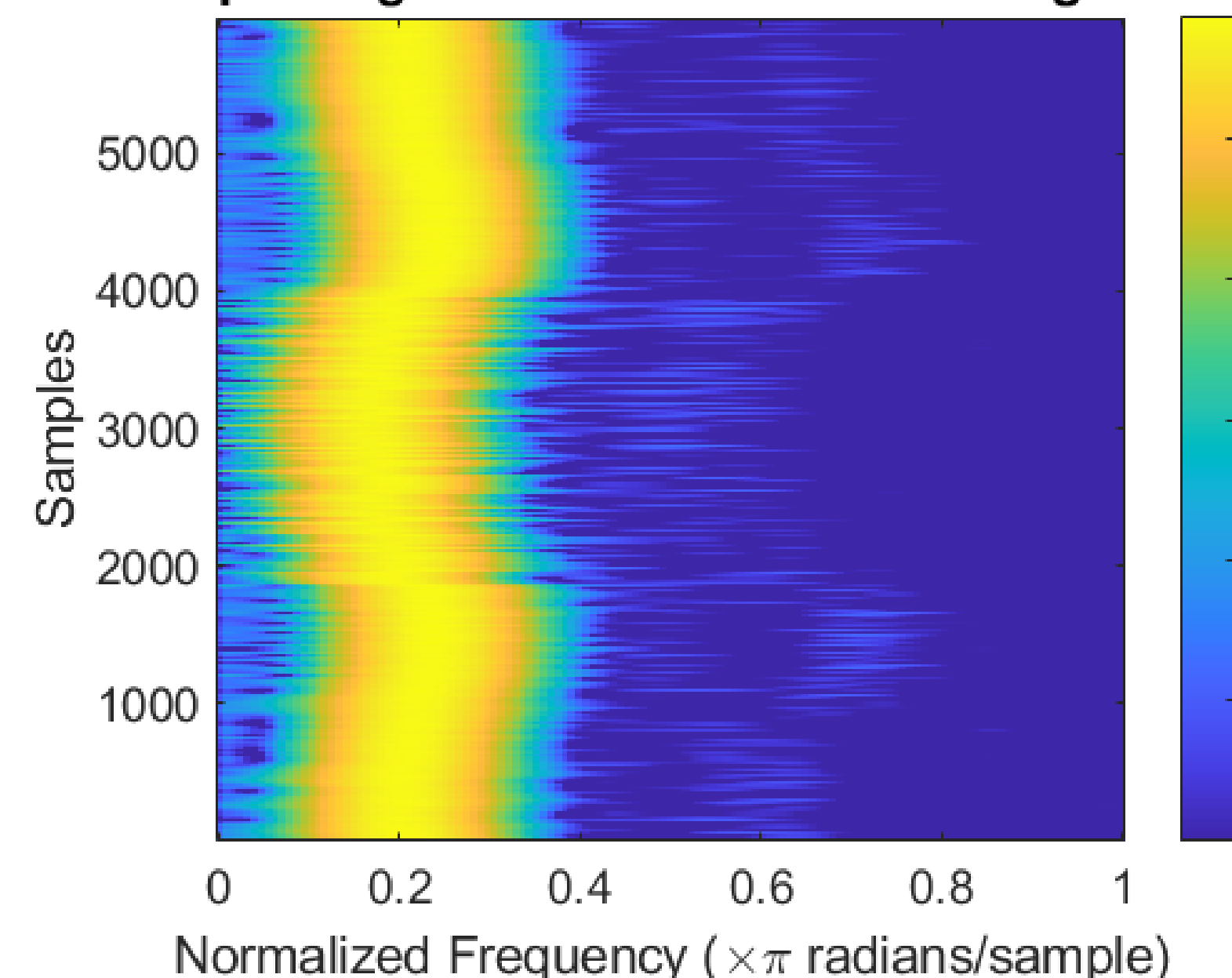
- Transmit packet decoding done two ways:
 - Software Testing
 - Transmitted RF signal mixed down off chip
 - IF signal demodulated in software showed preamble, access address, and payload
 - Commercial (Nordic nRF52DK) receiver
 - LO calibrated to BLE channel 38 (advertisement)
 - Packet transmitted periodically with commercial receiver configured as sniffer
- Receiver tested from PCB antenna port to differential output of final VGA (pre-ADC)

Radio Measurement Summary	
TX Frequency Modulation Range	~250 kHz
TX Power 1 meter away	-55 dBm
RX Chain SNDR (pre-ADC)	24.87 dB

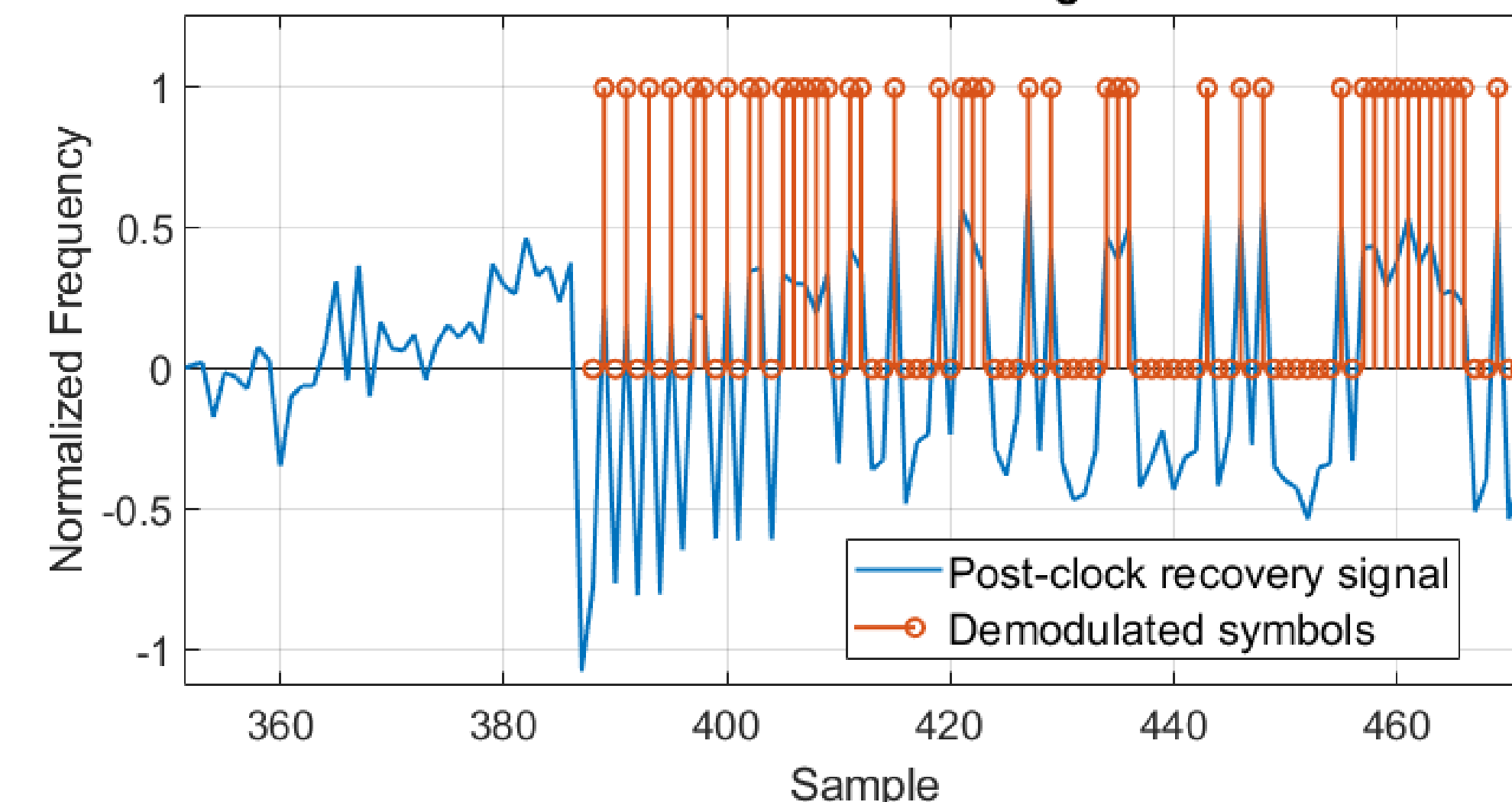


Commercial receiver decoding correctly formed packet sent with "GOBEAR HOTCHIPS23" as payload

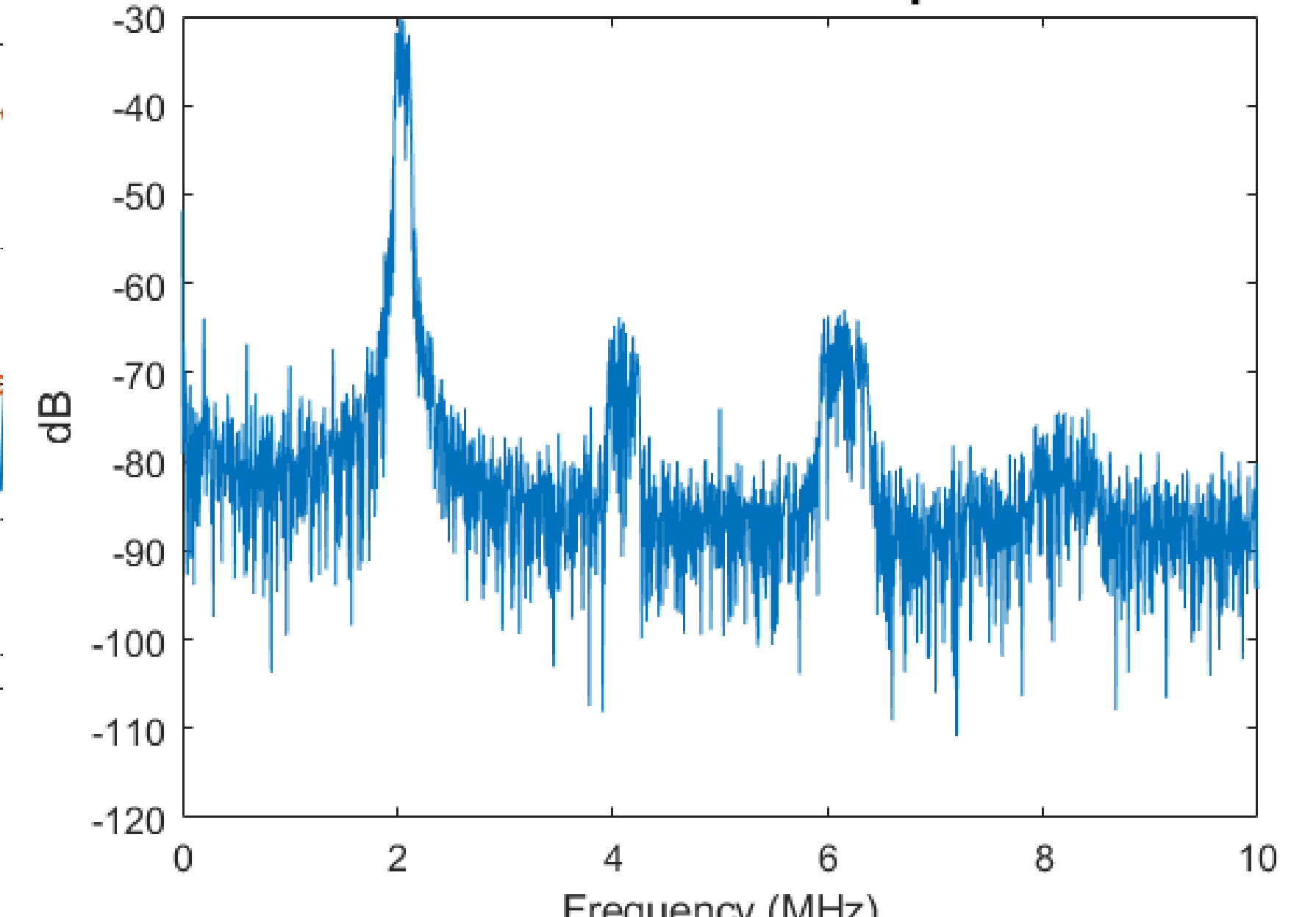
Spectrogram of GFSK Modulated Signal



Demodulated GFSK Signal



Full Receiver Chain Output FFT



Acknowledgements

We would like to acknowledge and thank Apple for supporting integrated circuit engineering classes at UC Berkeley EECS department through Apple's New Silicon Initiative program. This work is also funded by NSF CCRI ENS Chipyard Award #2016662