A Batteryless Power Management Unit for RF Energy Harvesting Sensors

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***Abstract*—We propose a RF energy harvesting system implemented in the 180nm CMOS technology that operates at 915 MHz ISM band. A system is designed to optimize the overall power conversion efficiency (PCE) within the input power range from -30 dBm to 0 dBm. The elements of the tunable matching network are selected based on the derived rectifier model. The dual-channel rectifier, including two Dickson rectifiers, is designed to achieve 64% power conversion efficiency (PCE) across the input power range. A power management unit (PMU), optimized for the operation modes of RF sensors, enables system to achieves 92% efficiency at -13 dBm. The end-to-end RF energy harvester (RFEH) PCE reaches 25.09% at the same input power.**

***Index Terms*—Batteryless, power management unit, dual-channel, Dickson rectifier, power conversion efficiency.**

I. Introduction

Over recent decades, the advancement of the Internet of Things (IoT) has significantly influenced our contemporary lifestyle through innovations such as smart cities, health care devices, electric vehicles, and more. In the RF energy harvesting field, it is required to have a PMU to store the energy collected from the environment into a super-capacitor or a rechargeable battery. However, the bulky size and the chemical content are not feasible to be applied in some implant medical devices. Further, the pervasive RF energy emitted by the communication infrastructure such as TV towers and WiFi sources offers a path to get over the problem of the battery lifetime with backscattering Tag-to-Tag Networks (BTTNs) [1]. In BTTNs, the power level under consideration for the source ranges from -30 dBm to 0 dBm [2].

A PMU, as the bridge between the rectifier and the application circuitry, usually includes a DC-DC converter and its control logic circuits to optimize the energy from the rectifier output to the storage element and the low drop-out linear voltage regulator (LDO), which generates the supply voltage for the application [3]–[5]. However, the control circuit of DC-DC increases the design complexity of the PMU. The share of power consumed by it becomes non-negligible when the overall available power is extremely small. In [6], a reconfigurable RF energy harvesting system aims to fulfill the current requirements of external DC loads while also storing surplus energy in external capacitors to enhance the efficiency of the available output power. Moreover, an novel adaptive capacitor charger (ACC) is proposed to fix the rectifier output voltage and charge the storage capacitor by the introduced extra current in [7]. Furthermore, [8] proposes a RF energy harvesting system which can achieve self-regulated function by a conceive negative feedback design.

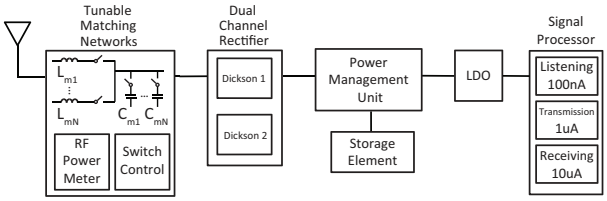


Fig. 1. Block diagram of the RF energy harvesting circuit in the sensory system-on-chip design.

The organization of this paper is as follows. Section II focuses on the implementation of the power management unit and its operation modes. Further, Section III presents the simulation results of the matching networks, rectifier and the power management unit. Finally, Section IV gives the summary and conclusion.

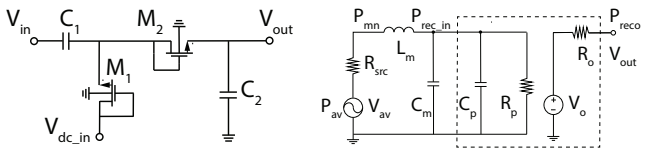
II. Proposed Power Management Unit

In Fig. 1, it depicts the diagram of the RF energy harvesting circuit in the sensory system-on-chip design. After the antenna, a tunable matching network, compromising parallel inductor and capacitors, is installed. The switches are controlled based on the source available power levels. A dual-channel Dickson rectifier with diode connected native NMOS transistors is designed to achieve the maximum PCE in the input power range below and above -18 dBm. A zener diode will be place at the output of the rectifier to limit the voltage at 1.5V when having excessive input power. The PMU is positioned between the rectifier and the load to optimize power transmission efficiency and set its output voltage in the range of 1∼1.2V. In order to minimize the leakage, a Panasonic ECQUL metalized polyester film capacitor is used as the storage element [9]. Additionally, an ultra-low power low dropout voltage regulator (LDO) is employed to facilitate the operation of the signal processor during listening, transmission, and receiving modes [10].

A. Rectifiers and Matching Networks

The proposed rectifier utilizes the Dickson's structure which is depicted in Fig. 2(a). Two diode connected native NMOS transistors are applied to block the reverse leakage current and

allow the usage of the low input power for their negligible threshold voltage [11]. The L-matching network, named for the configuration of its components, is widely recognized as one of the most commonly used and straightforward matching network designs [12].



(a) (b)

Fig. 2. (a) 1-stage Dickson rectifier with diode-connected native NMOS and (b) L-matching networks with the rectifier model.

From the voltage and power sensed at the input of rectifier, the rectifier can be modeled as a parallel resistor R_p and capacitor C_p, which can be expressed as below,

$$R_p = \frac{V_{rms}^2}{P_{reci}} \tag{1}$$

$$C_p = \frac{1}{\omega R_p}\sqrt{\left(\frac{I_{rms}R_p}{V_{rms}}\right)^2 - 1} \tag{2}$$

where P_{reci}, I_{rms} and V_{rms} are the input power, the RMS input current and voltage of the rectifier.

The inductance L_m and capacitance C_m of the L matching network are expressed as follows [13],

$$L_m = \frac{QR_{src}}{\omega} \tag{3}$$

$$C_m = \frac{Q}{\omega R_p} - C_p \tag{4}$$

$$Q = \sqrt{\left(\frac{R_p}{R_{src}}\right) - 1} \tag{5}$$

where Q is the quality factor.

B. Implementation of the Proposed PMU

The implementations of the PMU and control logic are illustrated in Fig. 3 and Fig. 4, respectively. All switches are designed by PMOS transistors. $R_1 \sim R_4$ are the feedback resistors. The input voltage of the PMU V_{pmui} is clamped at $2V_{ref1}$ by the closed loop formed by the operational amplifier(OpAmp) A and feedback resistors R_1 and R_2. The V_{pmui} is expressed as the equation below,

$$V_{pmui} = \frac{V_{ref1}}{\beta} = \frac{R_1 + R_2}{R_2}V_{ref1} \tag{6}$$

where $R_1 = R_2$. In other words, it becomes simple to obtain the maximum PCE of the dual-channel rectifier under the fixed voltage condition.

When charging the storage capacitor C_{store}, the switch S_1 is acting like a current source. The current injected into the C_{store} is adjusted by the output of the OpAmp A, so as to clamp the V_{pmui}. Once the charged voltage V_{chrg} is accumulated over the ready signal V_{rdy}, the S_1 is fully turned on. S_2 is cut off to avoid the V_{chrg} going high with excessive

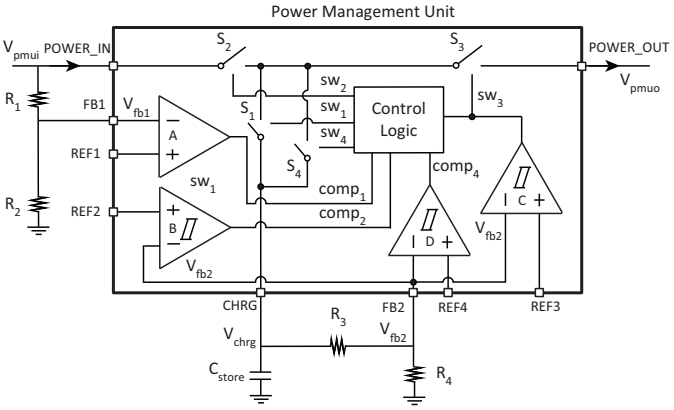


Fig. 3. Implementation of the power management unit.

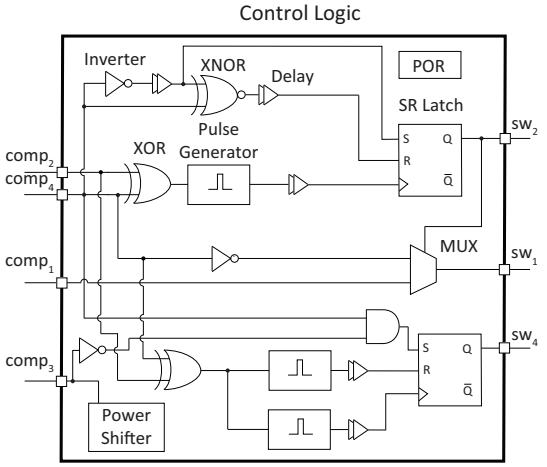


Fig. 4. Control logic implementation.

power. S_3, behaving as the under voltage lockout(UVLO) is turn on when V_{chrg} is larger than V_{shd}. S_4 is either turned on at the beginning of low power harvesting or discharging.

TABLE I
TURNED-ON PATHS OF THE PMU IN THE DEFINED VOLTAGE REGIONS

Vpmui / Vpmui	Vpmui<Vstart	Vstart<Vpmui<Vrdy		Vpmui>Vrdy	
Vchrg<Vshd	Open	IN2C		IN2C	
Vshd<Vchrg<Vrdy	Open	IN2C,L		IN2C,L	
Vrdy<Vchrg<Vovc	C2L	IN2C,L	C2L	IN2C,L	C2L
Vchrg>Vovc	C2L	IN2C,L	C2L	IN2C,L	C2L

IN2C: power is from PMU input to the C_{store}; IN2C,L: power is from PMU input to the C_{store} and LDO; C2L: power is from the C_{store} to the LDO.

Further, the proposed control circuit uses a SR latch to prevent the V_{pmuo} from increasing without limitation after charging up. Otherwise, it will result in the low efficiency of the LDO and damage to the circuit. The MUX makes sure the S_1 fully turned off during the discharging.

In TABLE I, it presents the turned-on paths of the PMU in the defined voltage regions. The relation of the reference voltages is defined as $V_{start}<V_{shd}<V_{rdy}<V_{ovc}$. The blue,

green, red and yellow colors represents the low power harvesting mode, regular mode, overcharge mode and stored energy supply mode of the PMU, which will be explained in the next subsection. Since the power to charging the C_{store} is related to the V_{chrg}, the PCE of the PMU is modified with the stored energy and the charging time t_c as follows,

$$PCE_{pmu} = \frac{P_{pmuo}t_c + \frac{1}{2}C_{store}V_{chrg}^2}{P_{pmui}t_c} \quad (7)$$

where P_{pmui} and P_{pmuo} are the input and output power of the PMU.

C. Operating Modes

Fig. 5 describes the five operation modes of the PMU, including standby mode, low power harvesting mode, regular mode, overcharge mode and shutdown mode. V_{start} is the threshold of the S_1. V_{shd}, V_{rdy} and V_{ovc} equal to $2V_{ref3}$, $2V_{ref4}$) and $2V_{ref2}$ respectively.

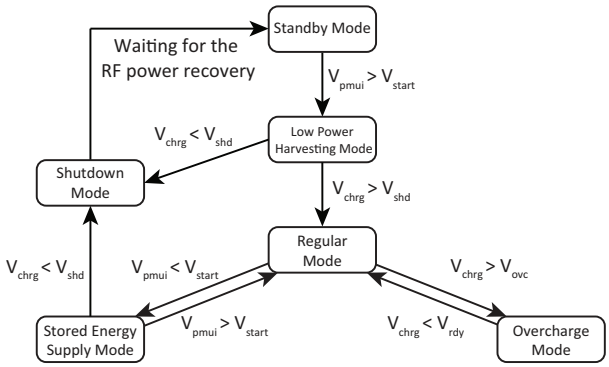


Fig. 5. Functional mode diagram of the power management unit.

In the standby mode, the PMU is waiting for the power coming into the system. Once the input power of the rectifier P_{rec_in} becomes enough to output a voltage, which is close to the PMOS switch threshold voltage $V_{th,p}$. Since $|V_{gs}|>|V_{th,p}|$, the switch can be turned on to charge the C_{store}. In the low power harvesting mode, S_1 and S_2 are turned on at the same time for fast charging. Meanwhile, the V_{chrg} increase as the energy being collected. Once V_{chrg} surpasses the shutdown voltage V_{shd}, the PMU shifts to the regular modes. At the time,only S_1 is supplying the input of the LDO and streaming the sufficient current into the C_{store}. V_{pmui} is clamped at $2V_{ref1}$. When the V_{chrg} reaches the overcharge voltage V_{ovc}, the PMU enters the overcharge mode. It will intermittently disconnect from the V_{pmui} to prevent excessive input energy. Therefore, the LDO is protected from the high input voltage and consuming the stored the energy on the C_{store}. Once the V_{chrg} declines to the V_{rdy}, the PMU returns to the regular mode.

Further, when the RF source does not provide enough energy or is cut off, the PMU enters the stored energy supply mode. The LDO consumes the stored energy on C_{store} until the V_{chrg} drops below the shundown voltage V_{shd}. If the RF power is resumed in time, it jumps back to the regular mode.

If the condition that $V_{pmui}<V_{start}$ and $V_{chrg}<V_{shd}$ are both satisfied, the shutdown mode is triggered by the PMU. In this mode, switches are turned off to prevent the excessive discharge. The PMU returns back to the standby mode.

III. Simulation Results

The RF energy harvesting system is designed in 180nm CMOS technology and simulated in Cadence simulation environment. A 915 MHz RF source is applied. In order to design the L matching networks, the R_p and C_p values are determined across the aimed source power range with the required loads in Fig. 6. The dual-channel Dickson rectifier is designed to transfer maximum PCE for the input power range from -30 to 0 dBm. Therefore, two 1-stage Dickson rectifiers are applied to fit in the input power below and above -18 dBm.

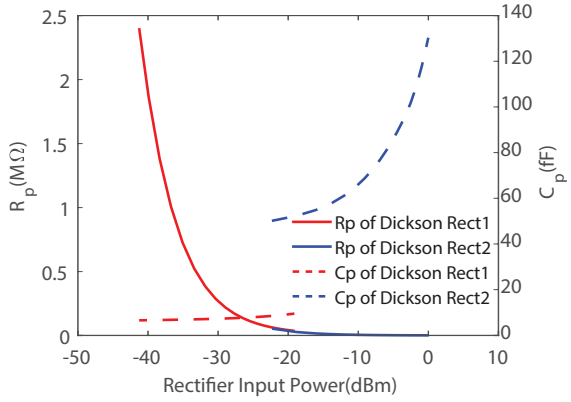


Fig. 6. Rectifier input resistance and capacitance vs. rectifier input power.

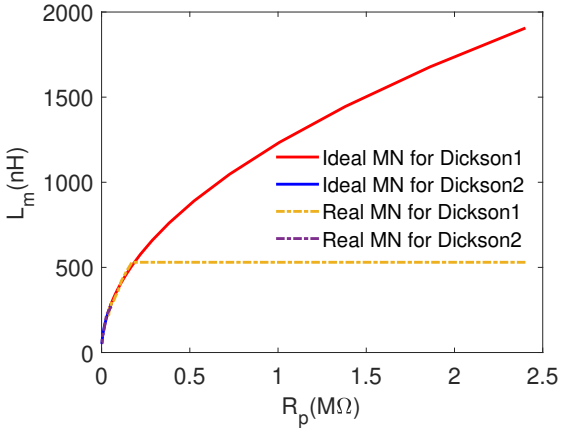


Fig. 7. Matching network inductance L_m vs. rectifier input resistance R_p.

In Fig. 7, it illustrates the calculated inductance and real inductor values from the 0402DF series with respect of the R_p [14]. The maximum inductor to be selected in the matching networks is 530 nH with 1000 MHz self-resonant frequency. In Fig. 8, it depicts the corresponding calculated and designed on-chip capacitors to realize maximum power transfer. The designed separate capacitance varies from 49 fF to 460 fF.

In Fig. 9(a), it presents the PCE of the matching network along with the source available power. For Dickson rectifier 1 used in -30 dBm∼-18 dBm, the PCE of the matching networks is from 85% to 97%. For Dickson rectifier 2 used in -18 dBm∼0 dBm, the PCE is from 98% to 99%. In Fig. 9(b), it

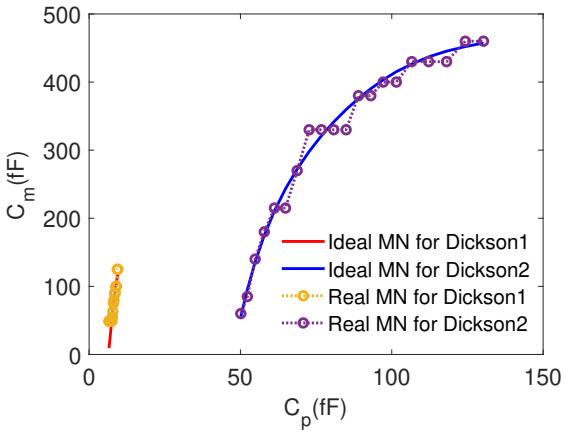
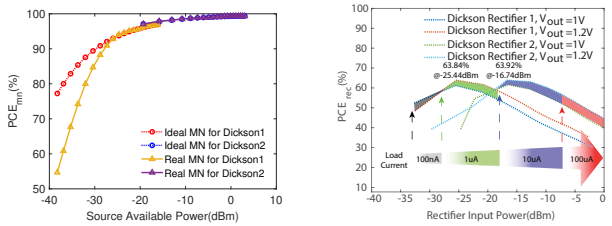


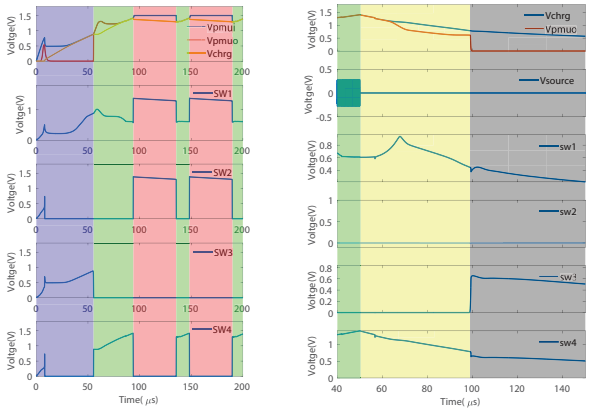
Fig. 8. Matching network capacitance C_m vs. rectifier input capacitance C_p.



(a) (b)

Fig. 9. (a) Matching network PCE vs. source available power and (b) Dual-channel rectifier PCE vs. rectifier input power.

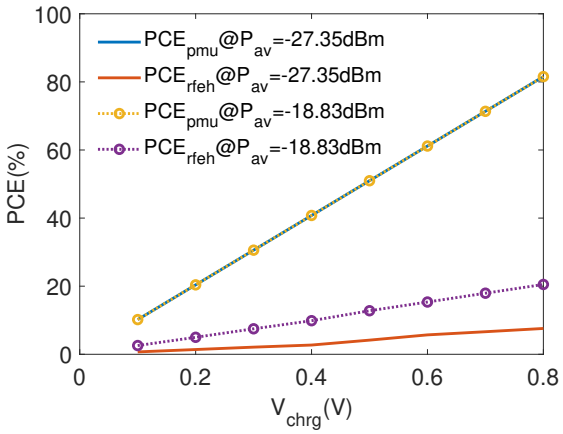
shows the PCE of the rectifier at the V_{pmui} range of 1 V∼1.2 V with the load current required by the signal processor. The maximum PCE of 63.84% and 63.92% are achieved at -25.44 dBm and -16.74 dBm.



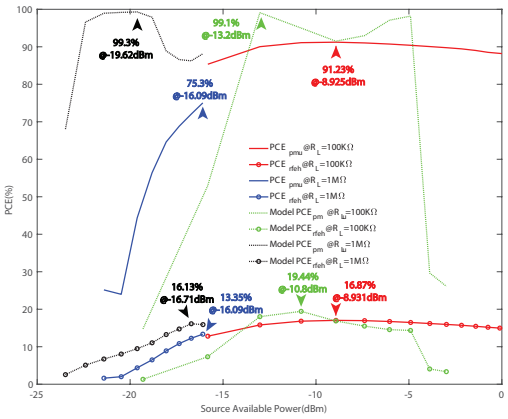
(a) (b)

Fig. 10. V_{pmui}, V_{chrg}, V_{pmuo} and switch control signals with respect of the (a) sufficient and (b) insufficient RF power.
Blue: low power harvesting mode; green: regular mode; red: overcharge mode; yellow: stored energy supply mode.

In the Fig. 10(a), it illustrates the simulated waveforms of the V_{pmui}, V_{chrg}, V_{pmuo} and the related switch control signals at -10.58 dBm rectifier input power. The $R1{\sim}R_4$ and C_{store} are selected as 100 MΩ and 1 nF, respectively. In the low power harvesting mode, the S_2 is on to charge the C_{store}. The V_{pmui} is low because of the low parallel resistance of the S_1 and the fully turned-on S_4. With the energy being collected, the PMU enters the regular mode. Since the V_{chrg} rises above 816 mV, the S_4 is off. The V_{pmui} is clamped at 1.2V to obtain the maximum PCE of the rectifier. The incoming energy is streamed to the C_{store} and the load. With the V_{chrg} reaches 1.4V, the overcharge mode is triggered to open the S_1 and S_2 to stop the excessive energy flowing in. The C_{store} is discharged to the load. Therefore, the V_{pmuo} ramps between 1.3V and 1.4V which provides enough supply for the OpAmp in the NMOS LDO, while does not harm the PCE. In the Fig. 10(b), it depicts the waveforms that power source suddenly becomes weak. The PMU switches to the stored energy supply mode until the V_{chrg} slides down to 816 mV. Once the S_3 is turned off to disconnect the load, the PMU it enters the shutdown mode.



(a)



(b)

Fig. 11. PCE of the PMU PCE_{pmu} and end-to-end energy harvester PCE_{rfeh} vs. (a) V_{chrg} in low energy harvesting mode and (b) source available power P_{av} in regular mode.

In Fig. 11(a), it depicts that the PMU PCE_{pmu} and RFEH end-to-end PCE_{rfeh} are proportional with the V_{chrg} in the low energy harvesting mode, where all the input currents are streamed to the C_{store} along with the V_{chrg} from 0.1 to 0.8 V.

TABLE II
PERFORMANCE COMPARISON OF THE STATE-OF-ART RF ENERGY HARVESTER

	[15]	[6]	[16]	[4]	[17]	[8]	This Work
Year	2015	2017	2019	2020	2020	2023	2024
CMOS Technology(nm)	180	180	180	180	180	65	180
Frequency(Hz)	830M	915M	915	403.5M	868M	915M	915M
Batteryless	Yes	Yes	No	Yes	Yes	Yes	Yes
System Architecture	CCDD rect + DC-DC	Reconfig. rect + Load regulation	Reconfig. rect + Load regulation	CCDD rect + DC-DC	Dickson rect + Load regulation	CCDD rect + Load regulation	Dickson rect + Load regulation
V_{out}(V)	1∼2	NA	0.4∼2.2	0.6	0.4∼1.7	0.4	1∼1.2
$R_{load}(\Omega)$	80K∼1M	1M	1M	3K∼200K	330K	10K	10K∼10M
Rectifier sensitivity(dBm) @ 1V V_{out} for R_{load}	NA	-14.8	17.8	NA	-15	-14.92	-27 for 1M*; -18 for 100K**
Peak $PCE_{rfeh}(\%)$	35.7@-15dBm	25@-5dBm	34.4@-1.3dBm	40.2@-9.1dBm	10.7@-13.3dBm	48.28@-14.92dBm	13.35@-16.09dBm*; 16.87@-8.9dBm**

NA: Not available; $*$: using Dickson rectifier1; $**$: using Dickson rectifier2.

At V_{chrg} = 816 mV, the PCE_{pmu}s are 81.55% at the P_{av} of -27.35 dBm and -18.83 dBm; while the PCE_{rfeh} are 10.38% and 20.73%. In Fig. 11(b), it presents the comparison between the PCE_{pmu} and PCE_{rfeh} obtained from the modeled and designed PMU. The model is the circuit replacing OpAmp and comparators with ideal devices. In the high power range, the maximum PCE_{pmu} and PCE_{rfeh} using the model achieves 99.1% and 19.44% at P_{av} of -13.2 dBm and -10.8 dBm with 100KΩ load. For the designed PMU, the maximum PCE_{pmu} and PCE_{rfeh} are 91.23% and 16.87% P_{av} of -8.9 dBm with the same load condition. In the low power range, the maximum PCE_{pmu} and PCE_{rfeh} from the model are at 99.3% and 16.13% at P_{av} between -19.62 dBm and -16.71 dBm with 1MΩ load. While the maximum PCE_{pmu} and PCE_{rfeh} extracted from the designed PMU are 75.3% and 13.35% at P_{av} of -16.09 dBm.

IV. CONCLUSION

A batteryless PMU is proposed for the 915 MHz RF energy harvesting sensors. The dual-channel Dickson rectifier is designed as the RFEH front-end to transfer the maximum PCE_{rec} of 63.84% and 63.92% below and above -18 dBm input power respectively. The PCE_{pmu} and the end-to-end PCE_{rfeh} reaches 91.23% and 16.87% at P_{av} of -8.9dBm. They are 75.3% and 13.35% at P_{av} of -16.09dBm.

ACKNOWLEDGMENT

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