Design of the Dual-channel Dickson Rectifier with Native NMOS for RF Energy Harvesting Sensors

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***Abstract*—We propose a dual-channel Dickson rectifier including two independent 1-stage rectifiers for the radio frequency (RF) energy harvesting sensors. It presents the characteristic model of the native NMOS and the leakage model of the Dickson rectifier. The power consumption model of the switch and charging time are derived. Further, 1-stage rectifiers with NMOS W/L=2μm/1μm and W/L=16μm/1μm are designed to work in the rectifier input power P_{rec_in} smaller and larger than -18 dBm, respectively. The maximum power conversion efficiency (PCE) are 63.84% and 63.92% in the two ranges. The size of the PMOS switch for charging the 1nF storage capacitor C_{store} is optimized as 100μm/180nm to minimize the power loss.**

***Index Terms*—Dual-channel, Dickson rectifier, native NMOS, power conversion efficiency, energy harvesting.**

I. Introduction

The development of the Internet of Things (IoTs) over the past decade has significantly shaped a wide range of application domains and technologies, like smart homes, health monitoring, wildlife protection and electrical vehicles [1], [2]. However, batteries as the power source for the networked device lead to a set of shortcomings, such as limited lifetime, bulky size and pollution [3]. Hence, RF powered sensors have been introduced and these sensors harvest energy from ambient wireless signals emitted by the communication infrastructure such as TV towers and WiFi access points [4]. They talk to each other based on the low-power communication link principle, backscatter [5], [6] and minimize the logic power consumption through adiabatic computing [7], [8].

In the conversion of incident RF energy to DC supply voltage, the rectifier plays an essential role and achieving high PCE from the antenna to the load over a wide range of input power is paramount [9]. Schottky diode with low turn-on voltage characteristic was a popular choice as the rectifying circuit element, however an additional required mask in the complementary metal–oxide–semiconductor(CMOS) fabrication process leads to higher manufacturing cost [10]. Several topologies with diode connected transistors have been used. Dickson rectifier offers an appealing structure to block the reverse current [11]. Cross-coupled rectifier has increased reverse leakage if the incoming voltage is larger than the threshold voltage of the transistor [12]. Self-body biasing are used to lower the forward threshold voltage and leakage current respectively [13]. Further, the reconfigurable architectures

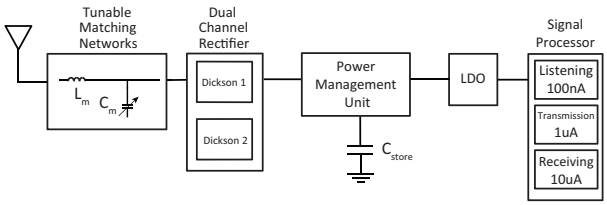


Fig. 1. Block diagram of the RF energy harvesting circuit in the sensory system-on-chip design.

are also proposed in the rectifier design to extend the working power range [14].

The organization of paper is as follows. Section II focuses on modeling of the leakage in the Dickson rectifier based on the I-V characteristic of the native NMOS. The charging model of C_{store} and the power consumption of the switch are also analyzed. Further, Section III presents the simulation results of sensitivities and PCE of the proposed rectifiers. Finally, Section IV provides the summary and conclusion.

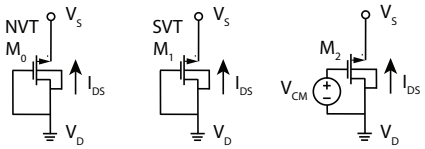
II. Proposed Dickson Rectifier Implementation

Fig. 1 depicts the block diagram of the proposed dual-channel Dickson rectifier with the tunable matching network and energy storage capacitor. In the dual-channel rectifier, there are two 1-stage rectifiers working in two distinct power ranges respectively in order to transfer the maximum power to their outputs. The L matching networks contain parallel inductors and capacitors which can be tuned by the switches once the input resistance and capacitance of the rectifier changes with variations of the input voltage and load. The power management unit is installed between the rectifier and the load to achieve the maximum power transmission. It also fixes the rectifier output between 1$\sim$1.2 V. In order to store the energy, a 1 nF film capacitor C_{store} is used [15]. Further, an ultra-low power low dropout voltage regulator(LDO) is applied to support the signal processor working in listening, transmission and receiving modes [16].

A. I_{ds} vs. V_{ds}

Native and standard V_{th} NMOS transistors of the Dickson rectifiers are illustrated in the Fig. 2(a)2(b). The NMOS model in the cross-coupled rectifier can be depicted as a transistor with a common mode voltage V_{cm} applied at the

gate, where V_{cm} equals the half of rectifier output voltage, in Fig. 2(c) [17].



(a) (b) (c)

Fig. 2. (a) Native V_{th} NMOS, (b) standard V_{th} NMOS in Dickson rectifiers and (c) NMOS in cross-coupled rectifiers

The current going through the MOSFET transistor contains mainly two part, which are the drain-source current I_{ds} and leakage current I_{leak}. I_{ds} follows the square law when the gate-source voltage V_{gs} is larger than the threshold voltage $V_{th,n}$ as shown below,

$$I_{ds} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{gs} - V_{th,n})^2 \tag{1}$$

where μ_n is the mobility of the electron, C_{ox} is the capacitance per unit area of the gate oxide.

The exponential relation should be taken into consideration once V_{gs} is smaller than $V_{th,n}$, where the NMOS is working in the subthreshold region [18]

$$I_{ds} = I_s e^{(V_{gs}-V_{\text{th}}-V_{\text{off}}/nV_{\text{T}})}\left[1 - e^{(-V_{ds}/V_{\text{T}})}\right] \tag{2}$$

In (2), I_s is the subthreshold saturation current. V_{off} is the offset voltage in subthreshold region for large W and L. n is the subthreshold swing factor. V_{ds} is drain-source voltage of the NMOS and V_T is the thermal voltage.

$$I_s = \frac{W}{L}\mu_n V_T^2\sqrt{\frac{q\varepsilon_{si}N_{ch}}{2\phi_s}}, \tag{3}$$

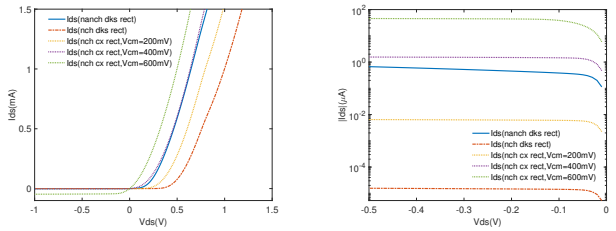
where ε_{si} is the relative permittivity of silicon dioxide, N_{ch} is the channel doping concentration and ϕ_s is the surface potential.

By sweeping the V_{ds} of the NMOS, the I-V functions of the native NMOS, SVT NMOS and NMOS with different V_{cm} values are plotted in Fig. 3. It illustrates that the native NMOS is able to generate much larger currents than the SVT NMOS. Even though, the large V_{cm} bias can make the forward I_{ds} increase greatly with small V_{ds} increments, the reverse I_{ds} of the transistor will contribute a lot to the power dissipation. This will limit the efficiency of the rectifier.

B. Leakage Model of the Dickson Rectifier

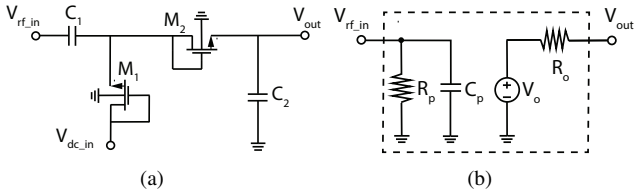
The proposed rectifier adopts the Dickson's structure which is shown in Fig. 4(a). Two diode connected native NMOS transistors are applied to allow the utilization of the low incident power since they have the negligible threshold voltage. Hereby, drain and leakage currents model based on the varying V_{rf_in} is analyzed and set up, meanwhile V_{dc_in} is tied to the ground. Besides, C_1 = C_2 = 400 fF.

The diode formed at the bulk-source junction will be turned on when V_{rf_in} goes below the ground where the bulk is



(a) (b)

Fig. 3. (a) I_{ds} vs. V_{ds} and (b) reversed $|I_{ds}|$ vs. V_{ds} of the Dickson and cross-coupled rectifiers.



(a) (b)

Fig. 4. (a) Schematic and (b) Thevenin equivalent model of the 1-stage Dickson rectifier.

connected. Hence, I_{leak} can be expressed as the diode current as the follows,

$$I_{leak} = I_{s0}[e^{(V_{bulk}-V_s)/V_T} - 1] \tag{4}$$

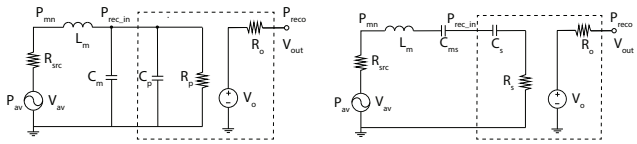
where I_{s0} is the reverse saturation current, V_{bulk} and V_s are the bulk voltage and the source voltage of the M1 and M2 respectively.

$$I_{s0} = A_{seff}J_{ss} + P_{seff}J_{sws} + W_{effcj}NFJ_{sswgs} \tag{5}$$

In (5), A_{seff} is the effective junction area on the source side, J_{ss} is the bottom junction reverse saturation current density, P_{seff} is the effective junction perimeter on the source side, J_{sws} is the isolation-edge sidewall reverse saturation current density, W_{effcj} is the effective source/drain diffusion width, NF is number of figners of a transistor, J_{sswgs} is the saturation current component through the gate-edge.

C. Design of the Matching Networks

The L-matching network, obtaining the name from the shape of the components' connection, is probably the most popular and simplest matching network structure [19]. Since R_p is larger than the R_{src} which is 50 Ω, the lowpass type of the L-matching network is selected to make R_s equal R_{src} with reasonable L_m and C_m values in the design in Fig. 5.



(a) (b)

Fig. 5. L-matching networks with Dickson rectifier of (a) parallel input resistance and capacitance and (b) series input resistance and capacitance.

From the voltage and power sensed at the input of rectifier, the rectifier can be modeled as a parallel resistor R_p and capacitor C_p, which can be expressed as the follows.

$$R_p = \frac{V_{rms}^2}{P_{rec\_in}} \tag{6}$$

$$C_p = \frac{1}{\omega R_p}\sqrt{\left(\frac{I_{rms}R_p}{V_{rms}}\right)^2 - 1} \tag{7}$$

The parallel RC model can be converted to a serial resistor R_s and capacitor C_s model in Fig. 5(b),

$$R_s = \frac{R_p}{1+Q^2} \tag{8}$$

$$C_s = \frac{C_p(1+Q^2)}{Q^2} \tag{9}$$

$$C_{ms} = \frac{C_m(1+Q^2)}{Q^2} \tag{10}$$

where Q is the quality factor [20].

$$Q = \sqrt{\left(\frac{R_p}{R_{src}}\right) - 1} \tag{11}$$

Thus, the impedance of the rectifier is

$$Z_{rect} = R_s + \frac{1}{j\omega C_s} \tag{12}$$

The inductance L_m and capacitance C_m of the L matching network are expressed as follows.

$$L_m = \frac{QR_{src}}{\omega} \tag{13}$$

$$C_m = \frac{Q}{\omega R_p} - C_p \tag{14}$$

In order to transfer the maximum power to the rectifier, the total impedance from the input of the matching networks should be equal as 50 Ω, by equating the imaginary part below to zero.

$$j\omega L_m + \frac{1}{j\omega C_{ms}} + \frac{1}{j\omega C_s} = 0 \tag{15}$$

D. Power Consumption of the Switch

In order to take advantage of the intermittent RF power, the energy should be collected and stored in a large capacitor. Therefore, the charging profile of the V_{out} and V_{chrg}, which is the voltage on the top plate of the storage capacitor C_{store}, is figured out in Fig. 6. The corresponding power consumption of the PMOS switch is analyzed and generalized into dynamic power consuming (DPC) region 1 and 2 and static power consuming (SPC) region 3.

In the DPC region, it can be divided as constant current charging (CCC) region 1 and decreasing current charging (DCC) region 2 from the aspect of changes of the charging current I_{chrg} into the C_{store}. In the CCC region, the DC component of the V_{out} keeps constant in a short time until V_{chrg} reaches the threshold voltage $|V_{th,p}|$ of the PMOS switch. Not like the NMOS, the PMOS switch is turned on

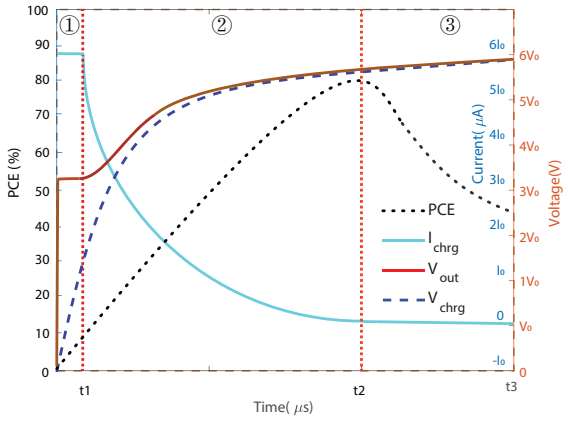


Fig. 6. Charging profile of the C_{store}.

to charge the C_{store} even at a very low V_{out}. Since the it is working in the saturation region, the charging current I_1 simply follows the square law expression.

The power consumed by the switch, equaling the area of the trapezoid surrounded by the voltages in the CCC region, is simplified as follows.

$$\begin{aligned} P_{sw1} &= \frac{1}{2}[(V_{out} - 0) + (V_{out} - |V_{th,p}|)]I_1 \\ &= \frac{1}{2}(2V_{out} - |V_{th,p}|)I_1 \end{aligned} \tag{16}$$

In the DCC region, the PMOS switch works in the linear region when V_{chrg} is from $|V_{th,p}|$ to where V_{out} and V_{chrg} almost verges. The charging current I_2 is written below,

$$I_2 = \mu_p C_{ox}\frac{W}{L}[(|V_{ds}| - |V_{th,p}|)|V_{ds}| - \frac{1}{2}|V_{ds}|^2] \tag{17}$$

where $|V_{ds}| = V_{out} - V_{chrg}$.

The power consumption of the PMOS switch in this region is shown as follows,

$$\begin{aligned} P_{sw2} &= \frac{\int_{t1}^{t2}(V_{out} - V_{chrg})I_2 dt}{t_2 - t_1} \\ &= \int_{t1}^{t2}(V_{out} - V_{chrg})^2 \mu_p C_{ox}\frac{W}{L}[(|V_{ds}| - \\ &\quad |V_{th,p}|) - \frac{1}{2}(V_{out} - V_{chrg})]dt/(t_2 - t_1) \end{aligned} \tag{18}$$

where t_1 is the time when V_{chrg} reaches $|V_{th,p}|$, t_2 is the time when V_{chrg} nearly catches up the open circuit voltage V_{oc}.

In the SPC region, the PMOS switch stays in the deep linear region. The difference of V_{out} and V_{chrg} becomes really small and C_{store} is getting close to the fully charged status. The charging current I_3 is expressed below.

$$I_3 = \mu_p C_{ox}\frac{W}{L}(|V_{gs}| - |V_{th,p}|)|V_{ds}| \tag{19}$$

The power consumption of the PMOS switch in this region is written as follows,

$$\begin{aligned} P_{sw3} &= \frac{\int_{t1}^{t2} R_{ds\_on} I_3^2 dt}{t_3 - t_2} \\ &= \frac{\int_{t1}^{t2}(|V_{gs}| - V_{th,p})|V_{ds}|^2 dt}{t_3 - t_2} \end{aligned} \tag{20}$$

where t_3 is the time when V_{ds} equals 0.

$$R_{ds\_on} = \frac{1}{\mu_p C_{ox} \frac{W}{L}(|V_{gs}| - |V_{th,p}|)} \tag{21}$$

From above equation of on resistance of the PMOS in linear region, it is known that a large W leads to the small resistance, which helps to reduce the static power.

E. Analysis of Charging C_{store}

Storage element as the power supply for the LDO which provides constant and stable current is required to be charged fast by the rectifier. The charging time t_c can be manipulated based on the equation expressed below,

$$\begin{aligned} P_{rec\_in}t_c &= P_{rec}t_c + P_{sw}t_c + \frac{1}{2}C_{store}V_{chrg}^2 \\ \eta P_{rec\_in}t_c &= P_{sw}t_c + \frac{1}{2}C_{store}V_{chrg}^2 \\ t_c &= \frac{C_{store}V_{chrg}^2}{2(\eta P_{rec\_in} - P_{sw})} \end{aligned} \tag{22}$$

where η is the PCE in the DPC region, P_{sw} is the power consumption of the switch.

Once the P_{rec_in}, C_{store} and V_{chrg} are given, the means to reduce t_c include improving η and reducing P_{sw}. From [21], it is known that V_{out} rises sharply with the increasing transistor size until the W/L ratio reaches around 50 for a certain V_{rf_in}. However, the PCE drops with an over large transistor size. Hence, the relation between V_{out} and P_{rec_in} should be figured out to design the input voltage of the LDO, which is required as 1 V at least. Also, the t_c and sensitivity are a pair of parameters need to be traded off.

III. Simulation Results

The proposed Dickson rectifier is designed in 180 nm CMOS technology and simulated in Cadence simulation environment. In Fig. 7, it illustrates the comparison between the simulation and calculation results of I_{ds} and I_{leak} of the NMOS of the 1-stage Dickson rectifier. V_s is source voltage of M1 when applying the 915MHz AC source with 2V amplitude to the rectifier input. I_{ds} decreases from 1.5mA to 131μA with the DC component of the V_s lifting up due to the effect of the rectifier. In the calculation model, I_{leak} keeps around just 24 fA even though the $V_{bs}(= V_{bulk} - V_{source})$ is larger than the diode turn-on voltage 200 mV, which is obtained from the I-V testbench of the single native NMOS. While, the ripples of the I_{leak} from the simulation are just coupling components, which will not contribute to the power consumption.

Since the LDO in our RF energy harvesting sensors requires 1V$\sim$1.2V input voltage, the outputs of rectifiers are aiming at these voltages in low power ranges. In Fig. 8(a) 8(b) and 9(a) 9(b), it presents V_{out} vs. P_{rec_in} for 1 and 4 stages Dickson and cross-coupled rectifiers under R_{load} of 10M, 1M, 100K and 10KΩ, which approximately correspond to I_{load} from 100 nA to 100 μA. Each color area covers the power range that generate at least 1V output for different W/L ratios of a rectifier until the load condition changes.

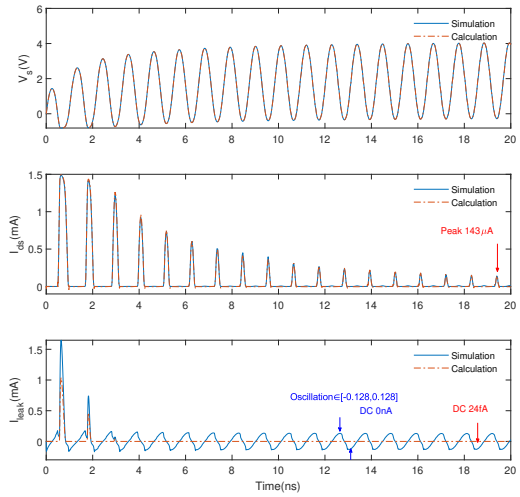


Fig. 7. Drain-source current I_{ds} and leakage current I_{leak} comparison between the simulation and calculation.

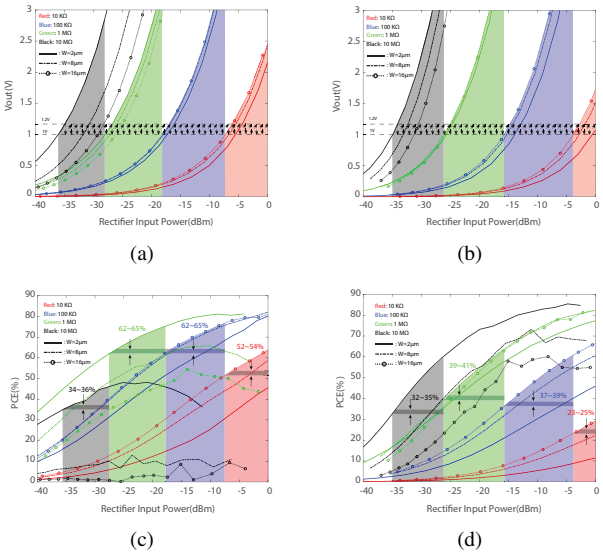


Fig. 8. Output voltage V_{out} vs. input power P_{rec_in} of (a) 1-stage and (b) 4-stage Dickson rectifier; power conversion efficiency PCE vs. P_{rec_in} of (c) 1-stage and (d) 4-stage Dickson rectifier.

The corresponding PCE are also plotted. In Fig. 8(c) 8(d), it illustrates that 1-stage Dickson rectifier with NMOS W/L of 16μm/1μm has PCE of 52$\sim$54% and 62$\sim$65% for R_{load} of 10KΩ and 100KΩ, which are higher than 4-stage Dickson rectifier. Moreover, 1-stage Dickson rectifier with NMOS W/L of 2μm/1μm provides the PCE of 62%$\sim$65% and 34%$\sim$36% which works better with 1MΩ and 10MΩ R_{load} than its 4-stage counterparts.

In Fig. 9(a), it is observed that the expected V_{out} is generated in the power range from -20 to -5 dBm when using 1-stage cross-coupled rectifier, though with the changing loads. This does not fit in with the low power requirement for the listening mode. For the 4-stage cross-coupled rectifier in

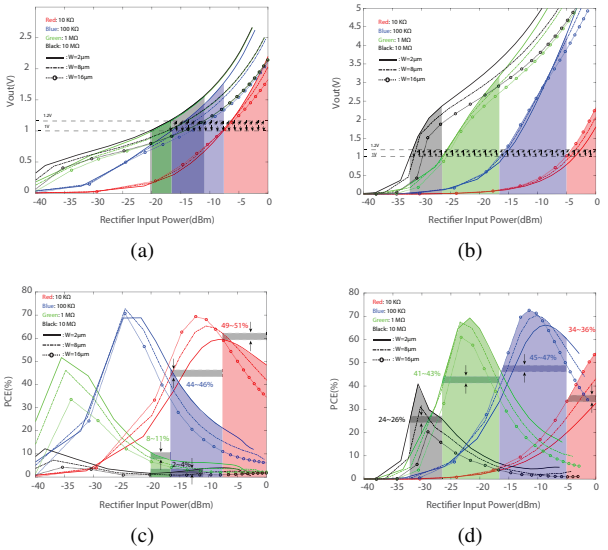


Fig. 9. Output voltage V_{out} vs. input power P_{rec_in} of (a) 1-stage and (b) 4-stage cross-coupled rectifier; power conversion efficiency PCE vs. P_{rec_in} of (c) 1-stage and (d) 4-stage cross-coupled rectifier.

Fig. 9(b), the sharp slope of the V_{out} around -32 dBm indicates that the rectifier does not work in function at this low power level. In Fig. 9(c) 9(d), 1 and 4 stages cross-coupled rectifiers show relative lower PCE than their Dickson counterparts.

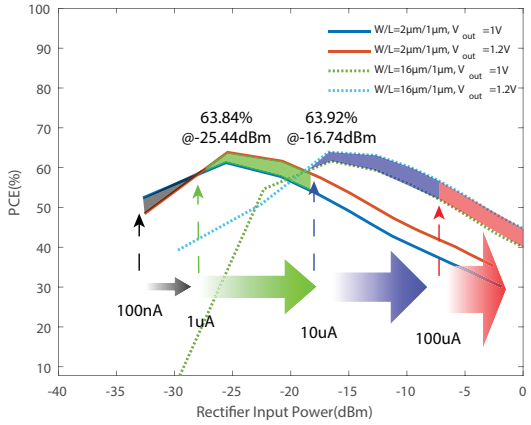


Fig. 10. Total rectifier's power conversion efficiency PCE vs. rectifier input power P_{rec_in}.

Therefore, the 1-stage Dickson rectifiers with NMOS W/L of 2μm/1μm and 16μm/1μm are selected in the design. To obtain PCE data with the continuously varying R_{load}, the proposed dual-channel Dickson rectifier is simulated with the V_{rec_in} from 100mV to 2V and the fixed V_{out} at 1V and 1.2V. In Fig. 10, it shows the PCE curves of the two chosen 1-stage Dickson rectifiers. For W/L=2μm/1μm, it displays the maximum PCE of 63.84% for the I_{load} between 1μA and 10μA; for W/L=16μm/1μm, it illustrates the maximum PCE of 63.92% for the I_{load} larger than 10μA.

For the charging PMOS switch design, it requires consuming power as less as possible when the signal processor is

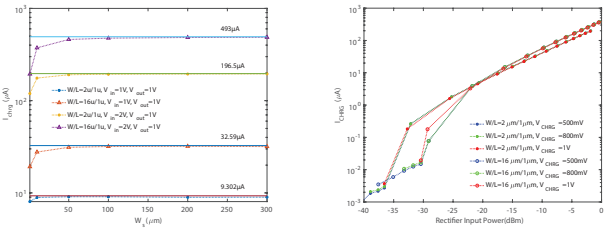


Fig. 11. (a) C_{store} charging current I_{chrg} vs. width of the charging switch W_s; (b) and charging voltage I_{chrg} vs. rectifier input power P_{rec_in}.

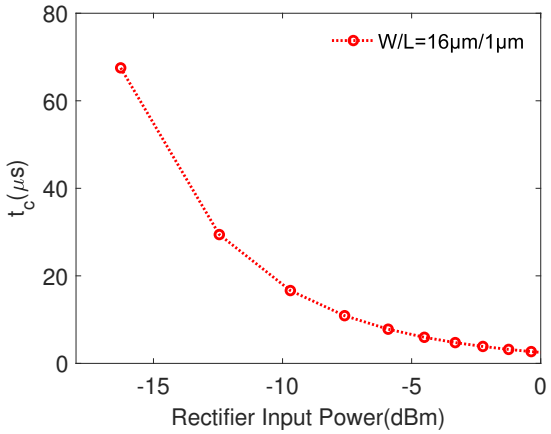


Fig. 12. Charging time t_c vs. rectifier input power P_{rec_in}.

working in the listening mode. Except 100 nA branched to the LDO, all the left current should be streamed to C_{store}. Thus, the switch should be easily working in the linear region when a low gate voltage is applied. Also, it is able to allow the sufficient amount of charging current go through. In Fig. 11(a), the width of the charging PMOS to 1 nF C_{store} is swept to attain I_{chrg}, which is plotted in dash lines. The results are compared with total I_{out}. The length of the switch is 180 nm. It is observed that the W_s of 100μm is the point where I_{chrg} starts to flat out, which means the switch can support such amount of current. In Fig. 11(b), it is known that the I_{chrg} is proportional to the P_{rec_in} once the rectifier design and switch size are determined. Moreover, Fig. 12 presents that the rectifier takes about 67.52μs to charge the C_{store} to 1V at P_{rec_in} of -16.27 dBm. Once P_{rec_in} is -0.3692 dBm, t_c reduces to 2.689μs.

IV. Conclusion

Obtaining sufficient efficiency of energy conversion for low incident RF power is critical for RF sensor operation using only ambient RF signals. We present a dual-channel rectifier that is optimized for low incident RF power that can support a wide range of active power consumption of the sensor in different modes of operation. Our future work will focus on the design of power management system that interfaces the proposed rectifier.

TABLE I
PERFORMANCE COMPARISON OF THE STATE-OF-ART DICKSON RECTIFIERS

	[22]	[23]	[24]	[14]	[25]	[26]	[27]	This Work
Year	2015	2017	2017	2019	2020	2020	2022	2024
CMOS Technology(nm)	130	180	65	130	65	180	130	180
Frequency(Hz)	902∼928M	915M	953M	820M	902M	868M	900M	915M
V_{out} Range(V)	0.5-5	NA	0.05∼3.6; 0.05∼0.55	0.3∼0.7	0.5∼4	0.4∼1.7	0.2∼8.2	1∼1.2
$R_{load}(\Omega)$	1M	1M	21.5K; 9.1K	4.7K∼220K	200K	330K	1M	10K∼10M
Peak $PCE_{rec}(\%)$	32@-15dBm	25@0dBm	84.37@-12.5dBm; 56.16@-15dBm	39@-5dBm	33@-8dBm	43@-11dBm	34.9@-10dBm	63.84@-25dBm*; 63.92@-17dBm*
Sensitivity(dBm) @ 1V V_{out} for R_{load}	-21.6	-14.8	-12.5 for 21.5K; NA	-3 for 4.7K	-20.2 for 1M	-15	-21.7	-27 for 1M*; -18 for 100K*

NA: Not available; $*$: simulation results.

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